

# fcCuBE<sup>®</sup>

## Flip Chip with Cu Pillar, Bond-on-Lead and Enhanced Processes

### Highlights

- Cu pillar with Pb-free cap enables ultra fine bump pitch for advanced silicon (Si) nodes ( $t_{0\leq} \leq 10\text{nm}$ ), increased I/O density with superior thermal and electro-migration performance
- Patented, routing-efficient Bond on Lead (BOL) interconnection structure eliminates ELK /ULK damage on advanced Si nodes (40/28/20/16/14/10nm)
- BOL eliminates Solder-on-Pad (no-SOP) and allows relaxation of line / space design rules to offer lowest flip chip substrate cost
- BOL w/ Open Solder Resist (SR) relaxes substrate design rules while enabling dense, efficient routing and lower cost substrate
- Compatible with either our uniquely developed Mass Reflow (MR) process or Thermo-Compression Bonding (TCB), and Laser Assisted Bonding (LAB)
- Lowest cost path to flip chip using Cu pillar: Typically a 10-30% cost reduction over standard flip chip packages for most designs

### Features

- In-house Cu pillar wafer bumping for 200 and 300mm wafers
- Ultra fine pitch capability: 150 $\mu\text{m}$  to 40 $\mu\text{m}$  bump pitch
- 0.35mm minimum package ball (BGA) pitch in production
- MR process supports bump pitches down to 60 $\mu\text{m}$  and below
- Mold Underfill (MUF) further reduces package size and enables higher production throughput
- Non-conductive Paste (NCP) available for TCB
- Bumped wafer thinning: 60 $\mu\text{m}$  Si thickness in production, 50 $\mu\text{m}$  qualified
- Conventional 2/4 layer laminate, laminate build-up (BU), ABF BU substrates, and coreless embedded trace substrate (ETS)
- Layer count reduction (6L to 4L, 4L to 2L) or 1-2-1 Build up to 4L PTH (2L with low cost BOM enables lowest cost flip chip solution)
- High Density (HD), and Ultra High Density (UHD) matrix strip for fcCSP and wide boat format for singulated fcBGA
- Broad fab node compatibility: 180n, 65n-LK, 40/28/20/10nm/ELK-ULK
- Applicable across broad package range: fcBGA, fcBGA-H, fcCSP, fcCSP-H, fcCSP-Hybrid, MLP fcPoP, Interposer PoP, Bare Die fcPoP and 3D TSV interconnect
- Available in a wide range of package body sizes: 7x7mm to 35x35mm

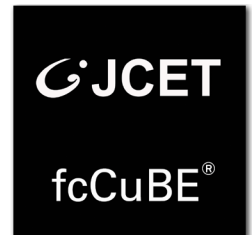
Our patented fcCuBE<sup>®</sup> technology is a low cost, high performance, advanced flip chip packaging technology that features copper (Cu) pillar bumps, Bond-on-Lead (BOL) interconnection and other enhanced assembly processes. Since receiving our first fcCuBE-related patent in 2006 on the innovative BOL process, we have developed this transformative technology into the flip chip platform of choice for mobile applications. fcCuBE is gaining wider customer adoption in cost sensitive markets where the performance and cost advantages of flip chip interconnect may not have been feasible before, from mobile and consumer to networking, automotive, and cloud computing where routing density and performance are imperative.

fcCuBE's unique BOL interconnect structure provides scalability to very fine bump pitches and high I/O while alleviating stress-related chip to package interaction (CPI), a common phenomenon associated with lead free and copper pillar bump structures. This is particularly important for mid to high-end networking and consumer applications.

### Scalability, Reliability and Performance

In conjunction with higher performance copper pillar interconnect, our patented, routing-efficient BOL interconnection structure expands the scalability of flip chip technology to ultra fine bump pitches ( $t_{0\leq} \leq 40\mu\text{m}$ ) and higher I/O densities and eliminates stress on delicate ELK/ULK structures at advanced silicon wafer nodes. BOL further enables substrate design rule simplification, elimination of tight Solder Resist Registration (SRR) rules, and elimination of Solder-on-Pad (SOP). This combination of results in a high performance, low cost solution which also allows greater design flexibility and a streamlined manufacturing process. fcCuBE's robust interconnect structure effectively alleviates thermo-mechanical stress which is a common phenomenon in advanced Si node ELK/ULK die with Cu pillar bump.

A unique feature of fcCuBE is the inherent compatibility with both standard Mass Reflow (MR) assembly, Thermo-Compression Bonding (TCB) or our recently introduced Laser Assisted Bonding (LAB). Our uniquely developed MR process, which utilizes either Mold Underfill (MUF) or Capillary Underfill (CUF), supports bump pitches down to 60 $\mu\text{m}$  and below, providing customers a lower cost alternative to TCB or LAB at these pitches. TCB or LAB is utilized for more complex face-to-back or face-to-face bonding of processes necessitated by Through Silicon Via (TSV) technology. Reflow method is determined by Si node, pitch, I/O design and product time to market.



## Specifications

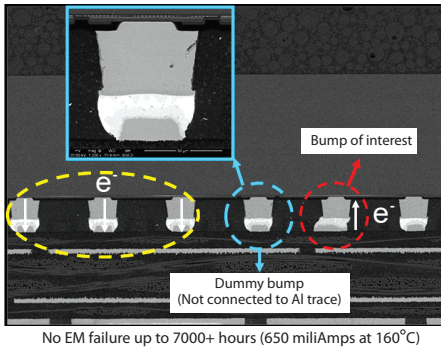
Package Thickness	0.55-2.9mm
Die Thickness	200mm wafers: 100-710 $\mu$ m (4-28mils) 300mm wafers: 60-810 $\mu$ m (2.5-32mils)
Bump Pitch	fcCSP: 40/80 $\mu$ m (qualified) fcBGA: 80 $\mu$ m (qualified)
Effective Bump Pitch	fcCSP 40/80 $\mu$ m w/1 line btw bumps (qualified) fcBGA 62.5 $\mu$ m w/1 line btw bumps (qualified)
Marking	Ink or laser

## Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a 13 x 13mm fCLCSP with a die size of 6.0 x 8.0mm and frequency of 100MHz.

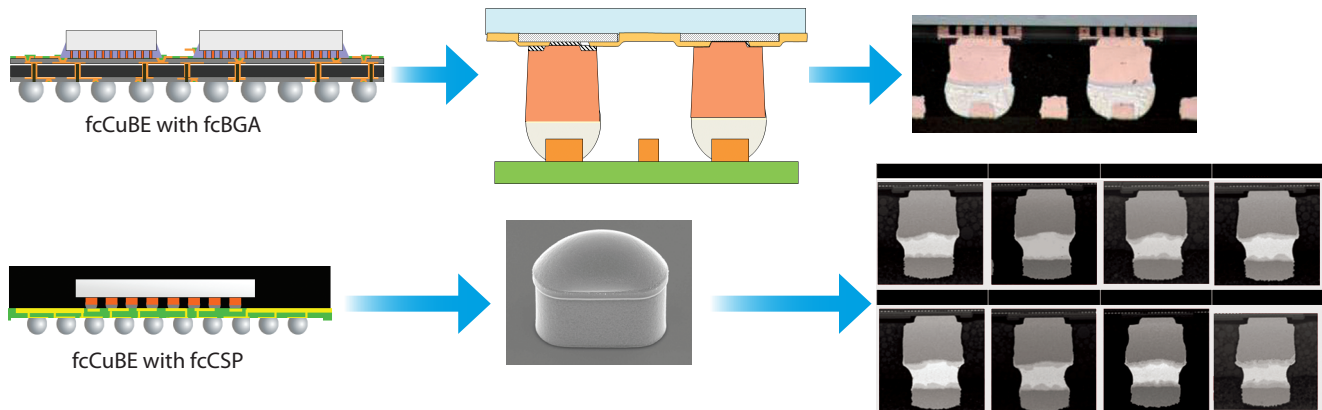
Length	Inductance (nH)	Capacitance (pF)	Resistance (m $\Omega$ )
Self (short)	0.89	0.65	18.3
Mutual	0.24	0.11	
Self (long)	1.78	0.73	32.5
Mutual	0.51	0.12	

Note: Net = Total Trace Length + Via + Solder Ball.



No EM failure up to 7000+ hours (650 milliAmps at 160°C)

## Cross Sections



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## Reliability

Excellent reliability margins: passed 3000 cycles for TCB and 3000 hours for HTS (well above industry standard requirement of 1000x each)

Moisture Sensitivity Level	JEDEC Level 3 @ 260°C
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiased HAST	130°C, 85% RH, 2 atm, 96 hrs (typical)

## Thermal Performance

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation and/or measurement for specific cases should be performed for maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Performance ja $\theta^{\circ}$ C/W
fcLCSP	7x7	49	4.6 x 5.0	46.0
fcCSPLGA	13x13	144	5.5 x 5.5	27.7
fcBGA-H	35 x 35	1084	10.0 x 10.0	11.2/8.0* (8.4/4.4*)

Note: Simulation data based on package mounted to 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2; \* represents cases with extruded Aluminium heat sink; numbers in parentheses are for 2 m/sec air flow and provided for reference for applications that provide fans or other forms of air flow in the system.

## Applications

fcCuBE<sup>®</sup> technology is a compelling solution for a wide cross section of end products in the low to high end mobile market, as well as mid to high end consumer and cloud computing markets:

- Mobile: application processors, baseband processors, PMIC, connectivity, RFIC, PA, touchscreen controllers, audio codec
- Consumer: GPS, set top box chipsets, gaming consoles, GPUs, memory controllers, DTV, application processors, video processors, image/signal processors, CPU
- Cloud computing: ASIC, DSP, broadband processors, FPGA, ASSP, Ethernet processors, network storage, network switches
- Automotive: Dashboard applications

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