The development and evaluation of RF TSV for 3D IPD applications

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***Abstract*—** In this paper, Silex Microsystems, the world's largest Pure-Play MEMS foundry, together with partners TNO and VTT, present our recent advancements in RF through silicon Vias (TSV) for 3D integrated passive devices (IPD) applications, achieved in conjunction with the European consortium EPAMO.

A novel open TSV fabrication process on 200 mm diameter 305 µm thick High Resistivity wafers has been used to demonstrated High Aspect Ratio Through Silicon Vias (HAR TSV), focusing on tight pitch, resulting in 36 TSV/mm2 Via density. 305 µm wafer thickness enables the fabrication of rigid interposers, an advancement in the commercialization of 3D packaging technology. The fabrication includes double sided deep reactive ion etching (DRIE), developments and evaluation on various conformal high aspect ratio (HAR) plating seedlayer processes, and void-free TSV Cu plating of open rigid TSV structures and bonding to glass wafers for characterization. The electrical characterization of the fabricated devices was performed by VTT with excellent measured RF properties: in specific, low RF losses as well as low DC resistances of less than 20 mOhm/TSV. Several different coplanar waveguide (CPW) test vehicles and other RF TSV test structures together with Daisy Chain and parasitic Capacitance test structures were designed, fabricated and evaluated. **The loss of a single coplanar TSV transition is less than 0.04 dB @ 5 GHz,** which is considered to be very small.

The developed TSV technology was also employed to fabricate 3D toroidal inductors. These inductors were characterized by TNO showing high Q-factor (>30) and self-resonance frequency (> 6 GHz) for 3D inductors in the range of 1-15 nH. 1 and 2 port inductor temperature characteristics over temperature interval from room temperature to 111°C are reported. A fabrication integration scheme for fully integrated RF-IPD with 3D TSV based inductors and high ohmic polysilicon (p-Si) resistors and piezoelectric (PZT) metal-insulator-metal (MIM) capacitors are discussed. Outlook for improvements using integrated high frequency magnetic flux materials and commercialization aspects are described.

Keywords*—*MEMS Manufacturing, RF TSV, 3D IPD, Toroidal Inductors, Q-value, RF Losses, HAR TSV, Cu plating, 3D Mechnical Stress, Reliablity, Thermal Characterization, Signal and Power Integrity.

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I. Introduction

Current and future wireless communication systems need to cope with the increased number of frequency bands and advanced mobile phone standards like LTE and LTE-A supporting high data rates. At the same time mobile phone systems have to become more energy-efficient in order to contribute to the Grand Challenge of "CO_2-reduction". One major limitation of today's mobile phones is the poor impedance matching of the antenna to the RF-front-end section of the mobile phone leading to overall poor antenna efficiency. In addition the ongoing trend towards higher miniaturization and integration is an ever increasing challenge in the design of complex RF systems, for example due to critical RF interaction on signal lines. By introducing tuneable RF-elements, the overall system architecture can be simplified leading also to a significant cost reduction for future RF-systems. Therefore the development of RF-MEMS 3D components is a key enabler for future highly advanced and energy efficient RF systems.

Similarly, the advancement of IC technologies with escalating costs for each successive processing node making new IC development more and more costly, in conjunction with packaging trends (especially in the mobile space) where higher levels of integration and packaging density are required by the industry, has led to widespread focus on 2.5D and 3D packaging technologies.

Where RF signal handling is a critical factor, Through-Glass Vias (TGVs) have emerged as the contemporary preferred solution where practical, due to inherent very low capacitive coupling possible with an all-glass substrate. TGVs used in wafer capping are currently in use at Silex Microsystems for RF capping applications, for example.

Being able to use the more flexible processing that silicon allows, though, has spurred the investigation and development of RF capable High-Res Silicon solutions, as demonstrated in this paper. Traditional silicon interposers present challenges in manufacturing and handling due to the need to thin the wafers down to 50 µm or less during processing. An interposer solution which can avoid the inherent difficulties of thin wafer handling is seen as a key advancement in 3D interposer technologies.

Within the EPAMO consortium [1], which consist of 15 partners, the four main challenges of providing future high performance RF-systems has been addressed, energy efficient mobile communication systems, highly miniaturized and integrated RF components, and cost efficient solutions to the mobile phone industry by exploring and implementing

multiple innovative process and testing technologies to realize an adaptive antenna front-end system for 4G mobile phones. One of the main building blocks of the overall front-end is the adaptive antenna tuner, consisting of MEMS switches, passive RF 3D IPD devices, as schematically shown in Fig 1.

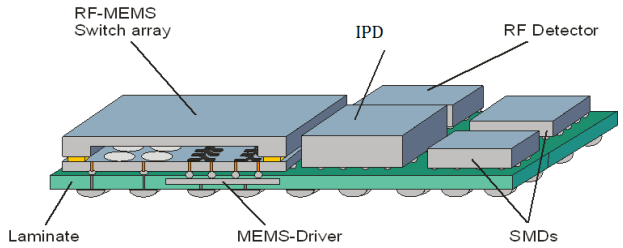


Fig. 1. Schematic view of EPAMO consortiums approach for a high-density integrated adaptive RF front-end antenna module with RF-MEMS switch array and embedded Integrated Passive (3D RF-IPD) die with TSVs and 3D Inductors on thin laminate substrates. The complete module will finally be overmoulded.

An advanced wafer level package technology and miniaturized thin film-based IPDs replacing conventional SMDs [2] is mandatory considering current major cost drivers for heterogeneous integration of size restrictions of packaging and mounting technologies. By realizing a hermetic wafer level package for the MEMS switches exhibiting RF capable fine pitch TSVs, the MEMS device size and therefore costs can be significantly reduced by having a true 3D interconnect technology.

High-Q inductors are part of the Integrated Passive Device (IPD) and they are required to build a matching network that can both correct the real as well the imaginary part of the signal. Miniaturized on-chip inductors therefore represent a critical element in the overall system. Due to the relatively low Q-factor value reported so far for on-chip semiconductor thin film components [2], new innovative solutions are desired.

Developments of new kind of 3D TSV based on-chip inductors with Q-factors above 30 for 0.5-4 GHz frequency range covering an area below 1 mm^2 for inductances of few nH are targeted in the EPAMO project. Low loss rigid TSVs are required for realization of such Inductors and will be presented in this paper.

In the case of planar inductors, several solutions have been investigated in order to obtain sensible improvements in the achieved Q-factor values. They are based on layout optimization [3], taking into account the contribution associated to both conductive and magnetically induced losses. Furthermore, magnetic losses can be reduced by properly inserting doped regions, creating blocking junctions against eddy currents [4]. However, sensible improvements in the Q-factor values are achieved especially at high operating frequencies.

Most industry-adopted three-dimensional configurations consist in the use of Stressed Metal (SM) and Through-Substrate-Via (TSV) technology. In the former case [5], both high Q-factor (e.g. 50-60) values and high self-resonance frequencies can be achieved only in correspondence of low inductance values. Since the Q factor and the self-resonant frequency of an inductor are determined by its inductance value, parasitic capacitance and resistance [6] a Cu based TSV process integration technology compatible also for integrating other passive functions is a key for success.

In the development of high-Q 3D inductors based on TSV technology, a key-factor is represented by the DC and RF resistance introduced by the Vias, relative to the substrate thickness [7]. High resistivity silicon (HR-Si) with resistivities above 3 kΩ-cm (preferably 10 kΩ-cm) are therefore needed. Special surface-passivated HR-Si techniques as proposed by Chen *et al* [6] is attractive to further reduce the substrate losses.

In the area of 3D packaging, the vertical chip stacking which is made possible by the metalized TSVs allows for higher performance in a smaller package space than conventional wirebonding or BGA assembly. Smaller package size means yields performance by shortening the distances traveled by high frequency IC signals. Parasitic capacitances likewise decrease, and the overall size and power consumption of the package is decreased. To do this, the TSVs must have low RF and DC losses (<30 mOhm per Via) and need to be isolated from the substrate to minimize capacitive coupling.

Additional passive functionality will be integrated into the EPAMO IPD die illustrated in Fig.1, including high Q inductors with the smallest possible size by using three dimensional windings enabled by the TSV technology. As a joint effort, VTT (the Technical Research Centre of Finland) and TNO of the Netherlands designed RF TSV structures and inductors which were fabricated by Silex Microsystems on its production 8" MEMS foundry line in Järfälla Sweden, and then fully tested for RF-characterization of the inductors.

II. TEHCNICAL DESCRIPTION

A. *TSV dimension design considerations*

For designing the 3D inductor demonstrators in this paper a strategic decision was made not to focus on smaller dimensions (i.e. 50 µm diameter) allowing 150 µm Via pitch since the RF- and the inductors properties would not benefit much from these smaller dimensions. Furthermore, as simulations showed that the Q factor of the inductors goes up when increasing the wafer thickness, the adopted approach of using a 305 µm thick wafer and TSVs with a 240 µm pitch was considered a good compromise between Q-factor and size of the inductors. As well, the CPW and RF TSV test structures were designed with those TSV dimensions in mind. Therefore the major focus in this paper is on TSV with 90 µm diameter Vias and the processes for fabricating these. It should be noted, however, that 50 µm Vias with aspect ratio of 6:1 have also been fabricated as part of this study.

B. *Manufacturing of Metalized Through Silicon Vias*

The microfabrication is performed with either a four or five mask process using 200 mm diameter Si substrates, as shown in Fig. 2. To minimize and reduce the risks of losses, the silicon substrate used was 305 µm thick high resistivity MCZ silicon wafers (3-10 kΩ-cm) from Okmetic Oyj. If regular CZ Si-wafers had been used with low resistivity (≦50 Ω-cm), the magnetic fields would penetrate deeply into the substrate causing losses and reducing both the inductance and Q-factor [2], and be a very lossy medium for RF signals [6].

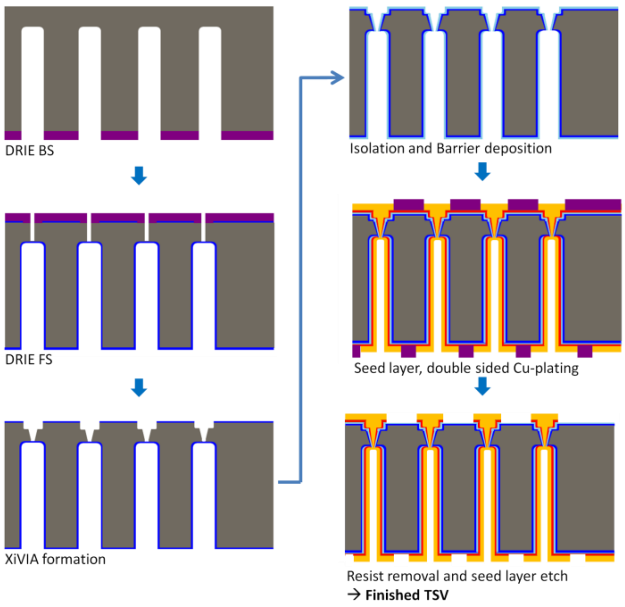


Fig. 2. Established process flow of the metalized TSV at Silex.

The fabricated TSV consists of a double sided etched open X-shaped-looking hole (XiVIA™) with a wider and a smaller part. The wider backside (BS) Via hole is designed with either a 50 µm or a 90 µm diameter with 280 ±10 µm depth, giving the aspect ratio (AR) of 6:1 respectively 3:1. The target goal is to achieve Vias with straight or even re-entrant wall profile, to decrease the shadowing effect while deposition of a conformal seed layer. Also, a re-entrant wall profile will ease the wetting and plating of the Vias. To be able to close the Via, a tapered structure should meet the Via from the front side (FS), with dimensions of 25 ±10 µm deep, surface opening and bottom 8 ±3 µm, see Fig. 3.

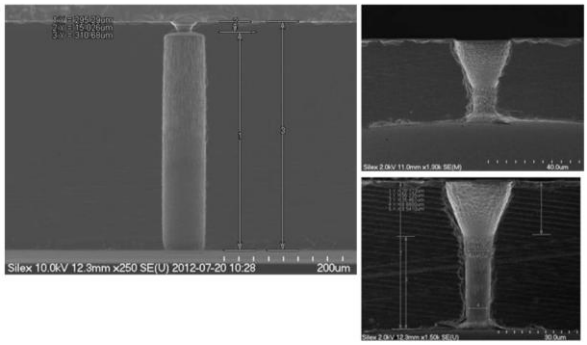


Fig. 3. SEM pictures of the after the finished DRIE development and optimization of tapered TSV structures for Met-Via50. The left picture showing the complete profile with 305 µm thick wafer (AR 6:1) and the right ones are a close-up of different XiVIA™ locking features in the small FS Via.

Different etching approaches were developed to get the tapered X-Via profile which requires two DRIE steps, where anisotropic and isotropic etches has been used. The X-shaped profile is desired since it locks the structure improving the mechanical reliability of the TSV and eases the complete void free metal filling of the FS Via in downstream processing steps. All the used DRIE steps have been using Bosch-processes in SPTS Pegasus or DSI 8" chambers available at Silex Microsystems, with different parameters in order to obtain the desired profiles.

After achieving the desired Via profile a deposition of insulation and barrier layers as well as a conductive Cu seed layer were executed as shown in Fig. 2. Of all the different deposition methods that were evaluated (including LP/PE-CVD, iPVD, ALD, and wet e-less plating [8]) the HAR MOCVD TiN/Cu technology deposition was found to provide best working seed layer with high conformality and thickness suitable for the electroplating Cu metallization step to follow. However several optimization runs were required as initial iterations sometimes showed non-conformal seed layer in the FS Via. This was discovered by small embedded voids obtained in the FS Via during Cu-electroplating, see Fig. 4. Such air voids could give reliability issues during operation of the devices.

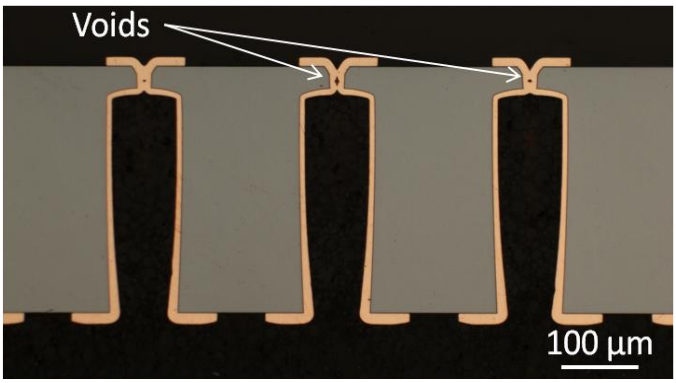


Fig. 4. Example of Cu Met-Via® (with X-shaped TSV structures) TSVs from Silex with 90 µm diameter Via and 240 µm pitch in 305 µm rigid wafers. Voids is obtained by electroplating TSV with non conformal seed layer.

Closer investigation showed that when just a thin seed layer (<20-30 nm, see Table I.) was present at the intersection between the FS and BS Via parts, as shown in Fig. 5, an increased risk for void formation during the Cu plating such as shown in Fig. 4 was sometimes obtained. This thin seedlayer effect is most likely due to a "shimmy" effect while processing the open Via holes.

TABLE I. MEASUREMENTS OF THE BARRIER AND SEED LAYER THICKNESS AFTER DEPOSITION RUN#1

Measure-points	**Layer thickness**		
	Barrier layer [nm]	***Seed layer [nm]***	***Remarks***
MP 1	69,78	142,4	100% (field)
MP 2	80,39	44,6	31%
MP 3	85,09	25,53	18%
MP 4	89,32	24,56	17%
MP 5	97,24	~20	Closed layer, rough
MP 6	134	~20	
MP 7	62,48	54,04	Deposited from BS
MP 8	62,61	73,79	
MP 9	72,95	154,8	

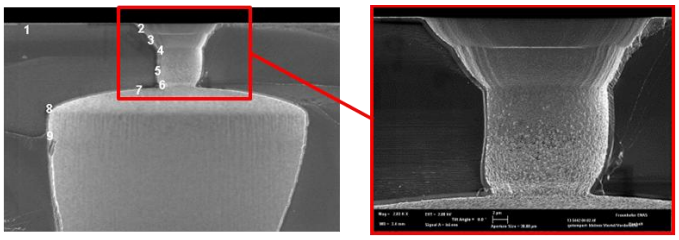


Fig. 5. SEM images showing the non perfect conformality of the Cu seed layer in the FS Via and the measurepoints used for the thickness measurements in Table 1.

Optimization of the seedlayer process and realized void-free Vias with a conformal line Cu film along the BS wall and the FS hermetic seal were achieved. The electroplated Cu was performed in a specially design plating tool, enabling cost effective simultaneous double sided plating and TSV sealing using thick dry film resist as plating masks for the Re-Distributions Layers (RDLs). Experiments were also carried out on modified RENA and SemiTool Cu plating systems available in Silex's 8" MEMS foundry line but with less successful results. The acid-based Cu plating contains Cu Sulfate ($CuSO_4$), chloride ions (Cl^-) based electrolyte, and organic additives chemistries provided by DOW and Enthone. By proper mixing, a desired conformal film and void free hermetic sealing of the small front side Via hole was obtained as shown in Fig. 6.

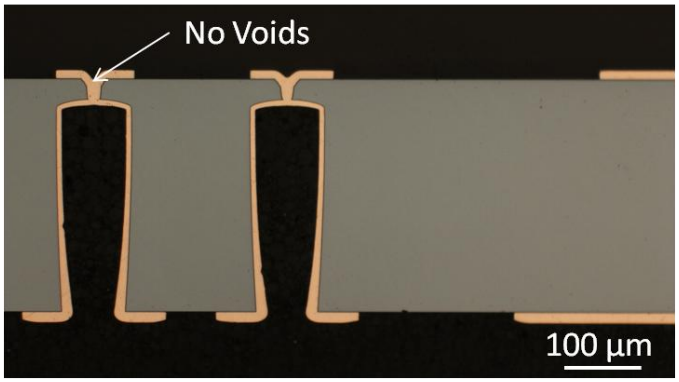


Fig. 6.. Example of void free and conformal plated Cu Vias (with X-shaped TSV structures) made by Silex with 90 µm diameter Via and 240 µm pitch in 305 µm rigid wafers. Image after seed and barrier layers are removed allowing very high DC insulation between the neigbourhing Vias.

HAR TSV Cu plating with blind Via structures and bottom up plating are challenging but with careful optimization of additives and the plating parameters it is possible to obtain void free TSV as described by Chen et al [6]. However, the plating time Chen et. al. used to achieve the void free RF TSVs structures are in the 20 hour/wafer range. A more production friendly plating process is therefore required for commercialization. With the XiVIA™ open TSV structures several advantages are obtained. The benefit by double sided plating using the open Vias is the enabling of a higher flow through the Vias of the Cu-plating chemistry (exchange) resulting in more conformal plating. Furthermore, since there is then no multi-metal interface between the front and backside RDLs the risk for RF losses by impedance mismatch or interface contact resistance are avoided as with conventional blind Via fabrication and Via reveal processes.

Since the skin depth for Cu for RF signals in the GHz range is in the µm range (skin depth at 5 GHz is approximately 0.9µm) complete filled Vias are not needed. A uniform and smooth Cu liner on the BS Via part of the XiVIA™ structure gives low enough RF and DC losses. Further, the reliability issues associated to thermal mismatch between Cu and Silicon is minimized when not filling the Vias completely and only rely on a local hermetic seal in the X-structured Via.

By proper mixing of adhesives and brightener in Cu plating solution, desired Cu grain structures and RDLs with smooth surfaces are obtained which is advantageous for low losses in RF applications. With the optimized chemistry and multistep plating using 0.3 A/dm^2 for 10 min, 1.0 A/dm^2 for 30-50 min and 1.3 A/dm^2 for 10-25 min, void free hermetic sealed RF TSV structures were obtained. This plating time is a >20x reduction of the plating time used by Chen et. al. [6] for other RF TSV structures using similar dimensions (i.e. 300 µm thick TSVs with 90 µm Via diameter).

The yield of conformal plated Vias was further increased by optimizing the pre-wetting steps, facilitating the wetting during plating. Also, introduction of a quick Cu-etch step was necessary in order to remove potential formed copper oxide, which would decrease the adhesion of the electroplated Cu. This means a minimum thickness of the Cu seed layers of approximately 40-50 nm is required for void free plating (compare Figs. 4-6.). The final thickness of the plated Cu was approximately 10 µm, sufficient for low ohmic DC Via resistance as well as RF signals. This thickness also completely and with zero voids seals the small FS Via hole. This is an essential feature for reliability concerns for the packaging approach, as described in Fig 1. Hermetic Vias are required for back-end packaging processes such as under fill in flip chip and overmolding or mold embedded Si packaging techniques [11].

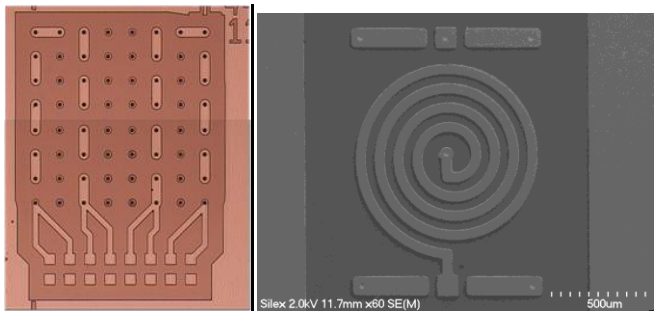
The final step in manufacturing the metalized TSVs is to remove the conductive seed layer and the barrier layer to isolate the Vias and create separated 3D connections between BS and FS, as shown in Fig. 2. This is preferably done by wet single or double sided etching.

C. RF TSV designs

To demonstrate the suitability of copper TSV technology to RF applications, TSV based RF transitions, transmission lines and inductors were designed by VTT and TNO, Daisy chain topographies with the manufactured TSVs as shown in Fig. 8 were used for DC measurement to evaluate the Via resistance.

Fig. 7. Schematic view of a TSV transition from CPW transmission line on the top side of the wafer to the CPW transmission line on the bottom side.

The main challenge in TSV based RF transitions is to have wideband 50 Ohm impedance which is needed for good matching. The following figure shows simulated transition from top metal co-planar waveguide (CPW) to the bottom side metal CPW transmission line with 90 µm Via diameter and 300 µm Via pitch., see Fig. 7.



a) *b)*

Fig. 8. ***a)*** Optical picture of the TSV daisy chain used for the DC Via resistance characterization, after Cu-plating with removed resist (seed layer still present). ***b)***SEM of a reference planar 4 turn Inductor.

3D inductors structures were also designed as a device demonstrator of the rigid TSV technology, where the amount of turns were varied from one to eight, illustrated in Fig. 9. Fig. 10. shows a top view of the finished 3D inductor structure with eight turns fabricated according to process flow shown in Fig. 2.

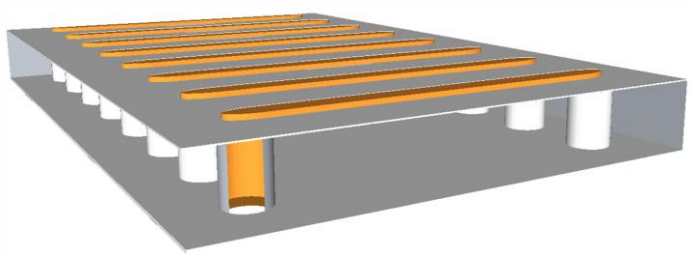


Fig. 9. Schematic cross-section view of the using three dimensional inductors enabled by the developed TSV technology.

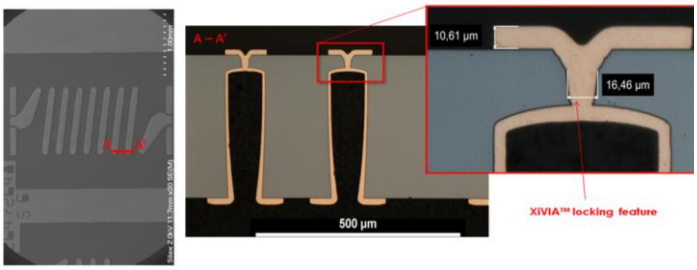


Fig. 10. A SEM image of the finished 3D Coil structure, seen from above (FS) to the left, and homogenous filled Met-Via TSVs with a close-up of the XiVIA locking feature in the cross section to the right (Silex license the XiVIA™ technology from ÅAC Microtec AB, Sweden).

In order to perform wafer level probing of both DC Daisy Chain test structures as the fabricated 3D Inductors some of the finalized wafers were temporary bonded to glass substrate carriers in order to avoid short from metalized wafer chucks in the probe station.

III. RESULTS

A. DC Via resistance by Silex

The Via resistance was measured with an Agilent 34401A 6 1/2 Digital Multimeter and a Karl SUSS PM5 probe station, where PCM die with Via daisy chains were characterized at Silex Microsystems using temporary glass carriers. A total of 712 TSV test structures, divided on three different wafers mounted on glass carriers, were evaluated and only eight Vias showed interruption, which states a TSV yield of greater than 98%. The mean Via resistance of the fully functional Vias were around 20 mΩ. Further development and yield optimization is currently in progress at Silex

B. RF TSV Characterization by VTT

The RF properties of TSV transitions were characterized by measuring S-parameters of the transitions. The measurements were carried out using on-wafer test setup with vector network analyser. The S-parameters of the RF test structures were measured from 10 MHz up to 10 GHz at room temperature. The test setup was calibrated so that the reference plane in the measurements is at the probe tips using line-reflect-reflect-match (LRRM) calibration method. Agilent network analyzer, CascadeMicrotech Infinity probes and CascadeMicrotech Summit 12K semi-automatic probe station were used in the measurements. As both sides of the wafers included patterned metal structures, the wafer was insulated from the metal chuck of the probe station with a 7 mm thick Rohacell foam to prevent short circuits (see Fig. 11). Another function of the foam was to provide nearly identical dielectric properties at both sides as the relative permittivity of Rohacell foam is close to the relative permittivity of dry air.

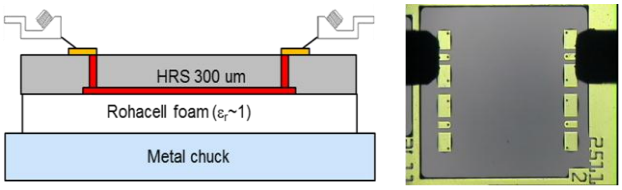


Fig. 11. Schematic picture of the on-wafer measurement setup (left) and a optical top view of the microstrip transmission lines with TSVs on the RF ground pads through the 300 µm thick silicon substrate.

Fig. 12 shows the measured S-parameters of five 2350 µm long coplanar transmission lines with two TSV transitions (one from front side to backside, and another back to front) through the silicon wafer.

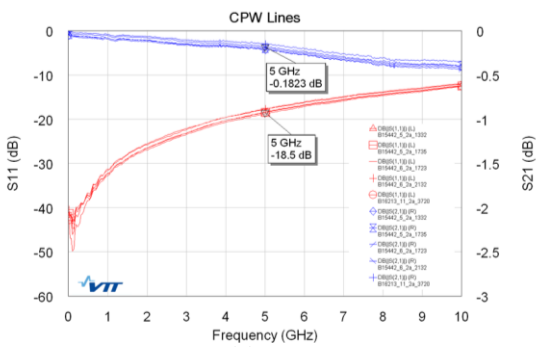


Fig. 12. Measured S11 and S21 of five identical coplanar transmission lines with TSV transitions through the 300 µm thick silicon substrate.

The measurements show total loss (loss contributions both from the CPW line and TSVs) less than 0.2 dB up to 5 GHz (equals to 0.8 dB/cm @ 5 GHz) while the matching is better than 18 dB.

In addition to the coplanar transmission line test structures microstrip transmission lines with a similar length but without TSVs on the signal line were fabricated as well as for a reference line. The schematic view of the measurement set-up and photograph of the component are shown in Fig. 13.

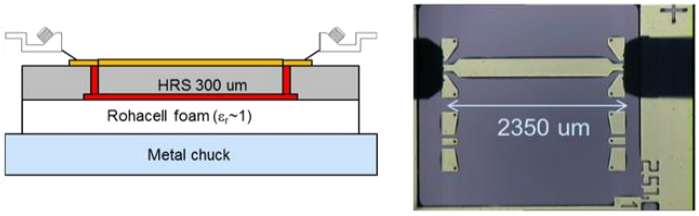


Fig. 13. Schematic picture of the on-wafer measurement setup (left) and a optical top view of the CPW line (right).

The measured loss in the case of microstrip lines was less than 0.12 dB up to 5 GHz (equals to 0.5 dB/cm @ 5 GHz) while the matching remained better than 26 dB (see Fig. 14).

In theory, both the coplanar and microstrip transmission lines should have approximately same kind of loss performance per unit length (0.5 dB/cm @ 5 GHz) with the dimensions and parameters as in this exact case. If it is assumed that higher losses of CPW lines are purely coming from the TSV transitions, it can be concluded that the loss of a single coplanar TSV transition is less than 0.04 dB @ 5 GHz. This is as stated by Chen *et. al.* [6] is to be considered to be very small. Chen *et. al.* used 5:1 AR completely filled Cu TSV with approximately 300 µm thickness, with a TSV loss of 0.04 dB at 2.5 GHz.

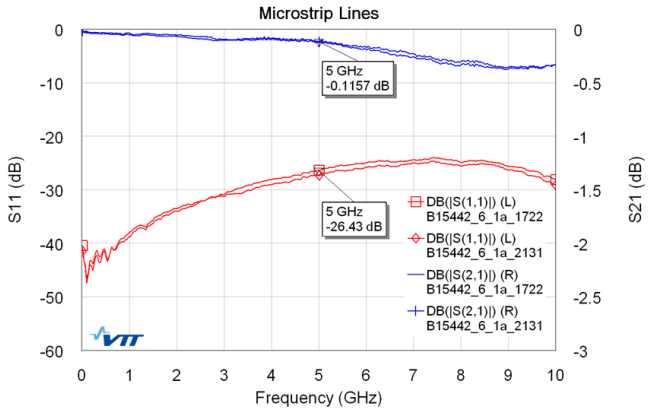


Fig. 14. Measured S11 and S21 of two identical microstrip transmission lines with TSVs on the RF ground pads through the 300 µm thick silicon substrate.

C. RF Characterization of 3D Inductor demonstrator by TNO

The 3D coil structures, as shown in Fig. 15 and Fig. 16 have been measured for small signal RF properties at TNO. The test wafers contained 3D coils with one to eight windings and thru-reflect-line (TRL) calibration structures.

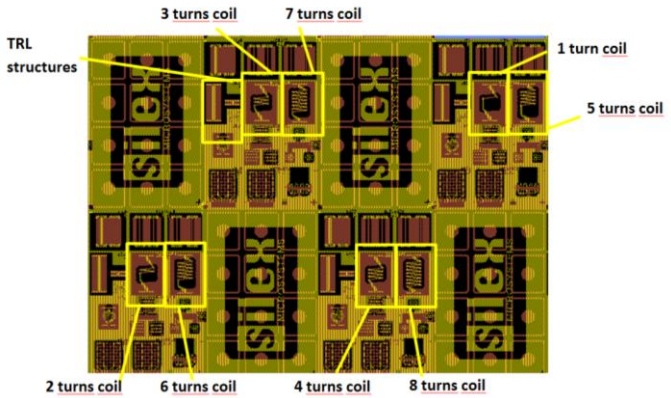


Fig. 15. Top-view of the wafer unit-cell. With inductors having 1 to 8 windings.

Coil structures originating from three different wafers have been measured. Because the metallization for the coil is present on both wafer surfaces the wafer has been placed on an insulating glass wafer for support during RF characterization. Measurement of the small signal S-parameters have been performed over frequency (10 MHz - 12 GHz) and temperature (25, 53, 81, 111°C). The temperature has been measured with a probe on the top of the glass wafer. The measurements have been done with an Agilent network analyser and a semi-automatic SUSS wafer prober.

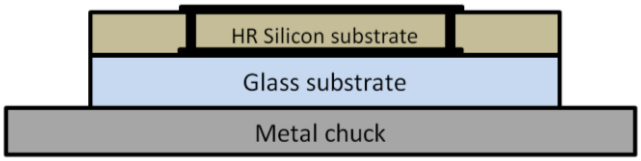


Fig. 16. Measurement setup for Inductor characterization insulating the devive wafer to wafer probe chuck using a temporary bonded glass carrier.

Using the TRL calibration structures the probes and probe pads can be subtracted from the measurements. Furthermore, an additional de-embedding of the input/output microstrip feeding lines, whose response has been previously determined through EM simulations, has been performed. The reference plane for the de-embedded coils is just before the area where the coil is located, as shown in Fig. 17.

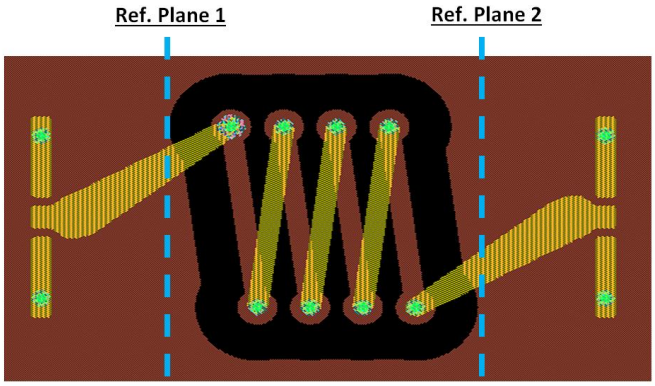


Fig. 17. 4-turns coil layout and reference planes.

The 2-port and 1-port (port 2 closed on a short circuit) Q-factor has been calculated at 1 GHz directly through the measured Y-parameters obtained from the measured data, using the following expressions:

$$Q_{2\text{-port}} = -\mathrm{Im}\{Y_{12}\}/\mathrm{Re}\{Y_{12}\} \quad (1)$$

$$Q_{1\text{-port}} = -\mathrm{Im}\{Y_{11}\}/\mathrm{Re}\{Y_{11}\} \quad (2)$$

The behavior of the Q-factor respect to the number of turns for the 2-port and 1-port at room temperature is highlighted in Fig. 18.

The inductance value for the structures has been determined form a fit of a parallel L-C model, with resistive loss in the L section, to the series branch of a pi-model of the measurement data. The series and two parallel branches were obtained by direct calculation form the Y-parameters. The values of the inductance, 2-port and 1-port Q-factor at 1 GHz and self-resonance frequencies with respect to the number of turns are listed in Table II for measurements at four different temperatures.

TABLE II. EXTRACTED INDUCTANCE, Q-FACTOR AND SELF-RESONANCE FREQUENCY AS FUNCTION OF OPERATIONG TEMPERATURE

No. turns	Temp. [°C]	L [nH]	$Q_{2\text{-port}}$	$Q_{1\text{-port}}$	SRF [GHz]
1	25 53 81 111	1.38 1.38 1.39 1.66	134 65 52 14	112 58 48 14	>10 GHz
2	25 53 81 111	2.50 2.50 2.52 2.74	59 47 42 31	50 58 48 14	>10 GHz
3	25 53 81 111	3.76 3.77 3.78 3.94	53 47 43 32	42 38 36 25	>10 GHz
4	25 53 81 111	5:13 5.15 5.16 5.22	51 56 43 31	37 34 33 23	>10 GHz
5	25 53 81 111	6.99 7.03 7.03 7.27	33 32 31 26	21 21 22 16	8.61 8.66 8.66 8.76
6	25 53 81 111	8.38 8.39 8.38 9.00	34 32 32 24	22 21 21 15	7.41 7.16 7.16 7.06
7	25 53 81 111	9.57 9.58 9.58 9.82	35 33 33 27	21 20 20 14	6.51 6.56 6.56 6.46
8	25 53 81 111	11.47 11.53 11.53 11.91	36 34 34 30	19 18 18 14	5.91 5.86 5.86 5.76

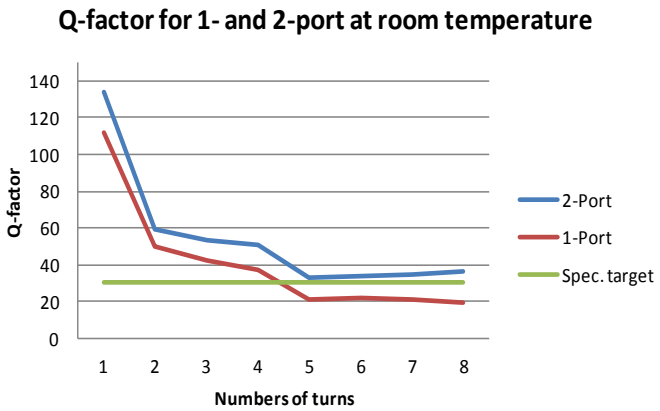


Fig. 18. 1- and 2-port Q-factor values obtained measured at room temperature.

The decrease in Q-factor for elevated temperatures is attributed to the increase in substrate loss. The silicon used as substrate is high resistivity MCZ silicon. At higher temperature the resistivity seems to decrease. With unchanged inductance and capacitance values this leads to a lower Q-factor. The effect is most pronounced above 100° C.

Five to eight different inductors of each turns design (i.e. the unit cell shown in Fig. 15) equally distributed over each wafer have been measured on three different test wafers mounted on glass carrier. Small variations <5% (1 sigma) in extracted Q-value were observed. Designs fulfilling the entire 1-12 nH spec for the EPAMO project have been obtained and for all designs with less than four turns, Q-values above 30 were obtained over the entire tested temperature interval from room temperature to 111°C. All measured Inductors with less than five turns show self resonance (SRF) above 10 GHz.

IV. OUTLOOK FOR FUTURE RESEARCH AND COMMERCIALIZTION

Within the EPAMO project on-going activities at Silex concern process integration of High Resistivity p-Si films as well as Silex PZT films [9] for high density MIM capacitors together with the TSV process described in this paper. This process integration will enable cost-effective small silicon area IDP structures that could be used for applications such as RF matching circuitry and DC-DC power converter blocks.

To further improve the performance of the demonstrated 3D Inductors, integration of magnetic materials can significantly increase inductance while keeping similar Q-factor as shown by Gardner [10] up to several hundreds of MHz. Finding magnetic materials to have both high permeability and resistivity at high frequencies of above 1 GHz is difficult due to eddy currents generated in the thin magnetic films. Being able to integrate such magnetic materials could drastically reduce the Inductor size to some single or few turns and still keep Q-values above 30. Further research on RF magnetic flux materials are therefore in progress and new approaches on how to integrate such magnetic and piezoelectric materials with the TSV process are also being researched by Silex.

The development of commercially viable rigid TSV interposers allows 2.5D integration work to be pursued without the need for a 3rd layer of organic substrate in the integrated package. The packaging engineering challenges of thermal and signal integrity design increase disproportionately with the number of layers in the package; therefore an alternative for 2.5D packaging which eliminates a functional layer of the package stack configuration has been a key goal of the current work.

We believe that this work represents the first viable 2-stack 2.5D interposer solution suitable for RF applications which has been proven to be commercially viable on an existing production line. In the coming months, Silex will be promoting this technology in the following areas:

- As alternatives to RF interposers on LTCC
- As RF capping wafers for RF MEMS and CMOS devices
- As fully integrated IPD devices, either as standalone IPD structures or as "functional interposers" combining the interposer and IPD functions

V. CONCLUSIONS

A new open TSV fabrication process with 90 µm and 50 µm diameter Via partly filled Via holes has been demonstrated using rigid 305 µm thick 200 mm diameter High Resistivity Silicon substrates. The open Via structure and locking X-shaped tapered Via hole profile together with low-cost double sided Cu plating for void free TSV filling and RDL in a simultaneous step allows for low fabrication costs. Further the "seamless" double sided plating process gives very low DC resistance due to the homogenous Cu plating characteristic of this process design. Different seedlayer deposition techniques have been evaluated and the best results were obtained with uniform MOCVD Cu layer with a minimum thickness of 40 nm inside smallest part of the Via structure.

The rigid TSV wafer approach also allows integration of other passive functions into the substrate, such as Capacitors and Resistors, which make possible highly functional IPD blocks to be manufactured either as standalone structures or integrated into an interposer design.

The fabricated RF Via test structures with coplanar transmission lines were characterized with RF measurements up to 10 GHz. Results show very low losses, less than **0.04 dB per coplanar TSV at 5 GHz frequency**, which is comparable to the results achieved also by other groups [6].

3D integrated coils using a silicon through wafer Via process have showed quality factors above 30 for inductance values up to 5 nH. The self-resonance frequency of these coils above 10 GHz which makes them suited for use in multi-band adaptive tuner matching networks for mobile technology. The rigid TSV approach used has the advantage of good scaling properties and simplified package design in 2.5D interposer applications. The performance of the inductors tested show great promise as IPD structures for both RF and power SOC applications.

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REFERENCES

[1] T. Metzger "Tunable Antenna Systems for Mobile Phones Based on Piezo MEMS", at 3rd Int piezo-MEMS Workshop, in Washington DC April 9th, 2013. Available from: http://www.epamo.eu

[2] X. Mi and S Ueda (2010), "Integrated Passives for High-Freuqncy Applications" in Advanced Microwave Microwave Circuits and Systems, V Zhurbenko (ed.), pp. 249-285.

[3] J. M. Lopez-Villegas, J. Samitier, C. Canè, P. Losantos and J. Bausells, "Improvement of the Quality Factor of RF Integraterd Inductors by Layout Optimization," IEEE Trans. On Microwave Theory and Tech., vol. 48, no.1, Jan 2000.

[4] F. Mernyei, F. Darrer, M. Pardoen and A. Sibrai, "Reducing the Substrate Losses of RF Integrated Inductors," IEEE Microwave and Guided Wave Letters, vol. 8, no. 9, Sept. 1998.

[5] D. H. Weon, J. H. Jeon, J. I. Kim, S. Mohammadi and L. P. B. Katehi, "High-Q Integrated 3D Inductors and Transformers for High Frequency Applications", Proc. Int. Symp. Microwave Theory and Tech., 2004.

[6] B. Chen, V. N. Sekhar, C. Jin, Y. Y. Lim, J. S. Toh, S. Fernando and J. Sharma, "Low-Loss Broadband Package Platform With Surface Passivation and TSV for Wafer-Level Packaging of RF_MEMS Devices", IEEE Trans. On Components, Packaging and Manufacturing Technology Volume:PP (2013), .pp - .

[7] H. T. Soh, C. P. Yue, A. McCarthy, C. Ryu, T. H. Lee, S. S. Wong and C. F. Quate, "Ultra-Low Resistance, Through-Wafer Via (TWV) Technology and Its Applications in Three Dimensional Structures on Silicon," Jpn. J. Appl. Phys. Vol. 38 (1999), pp. 2393-2396.

[8] S.Moulodi, J. Fredlund, T. Ebefors , "Development of New Metallization Processes for High Aspect Ratio Through-Silicon-Via (TSV)", presented at MME conference, Finland, Sept 1-4, 2013.

[9] T. Ebefors et. al., "Successful Experiences from Integration and Compatibility program of New Piezoelectric Materials in a MEMS Foundry Production Line" ", at 3rd Int piezo-MEMS Workshop, in Washington DC April 9th, 2013.

[10] D. S. Gardner et. al., "Intergrated On-Chip With Magnetic Films", IEEE Transaction on Magnetics, Vol. 43, No. 6, June 2007, pp. 2615-2617.

[11] T. Ebefors et. al., "Recent Results Using Met-Via® TSV Interposer Technology as TMV Element in Wafer-Level Through Mold Via Packaging of CMOS Biosensors", to be presented International Wafer-Level Packaging Conference IWLPC, November 5-7, 2013 San Jose, CA.