

## White Paper

# Innovative RF-SOI Wafers for Wireless Applications



### Abstract

The increasing demand for wireless data bandwidth and the emergence of LTE and LTE Advanced standards pushes radio-frequency (RF) IC designers to develop devices with higher levels of integrated RF functions, meeting more and more stringent specification levels. The substrates on which those devices are manufactured play a major role in achieving that level of performance.

This paper explains the value of using RF-SOI substrates and what the latest generation of Soitec Wave SOI™ (Soitec eSI™) brings to RF IC performance while simplifying the IC manufacturing process in order to address the mainstream smart phone market.



## Introduction

We are living through a mobile revolution that is providing huge growth opportunity for the semiconductor industry. With this opportunity come two major challenges for producers of RF devices:

- Support data transfer rates of one gigabit per second (Gbps) and higher by complying with increasingly complex communication standards such as LTE, LTE Advanced, 802.11.ac and others over a wider frequency spectrum
- Support the market for entry-level smart phones, which enjoys the fastest growth by providing innovative, power-efficient, compact and cost-effective solutions

RF-engineering substrates are playing a major role in the growth of the front-end module market, which today represents more than US\$6 billion in annual business. Diverging from the historical mainstream usage of GaAs wafers, high-resistivity silicon-on-insulator (HR-SOI) has emerged as today's substrate of choice. HR-SOI wafers produced with Soitec's Smart Cut™ technology on a high-resistivity base are used in the majority of smart phones, making them the mainstream engineering substrates for switches. In addition, HR-SOI is emerging as the preferred solution for on-chip integration of advanced multi-mode, multi-band power amplifiers with switches.

A key benefit of HR-SOI wafers is that these high-linearity substrates with built-in isolation are compatible with CMOS processing, allowing integration of complex high-power, mixed-signal system-on-chip devices.

To address the different communication standards and functions used in front-end modules, Soitec, the leader in SOI technology, has developed two flavors of SOI products – HR-SOI and Enhanced Signal Integrity™ (eSI) SOI – both of which are compatible with standard CMOS processes. While standard HR-SOI is capable of meeting 2G or 3G requirements, advanced eSI SOI achieves much higher linearity and isolation, allowing designers to address some of the most stringent LTE requirements. This paves the way for integrating more functions on a device with better RF performance at competitive cost.

## The mobile revolution: The new semiconductor industry driver

A major transition from PCs to mobile computing is underway. By 2015, unit shipments of laptops, tablets and smart phones will be eight times higher than they were 10 years ago (Source: KPCB, Kleiner Perkins Caufield & Byers, 9/12 – Ref [1]) with smart phones and tablets representing 1.6 billion units or approximately 80 percent of all mobile computing devices.

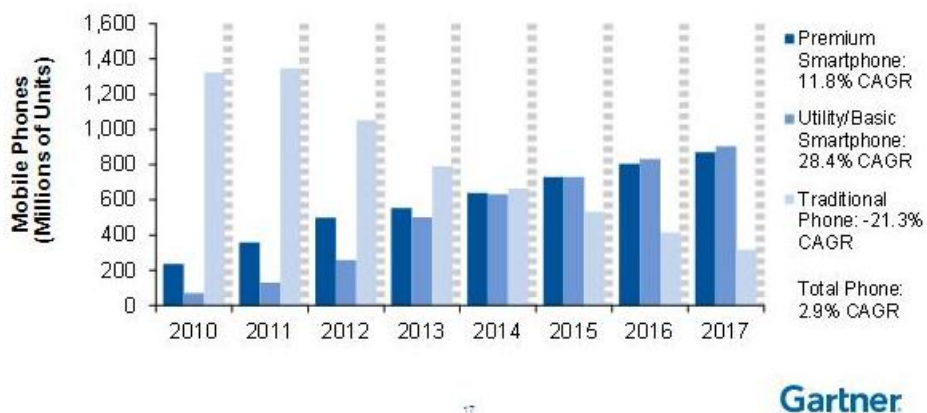
Growing usage of multimedia applications associated with consumers' desire for ultimate mobility experience has created significant market changes:

- More mobile devices: The number of smart phones will grow at a compound annual growth rate (CAGR) of 14 percent between 2013 and 2017 (Source: IDC - Ref [2]).

- More mobile users: The number of mobile connections worldwide is over six billion, and will surpass the world population by the end of 2013 (Source: World Bank – Ref [3]).
- More multimedia applications: More and more applications are being run on mobile phones including video streaming, TV, social media and content sharing. This has led Qualcomm to predict that data traffic will grow by a factor of 1,000 between 2010 and 2020 (Ref [4]).
- Faster mobile throughput: With data consumption increasing, more advanced technologies – such as LTE, LTE Advanced, Wi-Fi 802.11.ac and beyond – are needed to offer higher data rates of 1 Gbps and greater on wireless networks. These new standards are emerging already.

The semiconductor industry will benefit from this mobile revolution on several fronts:

- Increased smart phone unit sales: Smart phones represent the major growth segment for the coming years with more and more semiconductor content (Figure 1 – Ref [5]).



**Figure 1: Premium and utility smart phone growth**

- Increased semiconductor complexity and content: For example, moving from 3G to LTE Advanced typically means an increase from four 3G bands to 26 LTE bands. Considering that all front-end module functions are done in silicon, the equivalent silicon area for RF front-end modules will be multiplied by a factor of three.

## RF front-end module market challenges

The advent of more advanced standards requires more frequency bands to achieve the needed throughput. At the front-end module level, this will translate into multiple changes for each main function (Figure 2):

- A proliferation of switches on top of the antenna switch including diversity, power-mode and antenna-swapping switches

- Advanced, tunable power-amplifier architectures to achieve compact and cost-effective multi-mode, multi-band transmission in a single broadband power amplifier
- Advanced power management: with an envelope-tracking system approach, the efficiency of broadband power amplifiers will be close to or as good as that of single-band power amplifiers
- Advanced wide-band antenna: with an antenna-tuner system making either impedance matching and/or aperture tuning, an antenna can efficiently cover bands with frequencies from 700 MHz to 3.5 GHz with optimum efficiency and a smaller footprint

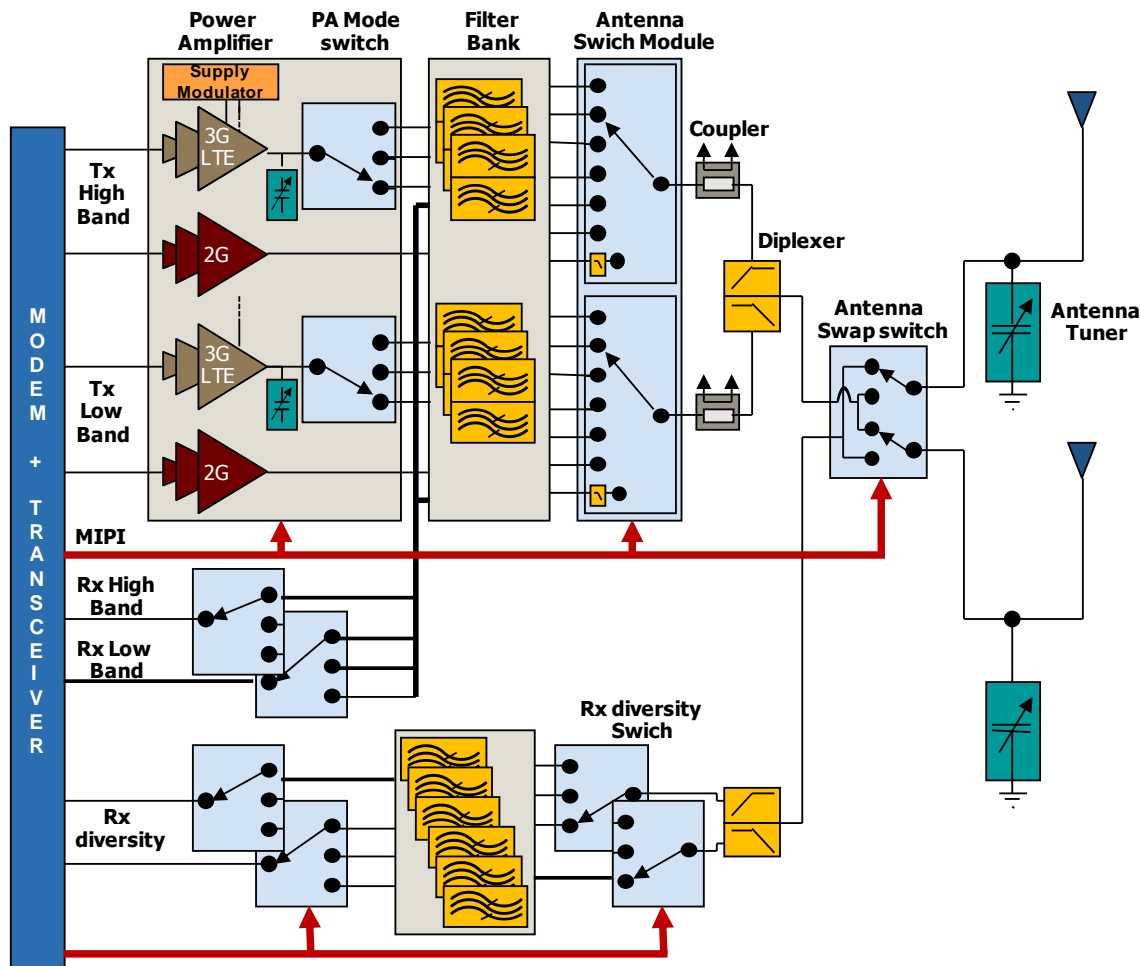


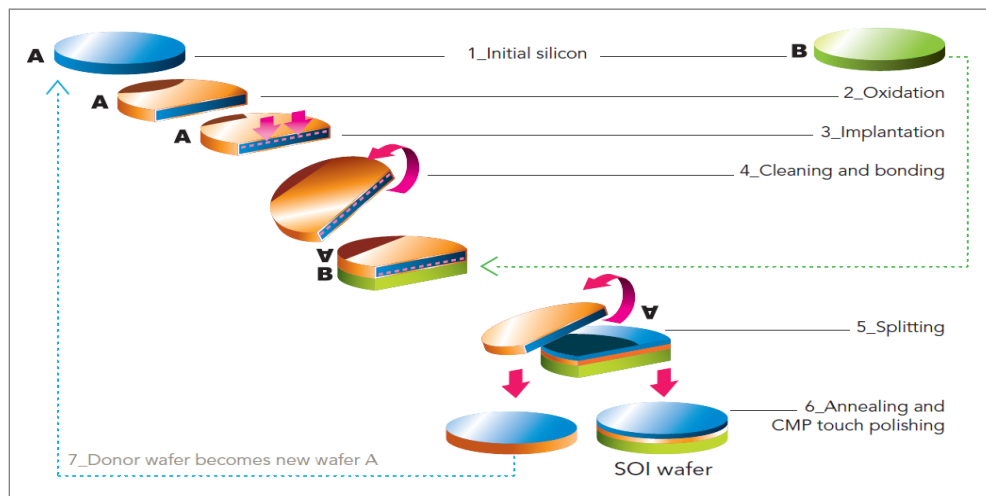
Figure 2: Front-end module block diagram for LTE

To meet the required performance, many changes are happening at all levels including systems, architectures, processes and devices as well as technologies down to the engineered substrate. These substrates on which devices are manufactured have a significant impact on the level of performance that the final devices will be capable of achieving (Ref [6]).

Historically, switches and power amplifiers were built on GaAs substrates. In the past three years, the industry has seen widespread adoption of new types of substrates such as silicon-on-sapphire (SoS) and silicon on insulated, high-resistive substrates (HR-SOI), enabling higher performance at reduced system cost and footprint.

## The emergence of SOI for RF devices

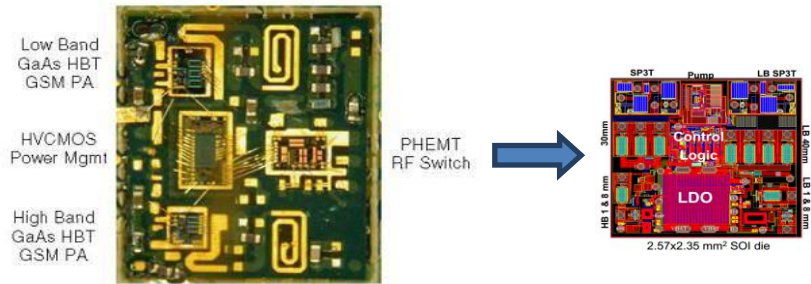
The majority of SOI-based RF devices employ Soitec’s Smart Cut™ technology (Figure 3) either directly or through licensing to third parties.



**Figure 3: Smart Cut™ technology process outline**

Traditionally, SOI wafers use bulk silicon as base wafers. For RF applications, the buried oxide is not thick enough to prevent the electrical field from diffusing into the substrate, inducing high-frequency signal losses, non-linearity and crosstalk.

To improve the insertion loss, harmonic distortion and isolation performance required for switches, bulk silicon is replaced by a high-resistivity base substrate, typically specified to be above 1 KOhm.cm. The adoption of HR-SOI wafers for RF applications has allowed monolithic integration of RF front-end modules, leading to smaller size, better reliability, improved performance and lower system cost (Figure 4 and Figure 5) (Ref [7], Ref[8]).



Source: RFMD, A Tombak, 2009

Figure 4: From a 12 cm<sup>2</sup> module to a 6 mm<sup>2</sup> module

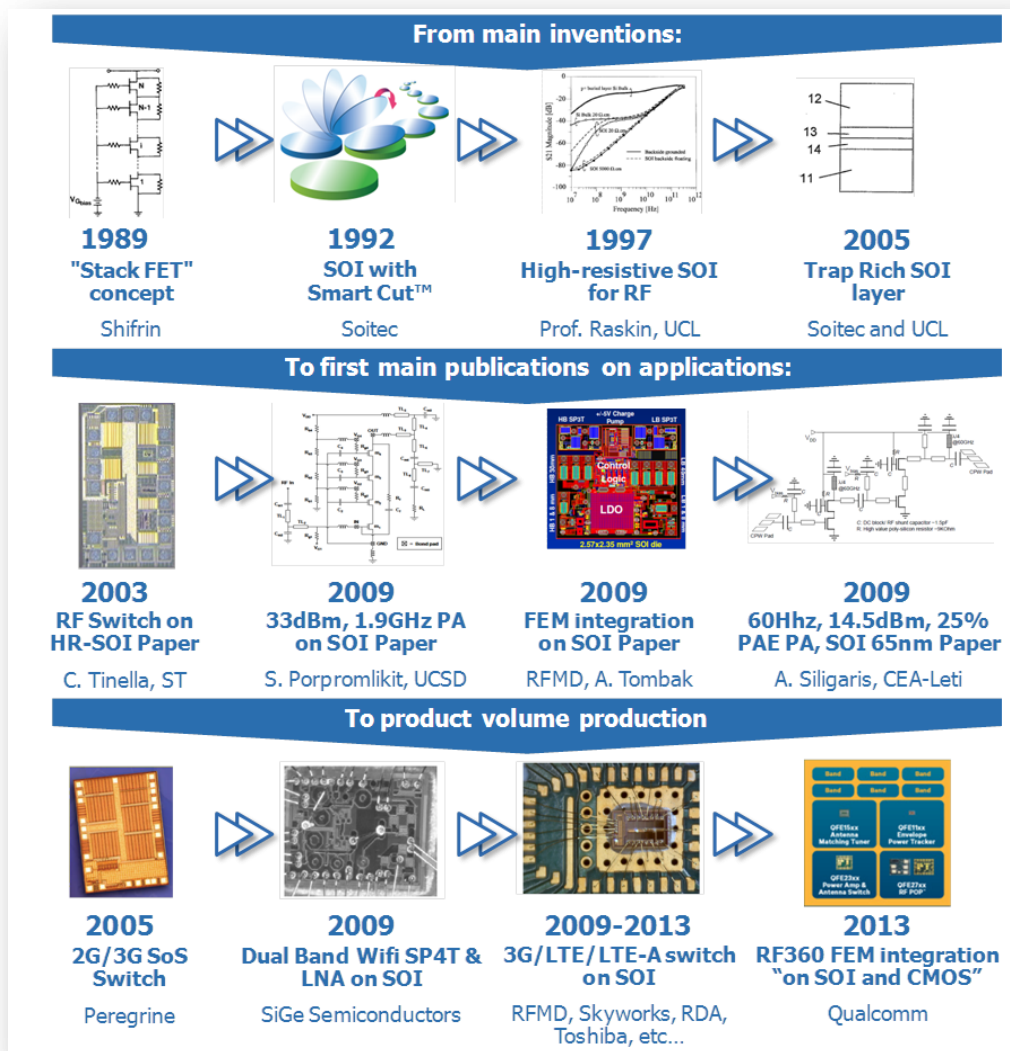
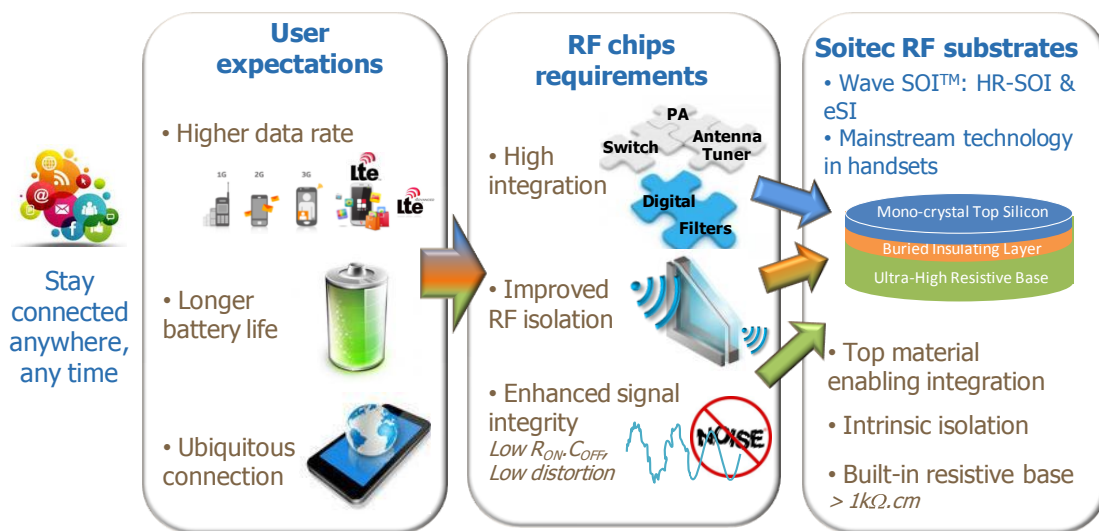


Figure 5: A brief history of RF-SOI adoption

Because RF-SOI wafers enable the device integration, cost effectiveness and high performance needed for high-volume 3G and LTE applications, their adoption in RF switches for handsets is over 65 percent (Source: Yole Développement). In addition, the first RF-SOI power amplifiers and integrated front-end modules are being well received and gaining momentum in the market. Based on current levels of adoption and performance, increasing use of RF-SOI wafers for integrated front-end modules is expected to follow the same adoption rate as seen with switches.

## Addressing the next RF standards and integration steps

The substrate's properties allow RF designers to integrate diverse functions such as switches, power amplifiers and antenna tuners while providing excellent RF isolation, good insertion loss and better signal integrity at lower cost than traditional technologies (Figure 6).



**Figure 6: RF-SOI benefits**

Soitec offers two flavors of its Wave SOI™ substrates:

- Soitec HR-SOI product line using a standard high-resistivity base substrate
- Soitec eSI product line using an engineered high-resistivity base substrate

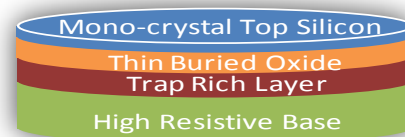
## Soitec HR-SOI substrate

Soitec’s HR-SOI product line employs a standard high-resistivity base. Compared to standard SOI, HR-SOI dramatically reduces both resistivity losses and crosstalk and has been adopted to integrate switches for 2G and 3G applications. While HR-SOI substrates are well suited for these applications, the need for higher linearity and increased integration requires a step-up in substrate capabilities.

Due to remaining charge in the buried oxide, a low-ohmic conductive layer below the buried oxide is induced, degrading the overall RF engineering substrates’ performances [Ref 9]. To reach the next step in performance and to address 4G requirements, it is imperative to limit the parasitic surface conduction. Various lithography techniques can be applied to achieve better results, although they will impact process complexity and impose performance and design tradeoffs.

## Soitec eSI substrate

Working together, Soitec and Université catholique de Louvain (UCL) developed a technique to freeze the parasitic surface conduction by adding a trap-rich layer underneath the buried oxide (Figure 7). Using a set of very specific patents, Soitec applies its proprietary technology and accumulated knowledge to build the eSI product line.



**Figure 7: Soitec Wave SOI eSI wafer**

Because this layer is built at the substrate level, expensive process steps such as high-energy implant and conservative design rules are not required on eSI wafers, leading to a cheaper process and a possible smaller die area per function.

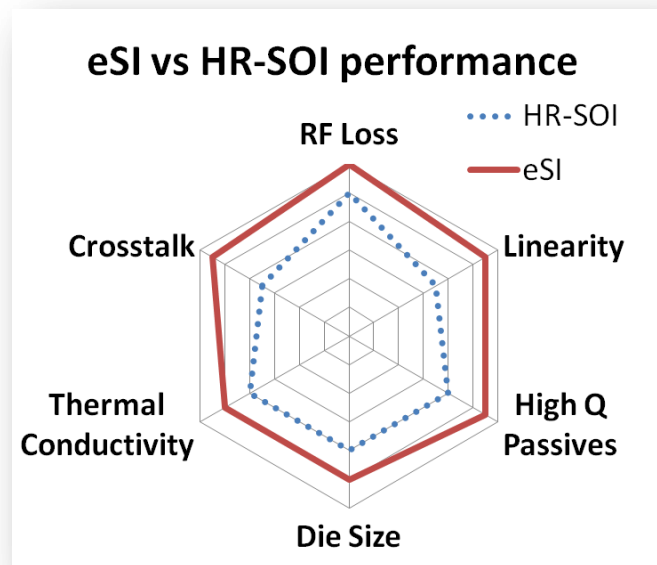
The substrate allows RF designers to integrate on the same chip diverse functions such as switches, power amplifiers and antenna tuners with excellent RF isolation, good insertion loss and better signal integrity than traditional technologies.

As illustrated in figure 8, eSI surpasses HR-SOI by providing some major performance advances that enable full front-end module integration:

- RF losses
  - Improved RF losses by maintaining constant substrate resistivity from DC to RF spectrum; eSI substrates behave like quasi-loss-less substrates with performance comparable to GaAs and sapphire types of substrates showing less than 0.15 dB/mm at 2 GHz
- Linearity
  - Improved second harmonic (H2) by more than 20 dB, enabling devices to meet or surpass IMD (inter-modulation distortion) switch specifications



- High Q passives
  - Improved inductors quality factor (up to two times higher Q factor for 2nH inductance at 2 GHz) , enabling high-performance matching networks for tuners, couplers and active circuits such as degenerated low-noise amplifiers and multi-mode, multi-band power amplifiers
- Die size
  - Improved transistor matching since eSI layers make transistors “independent” from the substrate electrostatic; this is very beneficial when a high transistor stack is required for handling voltages beyond 40 V
  - The built-in isolation under the buried oxide simplifies design rules and the requirement to use wide trenches between the transistors, thus leaving room for saving die area
- Thermal conductivity
  - Improved thermal conductivity: although the fact that SOI could present a “thermal roadblock” previously limited its application in power amplifiers, Soitec has demonstrated that RF performance is not degraded by thinning the buried oxide in eSI wafers and, in fact, that using thinner buried oxide provides even wider design margins for existing power-amplifier solutions
- Crosstalk
  - Improved crosstalk, typically by 20 dB at 1 GHz; this gives designers of increasingly complex mixed-signal system-on-chip devices more freedom in chip layout partitioning, enabling better performance and avoiding multiple re-spin
  - Because the eSI layer is below the full buried-oxide surface, metal layer coupling with the substrate is the same whether it runs above an active device or not

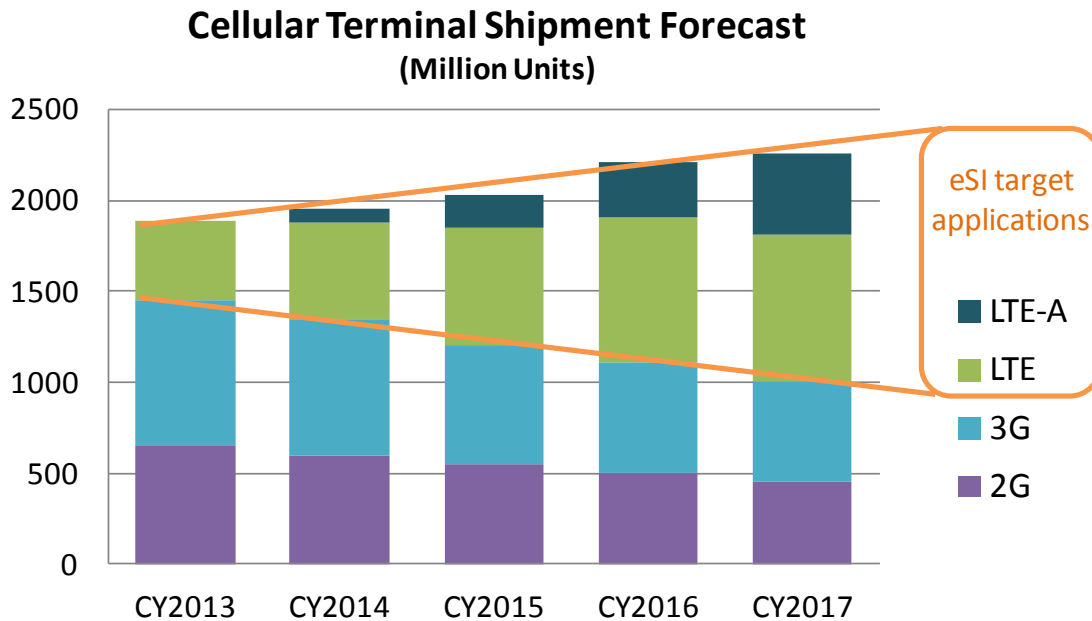


**Figure 8: eSI vs. HR-SOI performance**

Another major innovation with eSI products comes from the ability to predict the RF harmonic distortion performance of the substrate immediately after the eSI substrates are fabricated and before any devices are manufactured on them. This guarantee is provided through the harmonic quality factor (HQF) specification.

As a solution addressing the next generation of RF standards (Figure 9) and integration steps, eSI wafers are enabling this market by meeting some of the most difficult LTE and LTE Advanced linearity specifications. These wafers further open the path to power-device integration on SOI through better thermal conductivity as well as streamline complex system-on-chip integration by improving all critical electrical parameters.

Soitec’s eSI products are now in full production and have been adopted as a preferred substrate for functions requiring high-linearity performance and cost effectiveness.



*Source: Soitec based on Navian RF devices/modules for cellular, Nov 2013.*

**Figure 9: Target market for Soitec eSI products**

## Conclusion

The mobile revolution is in full swing, putting pressure on smart phone and device manufacturers to support increased demand for data traffic. This requires the contributions of all players along the value chain, including substrate manufacturers. SOI substrates are now playing a major role in RF applications and Soitec, with its innovative eSI substrates, enables the cost-effective integration of more and more functions as well as better RF performance to address the mainstream smart phone market.

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## References

- [1] KPCB, Kleiner Perkins Caufield & Byers: 2012 Internet Trends (Update)  
<http://www.kpcb.com/insights/2012-internet-trends-update>
- [2] IDC: Worldwide Mobile Phone Market Forecast to Grow 7.3% in 2013 Driven by 1 Billion Smartphone Shipments, According to IDC – Sept 2013  
<http://www.idc.com/getdoc.jsp?containerId=prUS24302813>
- [3] World Bank: Mobile Phone Access Reaches Three Quarters of Planet's Population – July 2012  
<http://www.worldbank.org/en/news/press-release/2012/07/17/mobile-phone-access-reaches-three-quarters-planets-population>
- [4] Qualcomm: 1000x Mobile Data Challenge – November 2013  
<http://www.qualcomm.com/media/documents/web1000x-mobile-data-challenge>
- [5] Gartner: Worldwide Mobile Phone Production & Semiconductor TAM Forecast Analysis
- [6] RFMD Ali Tombak - Devices and Design Techniques for Advanced Handset / Mobile PAs - RFIC 2009 – Boston, June 7 - 12, 2009  
[http://www.rfmd.com/cs/documents/COMMali\\_TombakRFIC.pdf](http://www.rfmd.com/cs/documents/COMMali_TombakRFIC.pdf)
- [7] Yole Développement: RF Filters, PAs, Antenna Switches & Tunability for Cellular Handsets
- [8] J.-P. Raskin, A. Viviani, D. Flandre and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology", IEEE Transactions on Electron Devices, vol. 44, no. 12, pp. 2252-2261, December 1997
- [9] D. Lederer and J.-P. Raskin, "Effective resistivity of fully processed SOI substrates", Solid-State Electronics, no. 49, pp. 491-496, 2005
- [10] K. Ben Ali, C. Roda Neve, A. Gharsallah and J.-P. Raskin, "RF SOI CMOS technology on commercial trap-rich high-resistivity SOI wafer", IEEE International SOI Conference – SOI'12, Napa, CA, USA, October 1-4, 2012, pp. 112-113
- [11] C. Roda Neve, J.-P. Raskin and E. Desbonnets, "Engineering substrate paths for RF front end module integration - Focus on trap rich high resistivity silicon-on-insulator", (invited paper), The 42nd European Solid-State Device Research Conference – ESSDERC 2012, SINANO-NanoFunction Workshop - Novel materials, devices and technologies for high performance on-chip RF applications, Bordeaux, France, September 17-21, 2012
- [12] Soitec: RF Substrate Technologies for Mobile Communications – Eric Desbonnet, Stephane Laurent -  
[http://www.soitec.com/pdf/RF\\_SubstratesTechnologies\\_2011-07-07.pdf](http://www.soitec.com/pdf/RF_SubstratesTechnologies_2011-07-07.pdf)