

Tankeblue

Silicon Carbide Substrates

(Version:2019)

Product Specifications

4H N-Type

6H N-Type

4H Semi-insulating

6H Semi-insulating

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Contact: Wang Bo

Tel: +86-10-61256850 ext 629

Cell phone: +86-18515302530

E-mail: TKHD-Sales@tankeblue.com

wangbo@tankeblue.com

Address: F3, ShiNong Building, No.9 TianRong Street, Daxing District, Beijing,
P.R.China, 102600

Web: <http://www.tankeblue.com>

SILICON CARBIDE MATERIAL PROPERTIES

Property	4H-SiC, Single Crystal	6H-SiC, Single Crystal
Lattice Parameters	a=3.076 Å c=10.053 Å	a=3.073 Å c=15.117 Å
Stacking Sequence	ABCB	ABCACB
Mohs Hardness	≈9.2	≈9.2
Density	3.21 g/cm ³	3.21 g/cm ³
Therm. Expansion Coefficient	4-5 × 10 ⁻⁶ /K	4-5 × 10 ⁻⁶ /K
Refraction Index @750nm	n _o = 2.61 n _e = 2.66	n _o = 2.60 n _e = 2.65
Dielectric Constant	c~9.66	c~9.66
Thermal Conductivity (N-type, 0.02 ohm.cm)	a~4.2 W/cm·K@298K c~3.7 W/cm·K@298K	
Thermal Conductivity (Semi-insulating)	a~4.9 W/cm·K@298K c~3.9 W/cm·K@298K	a~4.6 W/cm·K@298K c~3.2 W/cm·K@298K
Band-gap	3.23 eV	3.02 eV
Break-Down Electrical Field	3-5 × 10 ⁶ V/cm	3-5 × 10 ⁶ V/cm
Saturation Drift Velocity	2.0 × 10 ⁵ m/s	2.0 × 10 ⁵ m/s

Applications

III-V Nitride Deposition

Optoelectronic Devices

High-Power Devices

High-Temperature Devices

High-Frequency Power Devices

General Definition

WABCDE-XXX

W – Standard

A – Diameter

2 – 50.8 mm (2 inch)

3 – 76.2 mm (3 inch)

4 – 100.0 mm (4 inch)

6 – 150.0 mm (6 inch)

B – Polytype

4 – 4H

6 – 6H

C – Dopant

N – Nitrogen

S – Semi-insulating

D – Orientation

0 – On-axis

4 – 4° off axis

E – Grade

Z – Zero MPD

P – Product

D – Dummy

X – Silicon face polish

P – Optical polish

C – CMP, EPI-ready

X – Carbon face polish

L – Lapping

P – Optical polish

C – CMP, EPI-ready

X – Thickness

E – $350 \pm 25 \mu\text{m}$

F – $330 \pm 25 \mu\text{m}$

G – $500 \pm 25 \mu\text{m}$

X – Other thickness

天科合达 6 英寸 SiC 晶片产品标准
6 inch diameter, Silicon Carbide (SiC) Substrate Specification

等级 Grade		精选级 (Z 级) Zero MPD Production Grade (Z Grade)	工业级(P 级) Standard Production Grade (P Grade)	测试级 (D 级) Dummy Grade (D Grade)
直径	Diameter	150.0 mm±0.2mm		
厚度	Thickness	4H-N	350 μm±25μm	
		4H-SI	500 μm±25μm	
晶片方向	Wafer Orientation	Off axis : 4.0° toward <1120>±0.5° for 4H-N		On axis : <0001>±0.5° for 4H-SI
微管密度 Micropipe Density	4H-N	≤0.5 cm ⁻²	≤2 cm ⁻²	≤15 cm ⁻²
	4H-SI	≤1 cm ⁻²	≤5cm ⁻²	≤15 cm ⁻²
电阻率 Resistivity	4H-N	0.015~0.025 Ω·cm		0.015~0.028 Ω·cm
	4H-SI	≥1E5 Ω·cm		
主定位边方向	Primary Flat	{10-10}±5.0°		
主定位边长度 Primary Flat Length	4H-N	47.5 mm±2.0 mm		
	4H-SI	Notch		
边缘	Edge exclusion	3 mm		
总厚度变化/弯曲度/翘曲度 TTV/Bow /Warp		≤15 μm / ≤40 μm / ≤60 μm		
表面粗糙度 Roughness	Polish	Ra≤1 nm		
	CMP	Ra≤0.5 nm		
裂纹(强光灯观测) Cracks by high intensity light		None		Cumulative length ≤ 20mm, single length≤2mm
六方空洞 (强光灯观测) * Hex Plates by high intensity light		Cumulative area ≤0.05%		Cumulative area ≤0.1%
多型(强光灯观测)* Polytype Areas by high intensity light		None		Cumulative area≤3%
目测包裹物(日光灯下观测) Visual Carbon Inclusions		Cumulative area ≤0.05%		Cumulative area ≤3%
划痕(强光灯观测)# Scratches by high intensity light		None		Cumulative length≤1×wafer diameter
崩边	Edge chip	None		5 allowed, ≤1 mm each
表面污染物 (强光灯观测) Contamination by high intensity light		None		
包装 Packaging		Multi-wafer Cassette Or Single Wafer Container		

Notes:

* Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.

天科合达 4 英寸 SiC 晶片产品标准
4 inch diameter Silicon Carbide (SiC) Substrate Specification

等级 Grade		精选级 (Z 级) Zero MPD Production Grade (Z Grade)	工业级(P 级) Standard Production Grade (P Grade)	测试级 (D 级) Dummy Grade (D Grade)
直径	Diameter	99.5-100 mm		
厚度	Thickness	4H-N	350 $\mu\text{m} \pm 25\mu\text{m}$	
		4H-SI	500 $\mu\text{m} \pm 25\mu\text{m}$	
晶片方向	Wafer Orientation	Off axis : 4.0° toward $\langle 11\bar{2}0 \rangle \pm 0.5^\circ$ for 4H-N		On axis : $\langle 0001 \rangle \pm 0.5^\circ$ for 4H-SI
微管密度	Micropipe Density	4H-N	$\leq 0.5 \text{ cm}^{-2}$	$\leq 15 \text{ cm}^{-2}$
		4H-SI	$\leq 1 \text{ cm}^{-2}$	$\leq 5 \text{ cm}^{-2}$
电阻率	Resistivity	4H-N	0.015~0.025 $\Omega \cdot \text{cm}$	
		4H-SI	$\geq 1 \text{ E}7 \Omega \cdot \text{cm}$	
主定位边方向	Primary Flat	$\{10\text{-}10\} \pm 5.0^\circ$		
主定位边长度	Primary Flat Length	32.5 mm ± 2.0 mm		
次定位边长度	Secondary Flat Length	18.0mm ± 2.0 mm		
次定位边方向	Secondary Flat Orientation	Silicon face up: 90° CW. from Prime flat $\pm 5.0^\circ$		
边缘去除	Edge exclusion	2 mm		
局部厚度变化/弯曲度/翘曲度 LTV/TTV/Bow /Warp		$\leq 4\mu\text{m} / \leq 10\mu\text{m} / \leq 25\mu\text{m} / \leq 35\mu\text{m}$		$\leq 10\mu\text{m} / \leq 15\mu\text{m} / \leq 25\mu\text{m} / \leq 40\mu\text{m}$
表面粗糙度	Roughness	Polish	$R_a \leq 1 \text{ nm}$	
		CMP	$R_a \leq 0.5 \text{ nm}$	
裂纹(强光灯观测) Cracks by high intensity light		None	Cumulative length $\leq 10\text{mm}$, single length $\leq 2\text{mm}$	
六方空洞 (强光灯观测) * Hex Plates by high intensity light		Cumulative area $\leq 0.05\%$		Cumulative area $\leq 0.1\%$
多型(强光灯观测)* Polytype Areas by high intensity light		None	Cumulative area $\leq 3\%$	
目测包裹物 (日光灯观测) Visual Carbon Inclusions		Cumulative area $\leq 0.05\%$		Cumulative area $\leq 3\%$
划痕(强光灯观测)# Scratches by high intensity light		None	Cumulative length $\leq 1 \times$ wafer diameter	
崩边 Edge chip		None	5 allowed, $\leq 1 \text{ mm}$ each	
表面污染物 (强光灯观测) Contamination by high intensity light		None		
包装 Packaging		Multi-wafer Cassette Or Single Wafer Container		

Notes:

* Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.

天科合达 3 英寸 SiC 晶片产品标准
3 inch diameter Silicon Carbide (SiC) Substrate Specification

等级 Grade		工业级 Production Grade	研究级 Research Grade	试片级 Dummy Grade
直径	Diameter	76.2 mm±0.38 mm		
厚度	Thickness	350 μm±25μm		
晶片方向	Wafer Orientation	On axis : <0001>±0.5° for 4H-SI	Off axis : 4.0° toward <1120>±0.5° for 4H-N	
微管密度	Micropipe Density	≤5 cm ⁻²	≤15 cm ⁻²	≤50 cm ⁻²
电阻率	Resistivity	4H-N	0.015~0.028 Ω·cm	
		4H-SI	>1E5 Ω·cm	(90%) >1E5 Ω·cm
主定位边方向	Primary Flat	{10-10}±5.0°		
主定位边长度	Primary Flat Length	22.2 mm±3.2 mm		
次定位边长度	Secondary Flat Length	11.2 mm±1.5 mm		
次定位边方向	Secondary Flat Orientation	Silicon face up : 90° CW. from Prime flat ±5.0°		
边缘	Edge exclusion	2 mm		
总厚度变化/弯曲度/翘曲度 TTV/Bow /Warp		≤15μm /≤25μm /≤35μm		
表面粗糙度	Roughness	Polish	Ra≤1 nm	
		CMP	Ra≤0.5 nm	
裂纹(强光灯观测) Cracks by high intensity light		None	1 allowed, ≤1 mm	1 allowed, ≤2 mm
六方空洞 (强光灯观测) * Hex Plates by high intensity light		Cumulative area ≤1%	Cumulative area ≤1%	Cumulative area ≤3%
多型(强光灯观测)* Polytype Areas by high intensity light		None	Cumulative area≤2 %	Cumulative area≤5%
划痕(强光灯观测)# Scratches by high intensity light		3 scratches to 1×wafer diameter cumulative length	5 scratches to 1×wafer diameter cumulative length	8 scratches to 1×wafer diameter cumulative length
崩边	Edge chip	None	3 allowed, ≤0.5 mm each	5 allowed, ≤1 mm each
表面污染物 (强光灯观测) Contamination by high intensity light		None		

Notes:

* Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.

天科合达 2 英寸 SiC 晶片产品标准
2 inch diameter Silicon Carbide (SiC) Substrate Specification

等级 Grade		工业级 Production Grade	研究级 Research Grade	试片级 Dummy Grade
直径	Diameter	50.8 mm±0.38 mm		
厚度	Thickness	330 μm±25μm		
晶片方向	Wafer Orientation	On axis : <0001>±0.5° for 6H-N/4H-N/4H-SI/6H-SI Off axis : 4.0° toward <1120>±0.5° for 4H-N/4H-SI		
微管密度	Micropipe Density	≤5 cm ⁻²	≤15 cm ⁻²	≤50 cm ⁻²
电阻率	Resistivity	4H-N	0.015~0.028 Ω·cm	
		6H-N	0.02~0.1 Ω·cm	
		4/6H-SI	>1E5 Ω·cm	(90%) >1E5 Ω·cm
主定位边方向	Primary Flat	{10-10}±5.0°		
主定位边长度	Primary Flat Length	15.9 mm±1.7 mm		
次定位边长度	Secondary Flat Length	8.0 mm±1.7 mm		
次定位边方向	Secondary Flat Orientation	Silicon face up: 90° CW. from Prime flat ±5.0°		
边缘	Edge exclusion	1 mm		
总厚度变化/弯曲度/翘曲度 TTV/Bow /Warp		≤15μm /≤25μm /≤25μm		
表面粗糙度	Roughness	Polish	Ra≤1 nm	
		CMP	Ra≤0.5 nm	
裂纹(强光灯观测) Cracks by high intensity light		None	None	1 allowed, ≤1 mm
六方空洞(强光灯观测)* Hex Plates by high intensity light		Cumulative area≤1 %	Cumulative area≤1 %	Cumulative area≤3 %
多型(强光灯观测)* Polytype Areas by high intensity light		None	Cumulative area≤2 %	Cumulative area≤5%
划痕(强光灯观测)# Scratches by high intensity light		3 scratches to 1×wafer diameter cumulative length	5 scratches to 1×wafer diameter cumulative length	8 scratches to 1×wafer diameter cumulative length
崩边 Edge chip		None	3 allowed, ≤0.5 mm each	5 allowed, ≤1 mm each
表面污染物(强光灯观测) Contamination by high intensity light		None		

Notes:

* Defects limits apply to entire wafer surface except for the edge exclusion area.

The scratches should be checked on Si face only.