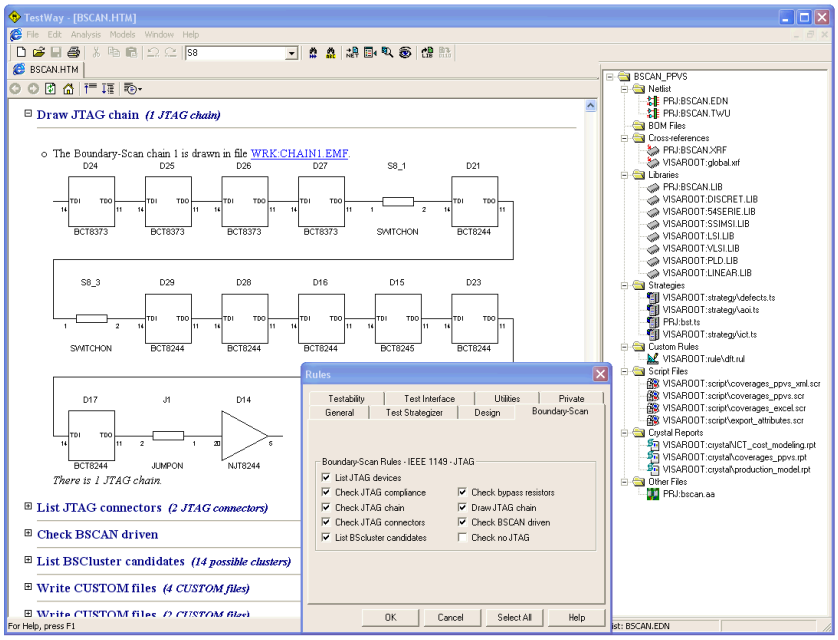
TestWay™ Board DfT & Test Coverage Analyzer



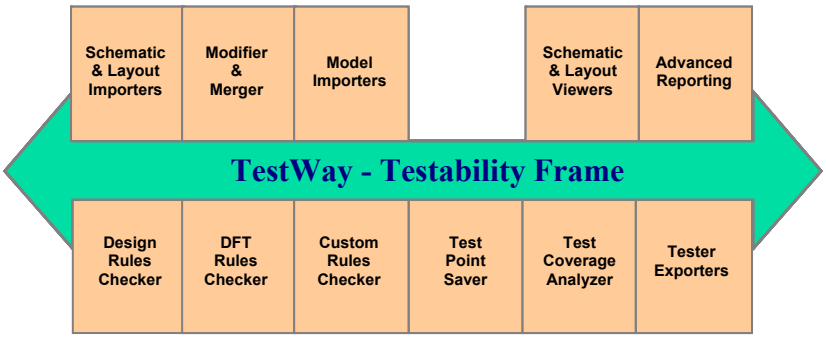
In today's electronic design and manufacturing climate, there is an increasing emphasis to shorten time-to-market, improve product quality and reduce cost. The ability to verify that PCB designs have been developed with adequate DfT (design-for-test) in mind and determine the most effective test strategies based on accurate test coverage estimations, is crucial in improving competitive advantage, lowering cost and determining the quality of a product.

TestWay's electrical DfT analyzer enables designers to validate designs at the schematic capture stage, to ensure that adequate measures have been included to comply with the manufacturers test requirements. This is particularly important when adopting a boundary-scan test strategy, where adequate DfT must be correctly implemented at the design stage.

Similarly, test engineers can use TestWay's coverage analyzer to estimate test coverage aligned to various test strategies, and identify where test coverage and testability improvements can be made. Increased cost savings and higher production yields can be achieved by improving test effectiveness in terms of test coverage.

The TestWay open architecture is based on a testability framework that interfaces to a variety of plug-in modules that provide both import and export opportunities as shown below.

TestWay reads the board level netlist (schematic or layout) and component model libraries. It then performs a basic topological analysis and symbolic simulation, and checks each rule using both topological and accessibility data.



Key product benefits:

- **Design rules checking**
  Confirm that specific design rules have been implemented prior to committing to PCB layout. Prevent costly design errors at the earliest possible opportunity.

- **DfT rules checking**
  Verify that DfT requirements are adhered to in order to maximize test coverage aligned to the PCB manufacturers test flow.

- **Test point saving**
  Identify nets not requiring physical test access; only place test points where absolutely necessary. Significantly reduce test fixturing costs due to less complex fixtures and fewer probes.

- **Test coverage estimation**
  Maximize test and inspection coverage by estimating coverage aligned to test strategy. Perform 'what-if' analysis to select optimal test strategy to achieve maximum coverage based on historical DPMO data. Eliminate redundant test steps.

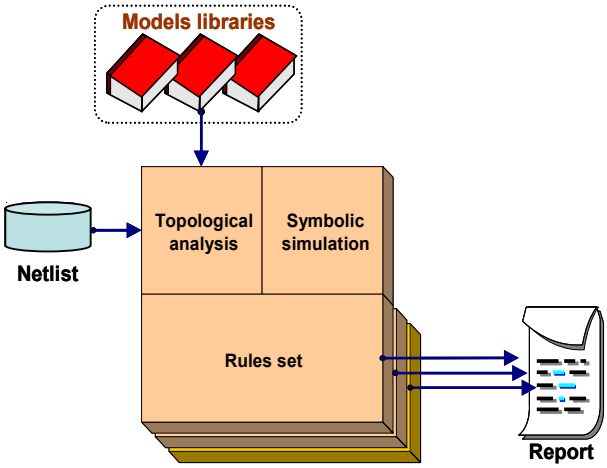
- **Test coverage measurement**
  Determine real test efficiency against theoretical coverage and identify areas for improvement.

- **Functional test coverage**
  Manage functional test as part of the overall test strategy, produce accurate coverage reports that assist with the diagnosis of faulty boards in production and repair centers.

- **Board visualization**
  Visualize test coverage and customer specific attributes in schematic, layout and netlist navigation views. Unique digitization feature creates interactive schematic view from PDF.

- **Advanced reporting**
  Produce comprehensive reports in a variety of formats that highlight production yield, test coverage by component, estimated placement time, etc.

- **Cost modeling**
  Estimate test execution times, total engineering time and calculate hardware costs such as: test fixture frame, wiring, spring probes, vector-less sensors, etc.



TestWay produces a testability report, written in a natural language that can be used by design and test engineers to validate that specific DfT criteria have been implemented.

RULES CHECKING

TestWay's electrical rules are distributed into 3 categories: Design rules, Testability rules, Boundary-scan rules. These rules are derived from formal standards and include rules commonly applied throughout the electronics industry that are complementary to the DfM and test point placement rule checking features of commercial CIM systems. Specific customer requirements can be specified in a natural language using TestWay's custom rules feature.

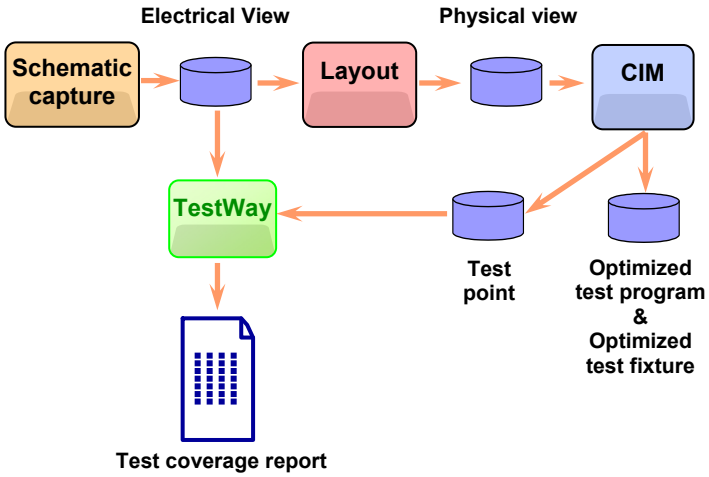
TestWay's electrical rules checking validates company specific DfT requirements in real time and are easily customized to reflect updates to testability guidelines, such as:

- Design rules to verify conformance restrictions imposed by certain technologies i.e. open-drain, bushold, specific termination requirements, noise immunity, etc.
- In-Circuit test rules for insuring initialization and test partitioning i.e. chip select, output enable, test pins, etc.
- Boundary-scan rules for verifying chain integrity, boundary-scan compliance, presence of bypass resistors, flash programming optimization, identifying boundary-scan clusters and boundary-scan bus terminations, etc.
- Custom rules to meet any specific in-house testability requirements. User may define and integrate new custom rules in real time.

TEST POINT SAVING

With the dramatic increase in device density on PCB's resulting in high net counts, it is virtually impossible to gain physical test access to each net for test purposes. In balancing different complementary test approaches, such as ICT, FPT and BST, TestWay optimizes the number of locations where physical test access is mandatory.

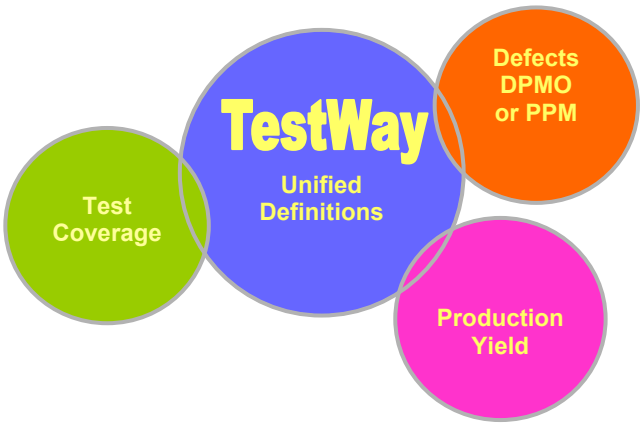
The test point optimization results can be integrated with commercial CIM layout tools to identify where physical access is required and back-annotate into the schematic design. In addition, TestWay provides physical confirmation that the requisite numbers of test points are placed once layout is completed.



COVERAGE ESTIMATION

TestWay simulates various test scenarios and test line combinations in order to estimate the global test coverage provided by a mixture of complementary test and inspection systems. This allows customers to leverage the benefits of each solution in reducing the number of test points, number of false calls and diagnostic inaccuracies, eliminating overlapping tests, resulting in a reduction of the overall test time.

TestWay sets the defect rates based on MPS (Material, Placement, Solder) criteria, provided as DPMO (Defect Per Million Opportunities) data for each component category, indicating the number of probable defects in the manufacturing process.



TestWay estimates test coverage based on selected test strategy at either the schematic or layout stages by using models provided for any type of testers (AOI, AXI, FPT, ICT, BST and FT).

The models can be easily adapted to simulate any tester options, so that customers are able to select the optimal test solution in order to achieve maximum test coverage.

Test coverage estimation is based on a combination of available physical test access and any virtual test access provided by boundary-scan cells. It is beneficial that this analysis is undertaken at the schematic capture stage so that any improvements in the ability to control and observe nodes can be implemented before committing to board layout.

Using TestWay at the earliest possible opportunity in the design cycle unlocks many potential benefits, such as:

- Higher test coverage, by identifying testability issues while designers are still able to make modifications.
- Improved test efficiency, by identifying optimal test point placement and back annotating the schematics.
- Fewer iterations during layout because test points can be assigned prior to layout.
- Lower fixture costs due to fewer test points.
- Faster time to market due to the majority of DfT issues being identified and resolved during schematic capture.

COVERAGE MEASUREMENT

By reading actual test programs or coverage reports, TestWay can control actual test coverage against theoretical coverage. A 'step-by-step' analysis of application specific test programs, determines the measurement type and the defects that can be detected.
Available coverage importers include HP3070, GR228x, Z1800, SPECTRUM, HP5DX, BST test systems, etc.

FUNCTIONAL TEST COVERAGE

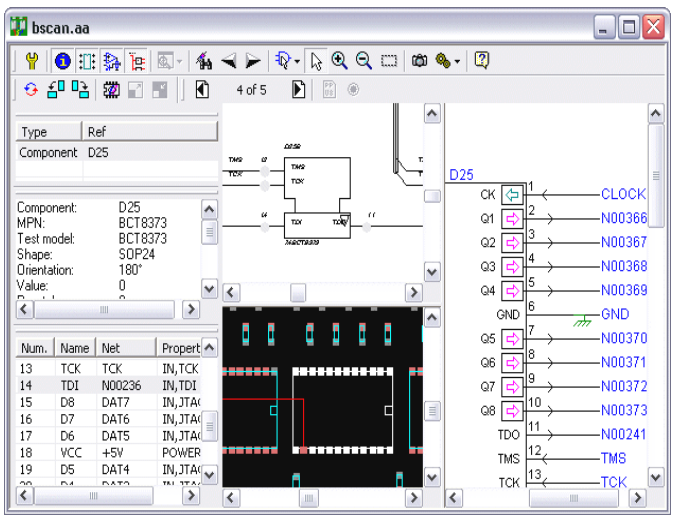
TestWay calculates functional test coverage using one of the following methodologies:

1. **Declaration:** Using schematic and/or layout viewers as test coverage input device.
2. **Deduction:** From a formal test description based on customer's rules.
3. **Inheritance:** Test reuse in a hierarchical design flow where a functional block is associated with test coverage calculations.

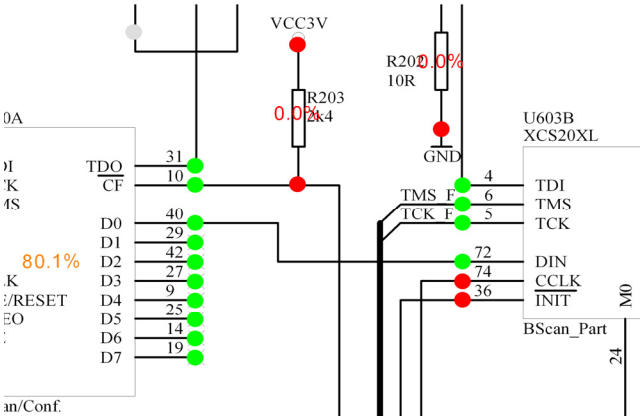
The functional test coverage report produced by TestWay, is reusable in production to facilitate diagnosis of faulty boards.

BOARD VISUALIZATION

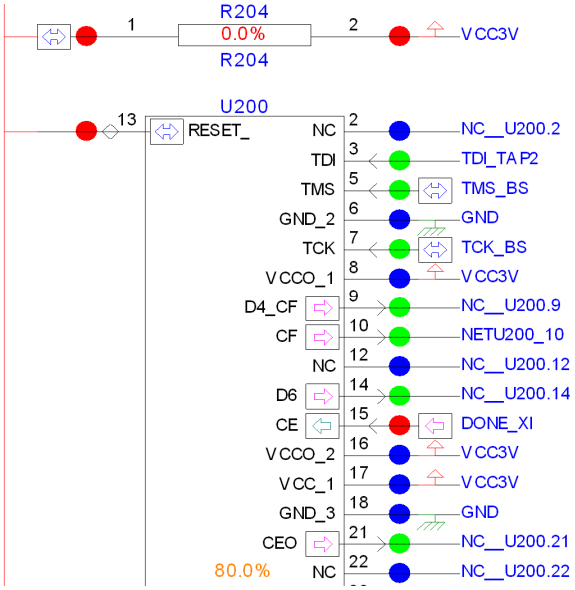
The powerful and flexible viewer, **QuadView®**, allows users to select items within the TestWay report and view the corresponding areas either on the schematic of layout diagrams.
It has a unique PDF digitization capability that allows users to convert searchable PDF files for interactive cross referencing with TestWay.



QuadView provides visualization of test coverage and customer attributes in both the schematic and layout views to clearly identify pin and device coverage, such as a green dot for covered and a red dot for uncovered pins.



TestWay also allows users to reconstruct "virtual schematics" directly from a netlist, providing a navigation capability that includes advanced graphical symbols to identify board interconnections.



Visualization features are:

- Import schematic from standard formats such as HPGL, PDF etc.
- Create layout views from standard formats such as CAMCAD, FATF, ODB++, GENCAD, or direct from native CAD layout data. No pre-processing needed.
- Search components, pins and nets throughout hierarchical designs and multiple sheets.
- Cross-probe between schematic, layout and TestWay reports.
- Capture snapshots of schematic or layout information for cut and paste into design/testability review reports.
- Show pin direction and BST functionality in virtual schematic view.
- Visualize test coverage by color coding devices, pins and nets according to test accessibility i.e. BST interconnect, BST cluster, ICT, FPT, etc.

TESTER EXPORTERS

TestWay is able to generate test data files for BST test systems including ASSET, ACCULOGIC, CORELIS, JTAG Technologies, GOEPEL,VICTORY, etc, directly from schematic data.
This adds significant benefits for boundary-scan development because tests can be created prior to layout, ensuring availability for early prototype builds. Boundary-scan development time is reduced by at least 30% by exporting TestWay test strategy data files to the target test development system.

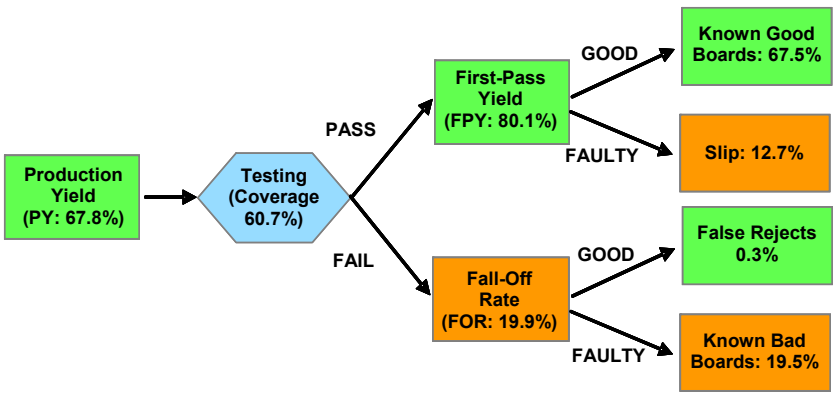
ADVANCED REPORTING

TestWay exports all available information into a standard database in order to analyze any type of test scenario, including single or multi-board configurations.
Multi-board analysis is particularly useful in system configurations that comprise of mother and daughter card combinations or in system configurations where test coverage estimations that include inter-board connectivity are mandatory.

The TestWay data can be exported in a variety of formats such as:

- Microsoft EXCEL
- XML
- HTML
- Crystal reports
- ASCII file in custom format
- Fully customizable graphical files

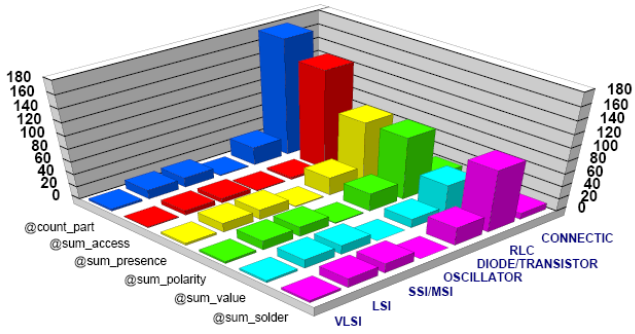
Reports are used to show estimated production yield obtained from historical DPMO data. The test coverage is calculated based on the defects that will be detected by a selected test strategy including inspection and test systems, such as boundary-scan, in-circuit, flying probe, etc.



TestWay reports can be used to identify areas for improving test coverage:

- Develop additional tests such as:
  boundary-scan cluster test, vector-less test, enhanced test patterns, etc.
- Suggest design modifications such as:
  additional physical test access, improved boundary-scan implementation, etc.
- Select additional complementary test strategies.

The initial test scenario can then be fine tuned to determine the best possible production yield, ensuring that good products are shipped to the customer. Charts are provided that identify 'coverage per defect category and by component complexity' for the following defect categories: presence, polarity, value and solder.



COST MODELING

The cost model provides total cost details such as:

- Test fixture hardware costs: fixture frame, wiring, spring probes, vector-less sensors, etc.
- Engineering costs: fixture & test program development.
- Test execution time: important for flow line balance.

For example cost modeling can calculate the actual cost savings that can be expected by adopting a complementary ICT and BST test strategy, where the number of fixture probes can be significantly reduced due to test point optimization.

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