# NEUROMEM®
# NEURAL NETWORK IP CORE

- Lowest Latency Pattern Learning and Classification
- Responsible and Explainable AI
- Real-time incremental learning
- Simple interface through 15 Register Transfer Level commands

A NeuroMem neural network is highly **inspired by the human brain**:

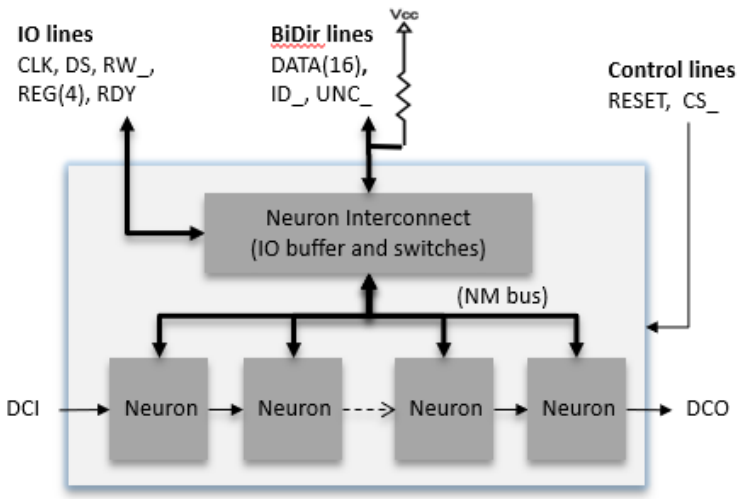
Neurons are memories with their own logic to learn and recall patterns while interacting with one another without any supervising unit
Neurons process all queries in parallel, whether to learn or recognize
Neurons autonomously react to stimuli matching or similar to their own memory content
The winner-takes-all and inhibits weaker responders. Responses are auto sorted per level of confidence
Two types of classifiers can be selected: Radial Basis Function or K-Nearest Neighbor classifier
The neurons know when they do not know and can therefore learn
The neurons auto correct themselves if a teacher contradicts their original response
Parallel architecture; energy efficient and highly scalable with no impact on the number of I/Os
For deatiled information refer to the NeuroMem Technology Reference manual.

| ANN Attributes | |
|---|---|
| Neuron memory size | 256 bytes |
| Categories | 15 bits |
| Distances | 16 bits |
| Contexts | 7 bits |
| Recognition status | Identified, Uncertain or Unknown |
| Classifiers | Radial Basis Function (RBF)<br>K-Nearest Neighbor (KNN) |
| Distance Norms | L1 (Manhattan), Lsup |

| Performances @ 18Mhz | |
|---|---|
| Broadcast pattern | < 14 µsec |
| Learn | 1 µsec |
| Best match | 2 µsec |
| Top K matches | K * 2 µsec |
| 128 neurons | equivalent to 9 Giga OPS |
| 2048 neurons | equivalent to 384 Giga OPS |

## PARALLEL EXPANDABLE ARCHITECTURE

A NeuroMem neural network is an assembly of 1 Neuron_Interconnect and N Neuron cores.




- The Neuron_Interconnect IP core connects all the Neurons together, enabling a broadcast mode to all the neurons in parallel, and their necessary interaction for the time of a learning or recognition.
- The Neuron IP core is a memory cell surrounded with logic gates and 26 IO lines
    - Default= 256 x 8-bits SRAM memory
    - 3000 ASIC gates or 4800 FPGA LUTs

A network of N neurons is designed by daisy-chaining N Neuron IP cores and connecting their 26 IO lines to the Neuron_Interconnect IP core.

**No address bus, just 26 fixed IO lines = NeuroMem bus**
The NeuroMem bus is the same to interconnect neurons internally and externally.

## IP PACKAGE

- Netlist of the Neuron IP and Neuron_Interconnect IP
- Documentation
- Full test benches (Verilog) for both verification and production