SWTEST ASIA 2018

Proceedings

October 18 – 19, 2018
Sheraton Hsinchu Hotel
Zhubei City, Taiwan

Welcome to SWTest Asia 2018

1st Annual SWTest Asia Conference

Welcome SWTest Asia Attendee!

On behalf of the SWTest Asia Team it is our great pleasure to welcome you to the inaugural SWTest Asia Conference and EXPO at the Sheraton in Hsinchu, Taiwan. We would like to thank the sponsors (9-platinum, 2-gold, and 9-silver), the 42 exhibitors, and SWTest Team for their support to make SWTest Asia a valuable event for the Asian wafer test community.

For the 1st Annual Conference, we are pleased to have a Technical Program with 8 outstanding podium presentations and two excellent Keynotes from Dr. Harry Chen, Chair of the MediaTek Design Technology R&D Lab, and from Lin Fu, Ph.D., and John West of VLSI Research.

During the 2018 SWTest Asia EXPO, premier suppliers to the wafer test industry will have an opportunity to showcase their latest product offerings and technical services. New for SWTest Asia, we have created a "Tech Showcase" Track for Platinum Sponsors during which they will make short presentations and/or have product demonstrations.

Once again, thank you for being a part of the 1st Annual SWTest Asia Conference and EXPO; and we hope that you enjoy your time in Taiwan and the Hsinchu area.

Jerry Broz, Ph.D.
General Chair, SWTest Asia
International Test Solutions

Clark Liu
Program Chair, SWTest Asia
Powertech Technology, Inc.

Rey Rincon
Program Co-Chair, SWTest Asia
Translarity, Inc.

Maddie Harwood
Finance Chair &
Conference Management,
SWTest Asia

2018
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Conference

SWTEST ASIA 2018

PROGRAM SCHEDULE

SWTest Asia 2018
Platinum Sponsors

international TEST SOLUTIONS

FormFactor™

JEM

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PROGRAM SCHEDULE

SWTest Asia 2018
Gold Sponsors

ZENFOCUS

HTSi Hermes Testing Solutions Inc.

SWTest Asia 2018
Silver Sponsors

ADVANTEST

FEINMETALL Contact Technologies

WinWay Technology

ERS

T.I.P.S. Technical Innovation - Physical Solutions

Hitachi Chemical Working On Wonders

SEMICS

TECHNOPROBE Wafer Probing Technologies

AIS Technology, Inc. Advanced Interface Substrate

2018

SWTest Asia Conference

PROGRAM SCHEDULE

"Program Overview At A Glance"

Day One	Thursday, October 18th, 2018
9:00 – 12:00	Exhibitor Registration Open Exhibitor Setup in Expo Hall with 42 booths – Exhibitors Only
12:00	Attendee Registration Open
12:00 – 16:00	Attendee Registration Open Expo Open
12:00 – 14:00	Lunch in Expo Hall – Two Sessions
15:00 – 16:00	Tea Break in Expo Hall
16:00 – 17:00	***Chair's Opening Remarks*** ***Thursday Keynote Presentation in Chapel Room*** Dr. Lin Fu and John West, VLSI Research
17:00 – 18:00	Welcome Reception in Expo Hall

Day Two	Friday, October 19th, 2018
8:00 – 17:00	Attendee Registration Open
8:30 – 9:15	***Chair's Opening Remarks*** ***Friday Keynote Presentation in General Session Room*** Dr. Harry Chen *Chair of MediaTek's Design Technology R&D Lab*
9:15 – 10:00	Expo Open & Tea Break in Expo Hall
10:00 – 12:00	**"*Innovations for the Next Generation of Test*" in General Session Room** Full Conference Only Expo Open
12:00 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions
14:00 – 16:00	**"*Asia Probing Spotlight*" in General Session Room** Full Conference Only Expo Open
16:00 – 16:15	Awards for Best Presentations
16:15 – 17:00	Closing Reception in Expo Hall

There will be a total of eight 30-minute technical papers, 14 hours of Expo, 2 tea breaks, 2 lunches, and 2 receptions

2018
SWTest Asia
Conference

SWTEST ASIA 2018

PROGRAM SCHEDULE

Program Overview

After 28 years in San Diego, California, the SWTest Team is proud to announce our 1st Annual SWTest Asia conference to be held in Hsinchu, Taiwan, October 18-19, 2018. This one and one-half day conference will be a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas. As with SWTest in San Diego, CA, there will be a very relaxed atmosphere with Technical Sessions, an EXPO, and a Tech Showcase, as well as our signature relaxed environment for "informal discussion and networking".

This inaugural event has attracted attendees from the local and regional semiconductor industry to include ASE, TSMC, Ardentec, KYEC, SPIL, Micron, ChipMOS, UMC, Winbond, PTI, and more. Visitors to the conference will come from Japan, Korea, China, Singapore, India, Philippines, and Malaysia. Conference registration includes all meals, refreshments, social activities, and technical program and exhibit attendance, as well as the eProceedings.

Thursday, October 18th, 2018	
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12:00 – 16:00	Attendee Registration Open Expo Open
12:00 – 14:00	Lunch in Expo Hall – Two Sessions
15:00 – 16:00	Tea Break in Expo Hall
16:00 – 17:00 *Space Available Seating*	***Welcome to SWTest Asia 2018*** Dr. Jerry Broz, SWTest General Chair Clark Liu, SWTest Technical Program Chair ***Thursday Invited Presentation in Chapel Room*** ***Semiconductor Industry Entering a New Era as the World Finds Ways to Extract More Value from Chips***  **Dr. Lin Fu** *Technical and Market Analyst* *VLSI Research*  **John West** *Managing Director* *VLSI Research Europe*
17:00 – 18:00	Welcome Reception in Expo Hall

2018

SWTest Asia
Conference

SWTEST ASIA 2018

PROGRAM SCHEDULE

Program Overview

Friday, October 19th, 2018

8:00 – 17:00	Attendee Registration Open
8:30 – 9:30	***Welcome to SWTest Asia 2018*** Dr. Jerry Broz, SWTest General Chair Clark Liu, SWTest Technical Program Chair ***Friday Keynote Presentation in General Session Room***  **Facing Test Challenges in Upcoming AI/5G-based Systems Opportunity for Radical Ideas** **Dr. Harry Chen** *Chair of MediaTek's Design Technology R&D Lab*
10:00 – 12:00	**"*Innovations for the Next Generation of Test*" in General Session Room** Full Conference Only Expo Open
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gram Overview

2018

SWTest Asia Conference

PROGRAM SCHEDULE

Program Overview	
Technical Session 1	**Innovations for the Next Generation of Test** **Session Chair**: Dr. Jerry Broz, General Chair (International Test Solutions)
10:00 – 10:30	**Next Generation OSAT – Innovative Circuit Probing with AI implement** Huang Po-Hao (TeraPower Technology Inc. – Taiwan)
10:30 – 11:00	**Wafer Level Efficient Characterization and Testing of MRAM** Dr. Siamak Salimy (Hprobe – France) Hantsun Chung (Hermes Epitek - Taiwan)
11:00 – 11:30	**Overcoming Challenges for 5G Production Tests** Dr. Choon Beng Sia (FormFactor, Inc. – Singapore)
11:30 – 12:00	**Simulation and verification of FeinProbe Probe Card Model for the 5G WLCSP Application** Krzysztof Dabrowiecki (Feinmetall GmbH – Germany) Adrian Lim (Feinmetall GmbH – Singapore) Jose Moreira (Advantest – Germany) Thomas Gneiting and Ali Abdallah (AdMOS – Germany) Paul Hurst (Harbor-Electronics – United Kingdom)
12:00 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions

Technical Session 2	**Technical Session 2 – Asia Probing Spotlight** **Session Chair:** Clark Liu, Program Chair (Powertech Technology, Inc.)
14:00 – 14:30	**LED Wafer Probe Test** Yoichi Funatoko (FormFactor, Inc. – Japan)
14:30 – 15:00	**Improve the Accuracy of High Speed Simulation to Meet 56G/112G Testing Requirement on PCB** Jackie Luo (Shanghai Zenfocus Semi-Tech Co.,Ltd – China)
15:00 – 15:30	**High Performance CIS Wafer Probing using 2D MEMS Technology** Dr. Yunhwi Park, Kyungsub Kim, Youngjin Kim, and Sungjoon Kang (Korea Instruments – Korea) Chang-Hoon Hyun (Samsung Electronics/S.LSI Division – Korea) Kyushik Min (Samsung Electronics. Co. – Korea)
15:30 – 16:00	**Hybrid Type (Mixed Probe Types) Vertical Probe Card** Bryan Lee and James Park (TEPS Co., Ltd – Korea)
16:00 – 16:15	Awards for Best Presentations
16:15 – 17:00	Closing Reception in Expo Hall

2018
SWTest Asia
Conference

PROGRAM SCHEDULE

2018 EXHIBITORS

Advantest Corporation
AIS Technology, Inc.
Celadon Systems
Chain-Logic International Corp.
CHPT
Complete Probe Solutions
ERS electronic GmbH
Feinmetall GmbH
Ferrotec Ceramics Corporation
FormFactor
Hermes Testing Solutions Inc.
Hitachi Chemical Co., Ltd.
Integrated Technology Corporation
International Test Solutions
InTEST Corporation
IWIN Co., Ltd.
JEM Taiwan
Johnstech International
Korea Instrument
MarTek, Inc
Microfriend Inc.
MJC Taiwan
MPI Corporation
NHK Spring Co., Ltd.
Nidec SV TCL
Oxford Lasers
PLI Co.,Ltd
R&D Altanova
Rudolph Technologies, Inc.
SEMICS
Shanghai Zenfocus Semi-Tech Co., Ltd
Specialty Coating Systems
STAr Technologies, Inc.
T.I.P.S. Messtechnik GmbH
Tanaka Precious Metals
Technoprobe America Inc.
Teradyne, Incorporated
Test Tooling Solutions Group
Veco B.V.
Vermont Microtechnologies
WinWay Technology
Xcerra Corporation

2018

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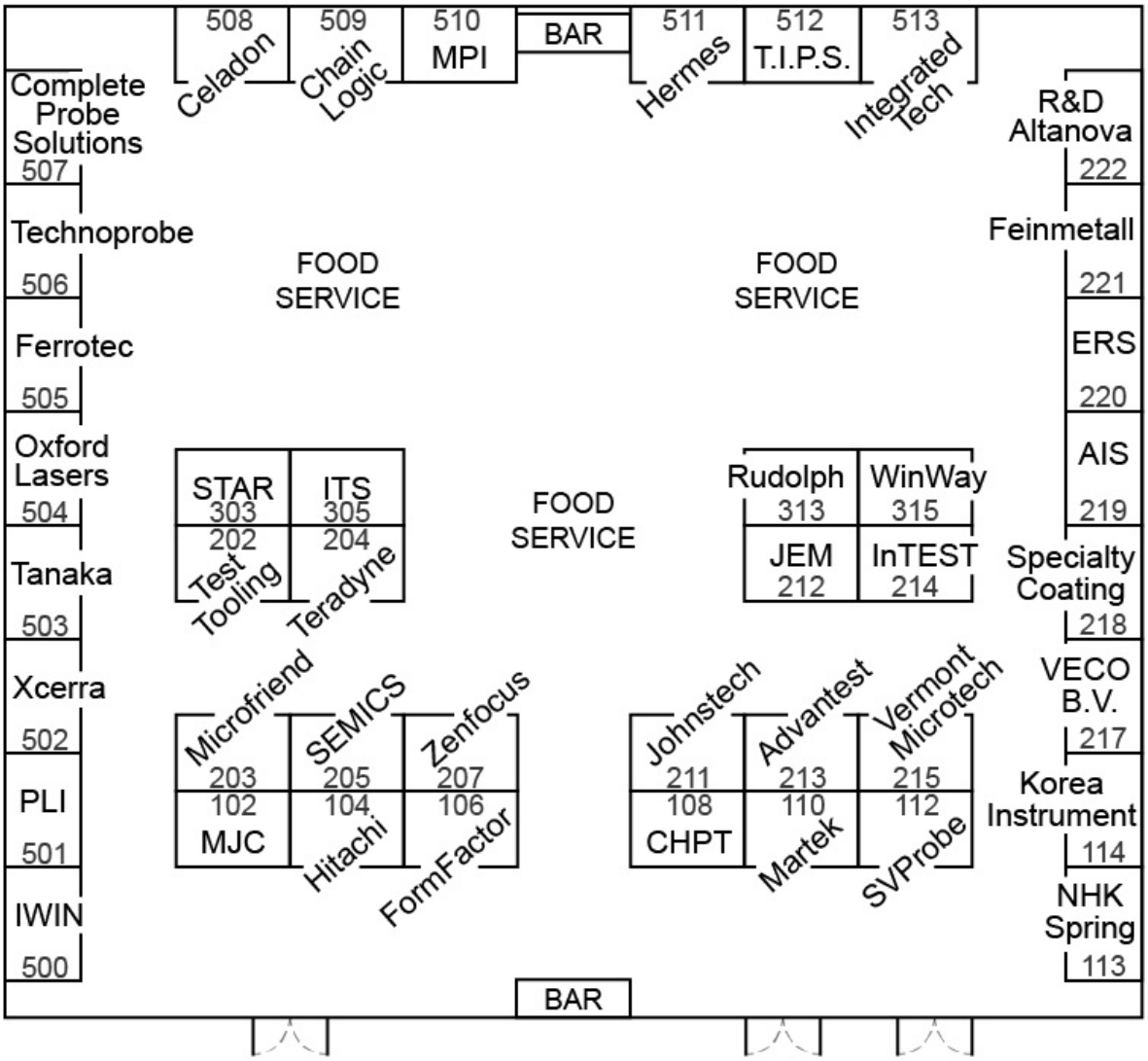
Conference

SWTEST ASIA 2018

PROGRAM SCHEDULE

EXPO HALL



2018
SWTest Asia
Conference

PROGRAM SCHEDULE

2nd Annual SWTest Asia

Coming in October, 2019
(dates will be announced soon!)

2018
SWTest Asia
Conference

SWTEST ASIA 2018

PROGRAM SCHEDULE

SWTW

Save The Dates

SWTest Workshop 2019

Rancho Bernardo Inn,
San Diego, CA
June 2 - 5, 2019

Abstract Submission Date
March 5, 2019

Golf Tournament
June 2, 2019

See You Next Year!

Thanks for your Support !

- **Contact the SWTest Asia Team with any questions**

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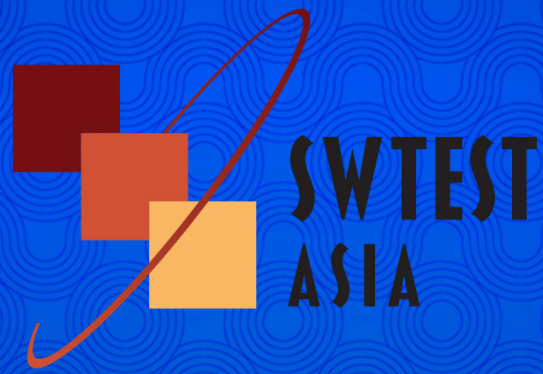
2nd Annual SWTest Asia
Coming in October, 2019
(will be announced soon!)

Thanks for Attending SWTest Asia !

We Hope to See you at SWTest San Diego June 2 to 5, 2019 !!!

Rancho Bernardo Inn, San Diego, CA

1st Annual SWTest Asia | Taiwan, October 18-19, 2018



Technical Program
SWTest Asia 2018

Friday, October 19, 2018

Taiwan, October 18-19, 2018

Friday, October 19, 2018

08:30 to 09:30 – Welcome to SWTest Asia 2018

Welcome SWTest Asia 2018

Dr. Jerry Broz (SWTest Asia General Chair) and Clark Liu (SWTest Asia Program Chair)

Facing Test Challenges in Upcoming AI/5G-based Systems Opportunity for Radical Ideas

Dr. Harry Chen

Chair of MediaTek's Design Technology R&D Lab

MEDIATEK

Friday, October 19, 2018

10:00 to 12:00 – Innovations for the Next Generation of Test

Next Generation OSAT – Innovative Circuit Probing with AI implement

Huang Po-Hao (TeraPower Technology Inc. – Taiwan)

Wafer Level Efficient Characterization and Testing of MRAM

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Dr. Choon Beng Sia (FormFactor, Inc. – Singapore)

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Krzysztof Dabrowiecki and Adrian Lim (Feinmetall GmbH), Jose Moreira (Advantest), Thomas Gneiting and Ali Abdallah (AdMOS), and Paul Hurst (Harbor-Electronics – UK)

Friday, October 19, 2018

14:00 to 16:30 – Asia Probing Spotlight

LED Wafer Probe Test

Yoichi Funatoko (FormFactor, Inc. – Japan)

Improve the Accuracy of High Speed Simulation to Meet 56G/112G Testing Requirement on PCB

Jackie Luo (Shanghai Zenfocus Semi-Tech Co., Ltd – China)

High Performance CIS Wafer Probing using 2D MEMS Technology

Dr. Yunhwi Park, Kyungsub Kim, Youngjin Kim, and Sungjoon Kang (Korea Instruments – Korea)

Chang-Hoon Hyun and Kyushik Min (Samsung Electronics. Co. – Korea)

Hybrid Type (Mixed Probe Types) Vertical Probe Card

Bryan Lee and James Park (TEPS Co., Ltd – Korea)

Additional Presentations

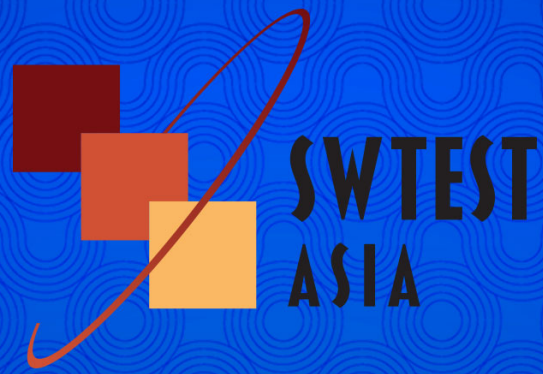
Please contact the authors regarding their work

KGD – Known Good >POWER< Die Diced Wafer Test at 7 kV and 1000 A

Mauro Serra (CREA Test), Jens Lochbaum (INFOTECH Automatio)
and Rainer Gaggl (T.I.P.S. Messtechnik)

A High-density Area-array Probe-unit with Non-discontinuous Fan-out Structure without Space Transformer using Monolithic Fabrication Method

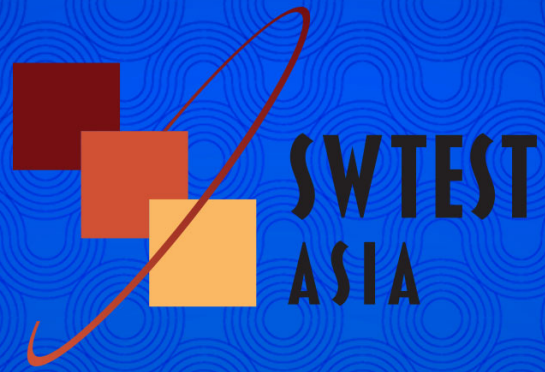
Gunsei Kimoto, Takayuki Kakinuma, Masao Seimiya (ProbeAce Co.,Ltd. – Japan)



Technical Program
SWTest Asia 2018

Friday, October 19, 2018

Taiwan, October 18-19, 2018



Welcome to the 1st Annual SWTest Asia in Taiwan

Jerry Broz, Ph.D.
General Chair, SWTest Asia
International Test Solutions

Clark Liu
Technical Program Chair, SWTest Asia
Powertech Technology, Inc.

Taiwan, October 18-19, 2018

Welcome to the Sheraton, Hsinchu !

1st Annual SWTest Asia | Taiwan, October 18-19, 2018

SWTest San Diego and SWTest Asia

- For 28 years, Semiconductor Wafer Test (SWTest) has been held annually in San Diego, CA, every June.
- SWTest is internationally recognized as the premier wafer test technology conference.
- Each year more than 500 industry leaders and technologists committed to solving problems and driving innovation attend.
- International attendance at SWTest has grown substantially; and, in 2018, almost 30% of the attendees came from Asia and Pacific Rim.
- SWTest Chairs decided to expand the conference because of Asia's tremendous technological importance to semiconductor and wafer level test.
- SWTest Team is proud to welcome you to the 1st Annual SWTest Asia Conference held in Hsinchu, Taiwan.

Held Annually
During June
In San Diego, CA

To be Held Annually
During October
In the Asia Region

1st Annual SWTest Asia | Taiwan, October 18-19, 2018

SWTest Asia Chairs and Committee

- **SWTest Asia Chairs**
  - Dr. Jerry Broz, General Chair (International Test Solutions)
  - Clark Liu, SWTest Asia Technical Program Chair (Powertech Technology, Inc.)
  - Rey Rincon, Technical Program Co-Chair (Translarity, Inc.)
  - Maddie Harwood, Finance and Conference Management Chair

- **SWTest Asia Committee Members**
  - Nobuhiro Kawamata, FormFactor K.K.
  - Joey Wu, STAr Technologies

Welcome to SWTest Asia 2018

- **SWTest Asia IS a Probe Technology Forum**
  - Technical Conference for Wafer Test Professionals
  - Providing practical solutions to real problems faced by probing technologists
  - Balanced mixture of presentations from semiconductor manufacturers, suppliers, and collaborations.

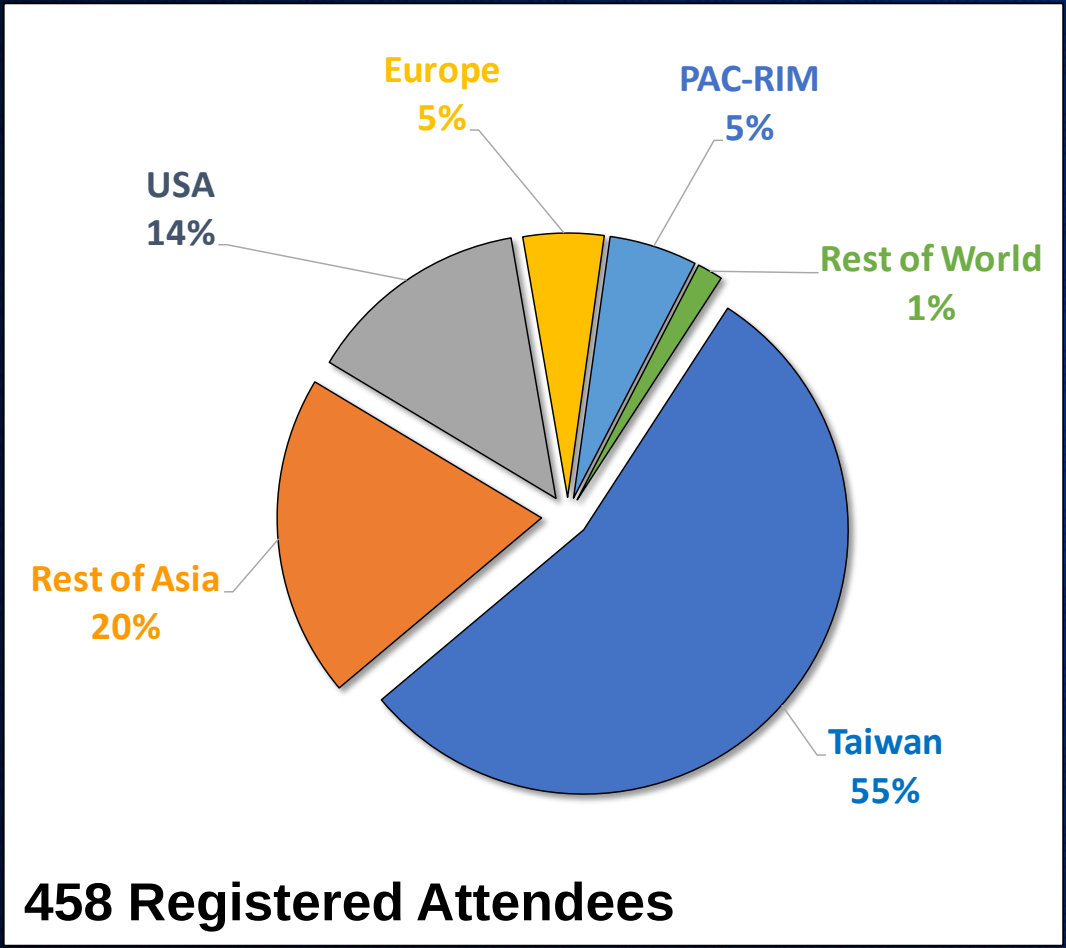
- **Informal Conference with a Relaxed Atmosphere**
  - "Workshop Style" conference focused on technical exchange
  - Great opportunities for friendly discussions and networking
  - Meet new people and have a little fun !

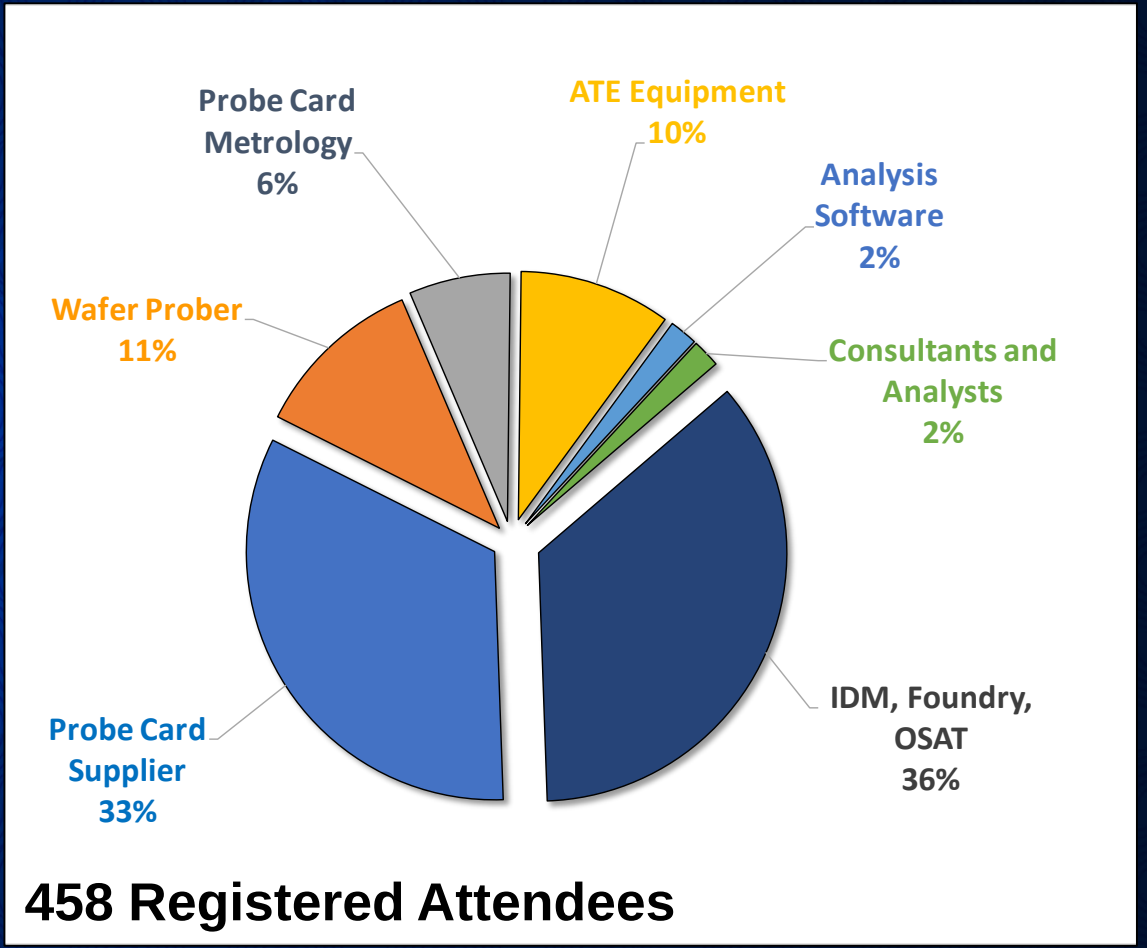
- **"Green Initiative" …**
  - eProceedings and enviro-friendly practices

Technical Program / Agenda

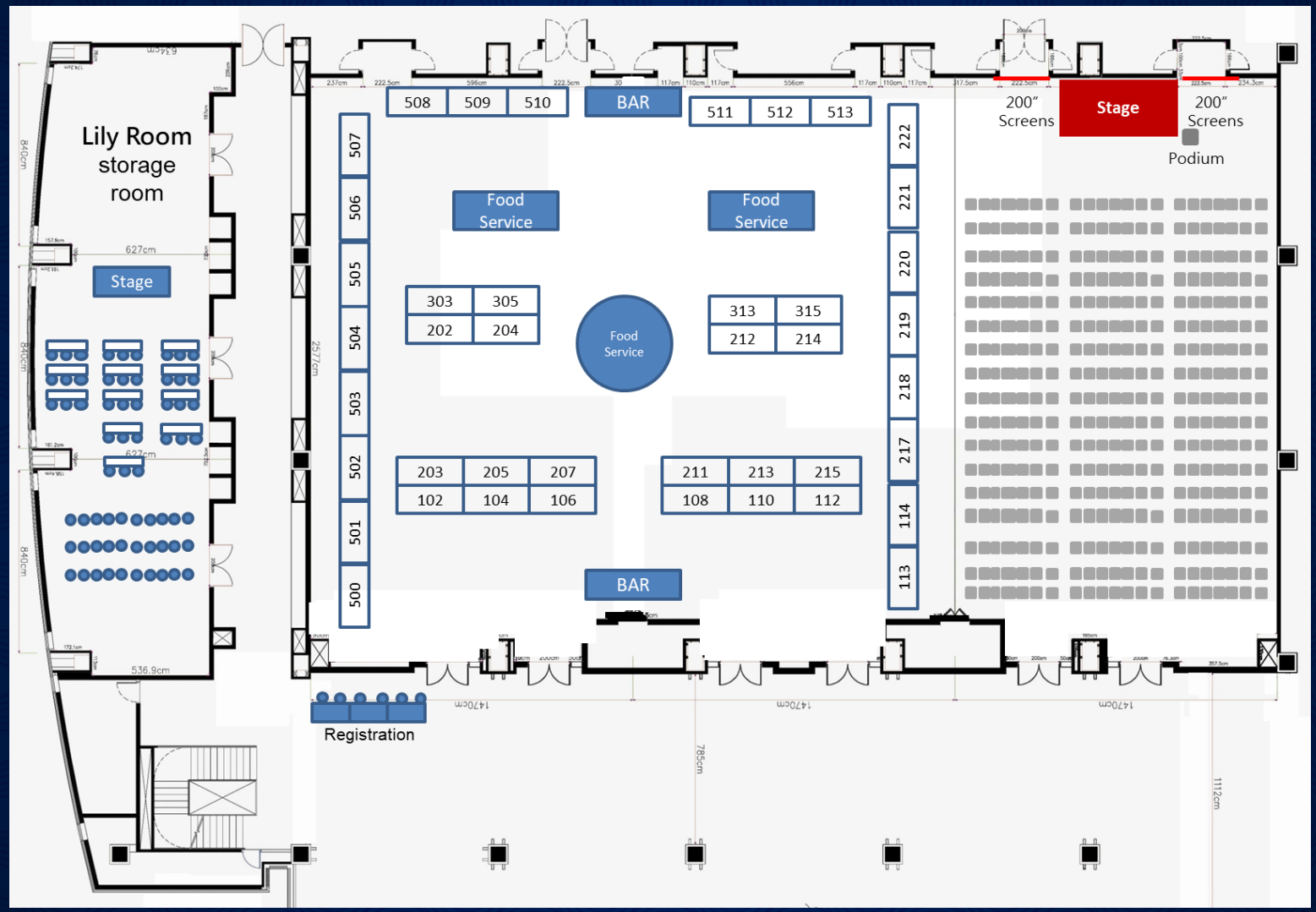
- **Thursday, October 18**
  - SWTest Asia EXPO 2018 with 42-key suppliers
  - SWTest Asia Technology Showcase Presentations with Platinum Sponsors
  - Invited Presentation from Dr. Lin Fu and John West of VLSI Research
  - Welcome Reception in Expo Hall
- **Friday, October 19**
  - Keynote from Dr. Harry Chen, Chair of MediaTek's Design Technology R&D Lab
  - Technical Program with 2-podium sessions
    - 1000 to 1200: Innovations for the Next Generation of Test
    - 1400 to 1600: Asia Probing Spotlight
  - SWTest Asia EXPO 2018 with 42-key suppliers
  - SWTest Asia Technology Showcase Presentations with Platinum Sponsors
  - Closing Reception in Expo Hall

SWTest Asia 2018 Demographics

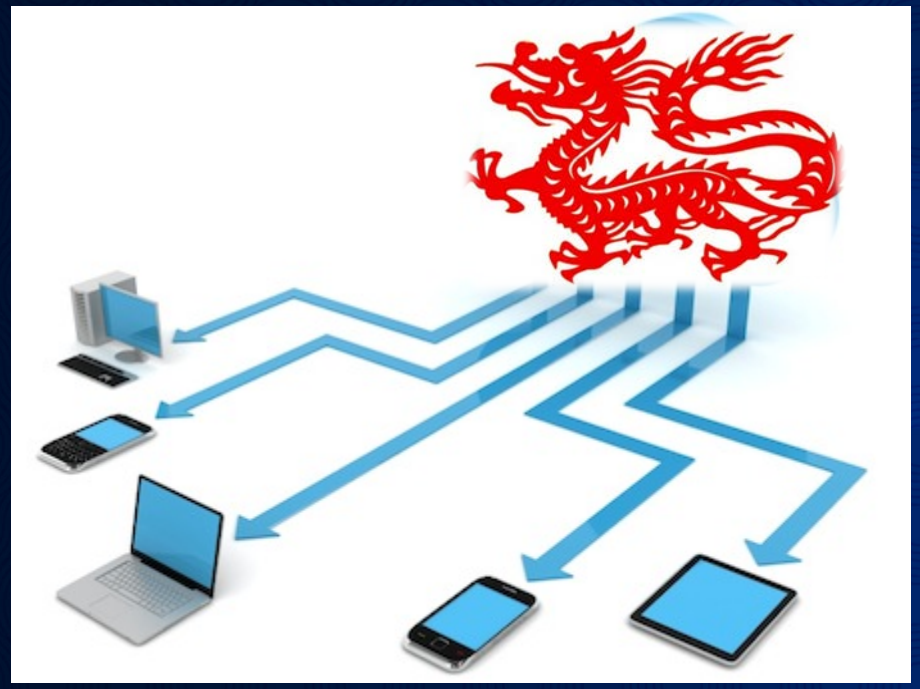




Map of the Area



SWTest Asia 2018 eProceedings



ePROceedings Password:

dragon

- **Conference e-Version is available for download in a password protected file.**
  - **Go to … http://www.swtestasia.org**
  - **Ballroom WiFi Password =**
- **Free WiFi access will be available during the entire conference to allow attendee access to the downloads.**
- **Password for the download files will be announced throughout each day and at the registration desk.**
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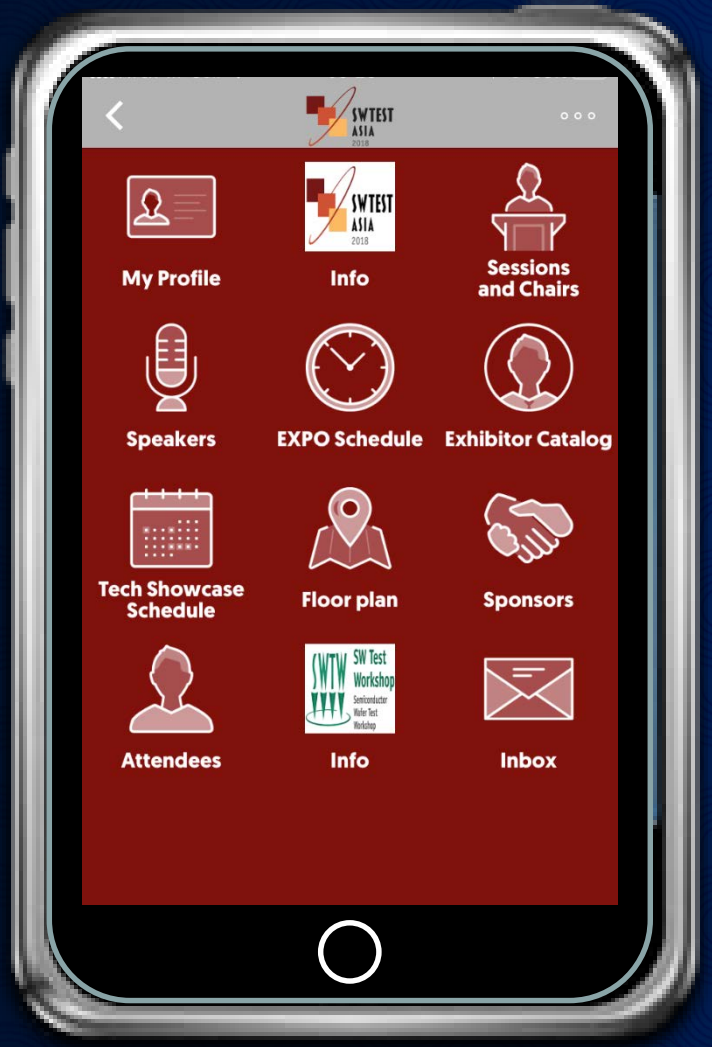
SWTest Asia App – “In the Palm of Your Hand”



- Up-to-the-minute “Event Info”
- Schedules of the “Sessions”
- Connect with the “Speakers”
- Meet with the “Exhibitors” and “Sponsors”
- Attend the “Tech Showcase”
- Get oriented on the “Floorplan”
- Network with the “Attendees”
- Get important updates with “SWTest Inbox”
- Learn about “SWTest in San Diego”

Platinum Sponsors

Gold Sponsors

Silver Sponsors

Thursday Invited Speakers

"Semiconductor Industry Entering a New Era as the World Finds Ways to Extract More Value from Chips"

Dr. Lin Fu
Technical and Market Analyst
VLSI Research Europe

VLSIresearch

John West
Managing Director
VLSI Research Europe

Friday Keynote Speaker

Facing Test Challenges in Upcoming AI/5G-based Systems Opportunity for Radical Ideas

Dr. Harry Chen
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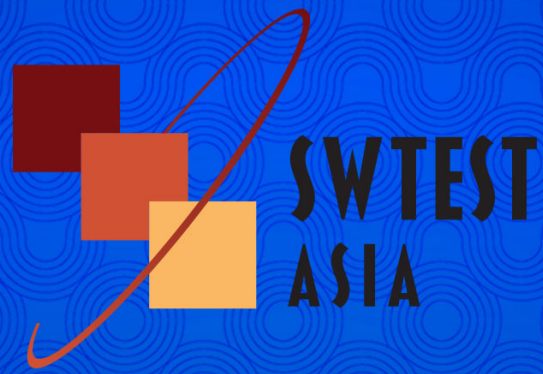

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SWTest Asia 2018

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Chang-Hoon Hyun and Kyushik Min (Samsung Electronics. Co. – Korea)

Hybrid Type (Mixed Probe Types) Vertical Probe Card

Bryan Lee and James Park (TEPS Co., Ltd – Korea)

Recognition & Awards

- **Best Data Presentation**
- **Best Overall Presentation**

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June 2 to 5, 2019 !!!

Rancho Bernardo Inn, San Diego, CA

Thanks for your Support !

- **Contact the SWTest Asia Team with any questions**

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Next Generation OSAT
- Innovative Circuit Probing with AI implement

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Product Engineering Div

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Mobile : +886-988-620927

Taiwan, October 18-19, 2018

Overview

- Introduction
  - AI is coming
- Key system (function) presentation
  - Opportunity
  - What we expect
    - Non-stop & real time production : I-AOI solution
    - Technology Application
    - Performance & Comparison
  - Follow on work
- Future development (Next Generation OSAT)
  - Industry 4.0 + AI application for manufacture process

Written by: Loveneesh Tejan Posted on: July 2, 2018

AI is Coming !!

AI is coming , will you join ?

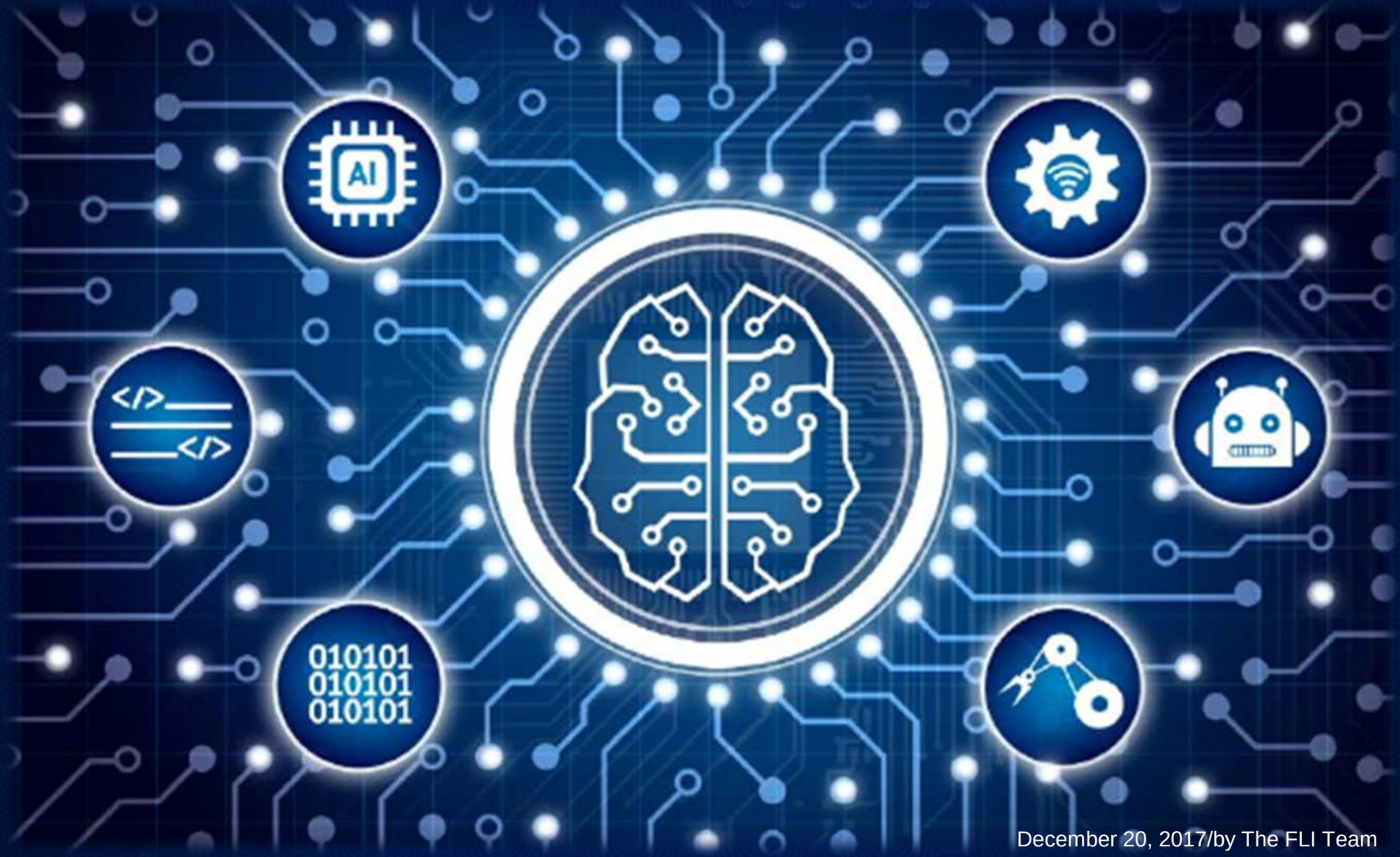
- **Attribute of AI (Artificial Intelligence)**
  - **Autonomy :**

    be able to keep working without the direct intervention of humans or event
  - **Reactivity :**

    be able to perceive current environment and have accurate response
  - **Social ability :**

    be able to interact with other agents (machine) and possibly humans

Elements of AI



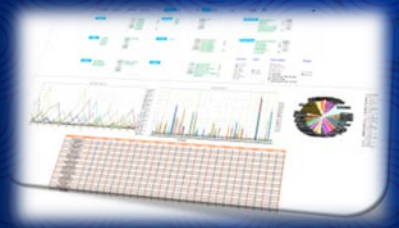
December 20, 2017/by The FLI Team

AI Development Progress

AI future

Self (deep) learning

Big data



Automation

- Quality control
- Setup control
- Efficiency / Yield Monitor
- Trouble shooting
- Cost down

Opportunity

✓ Workflow & Handling

Derivative Issue

- Long pre-heat time (Productivity loss)
- **Re-setup (Productivity loss)**
- **Quality concern**

Test Quality

- Yield / overkill

Appearance Quality

- Probe mark
- OCR

Mechanical / Environemt

- Machine /fixture working
- Environment (temperature)
- Program

Other

- Network
- Facility

Freuquency

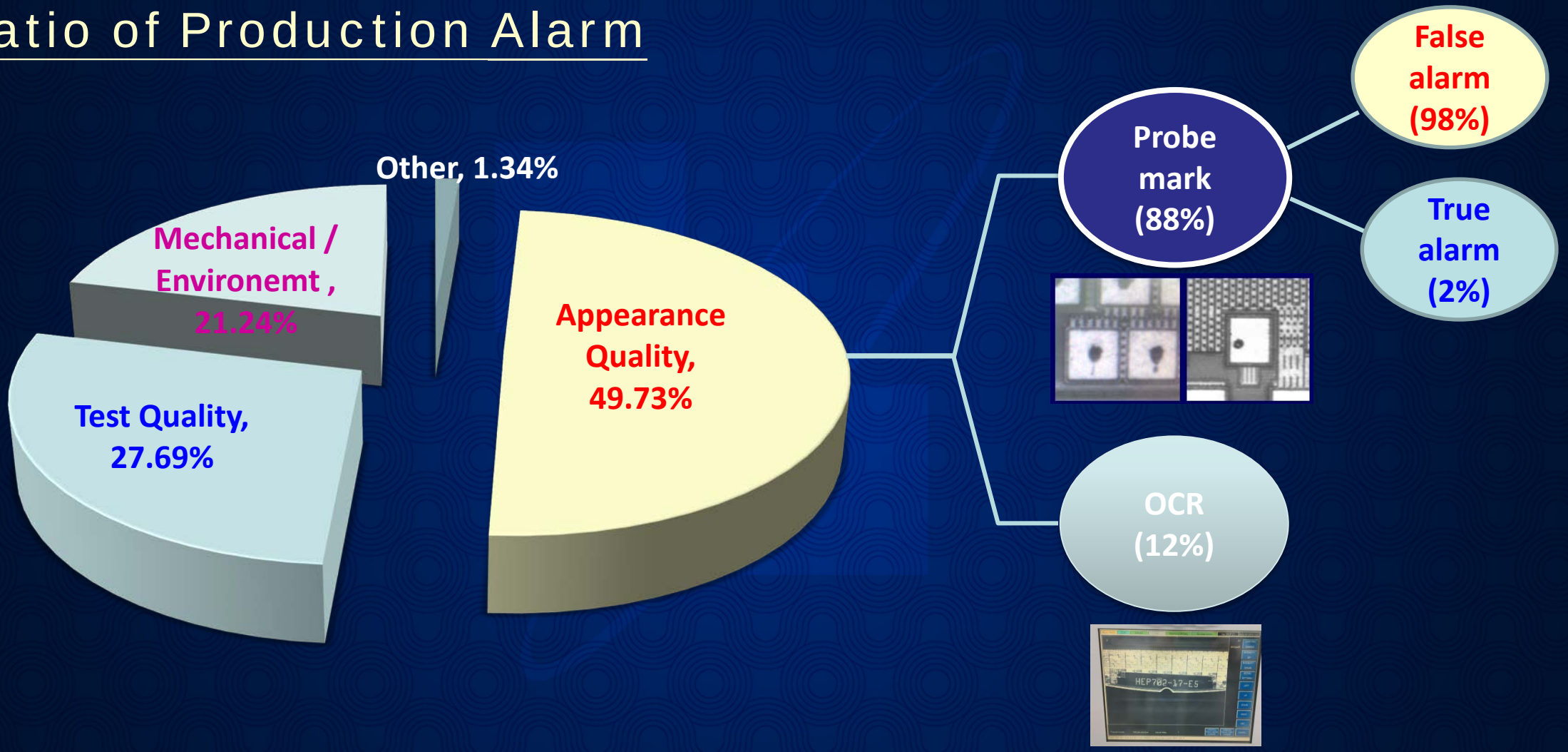
- High alarm rate/ overkill

Derivative Issue

- Long waiting

Opportunity

✓ Ratio of Production Alarm

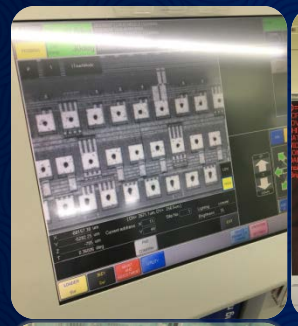


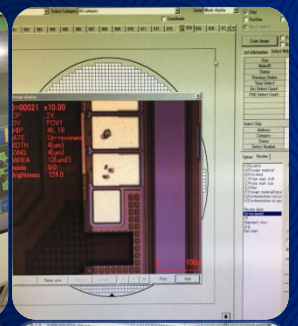
What we expect !!

Non-stop & Real time Disposition : I-AOI Solution

As is

Alarm occur !!





Manpower support for judgement

- False alarm -> Keep going
- True alarm -> Ask engineer to support

To be

Alarm occur !!

AI support for judgement

False alarm

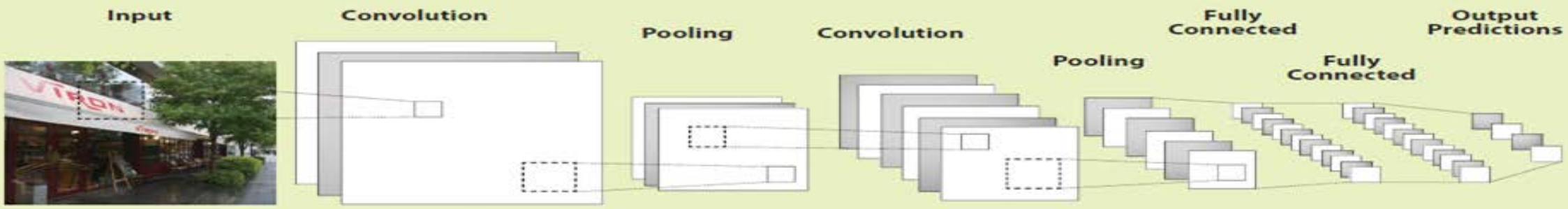
Keep running

True alarm

Engineer for trouble shooting
(Saving 98% effort due to false alarm)

Technical Application

Artificial Neural Networks Application



New Event

Image segment cutting , Unitization
(accuracy base on level)

Self learing

Judge & Foercast

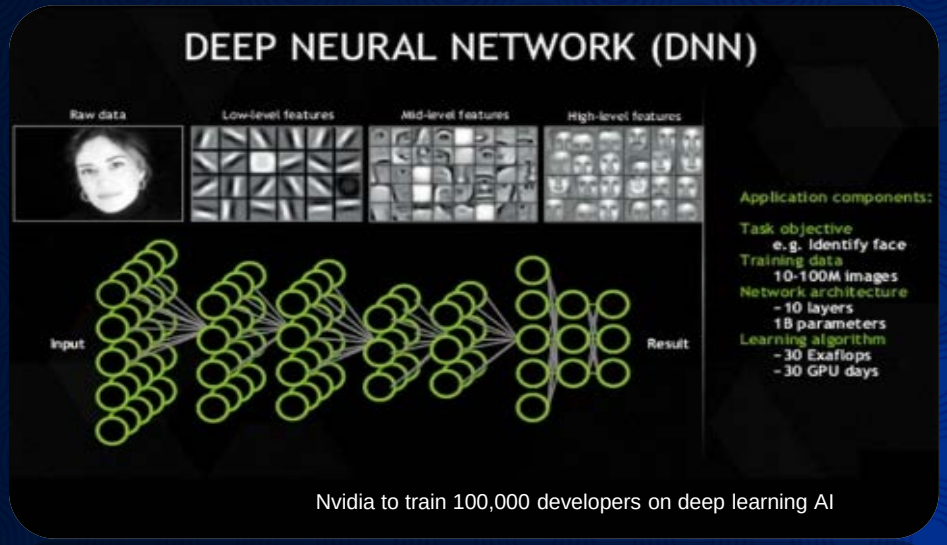
Tooling Java / Scala / Object C++ / OpenCV

PMI image (million of golden image)	Image analysis processing algorithm GPU operation(CUDA or OpenCL) Model construction(MataLab/Simulink)	machine learning algorithm Caffe, Torch, Theano and TensorFlow

Big Data AnalyticsHadoop / Spark

Technical Application

Aritificial Neural Networks

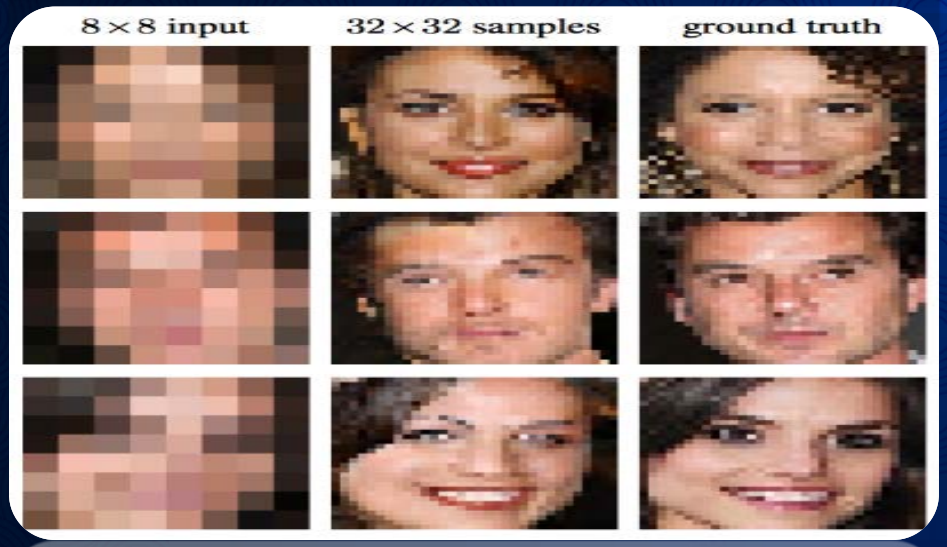


Nvidia to train 100,000 developers on deep learning AI

Real-time analysis of behaviors

yaron / March 16, 2017 / Comments Offon 30 amazing applications of deep learning / AI, Mathematics, Philosophia Naturalis, Writings

Pixel restoration CSI style



Sample Training

Technical Application

Aritificial Neural Networks

Object detection (Machine learning)

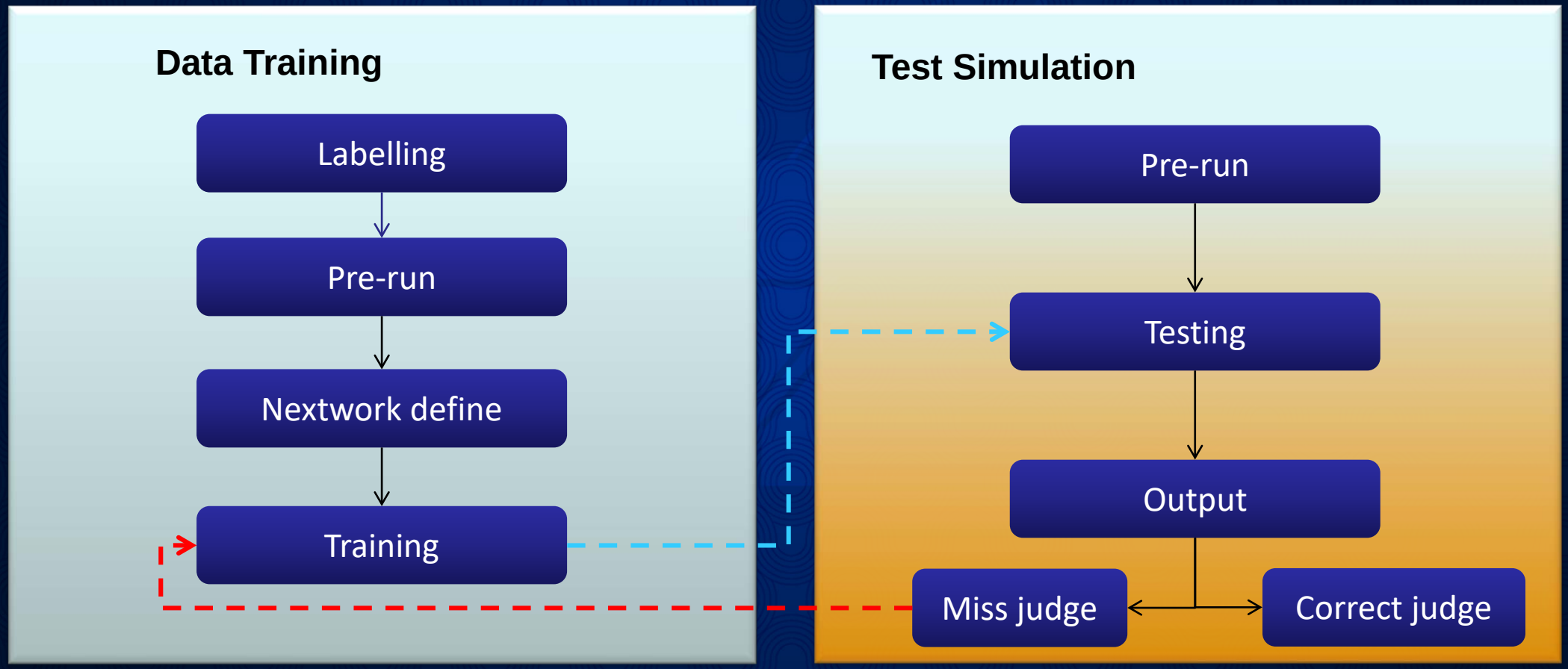
Feature Recognition (Algorithm analysis)

Judge & Forecast
(Find out the target or same one in the database)

Similarity comparison(Algorithm analysis)

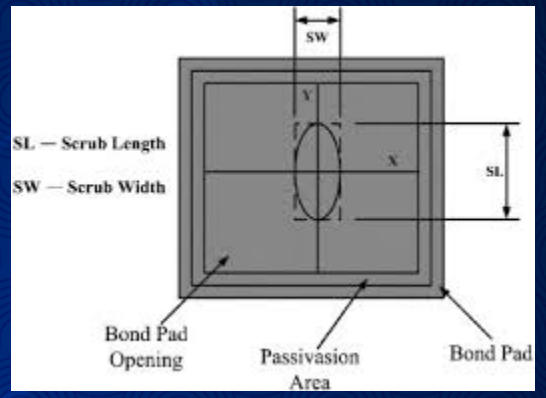
Technical Application

Defect Classification



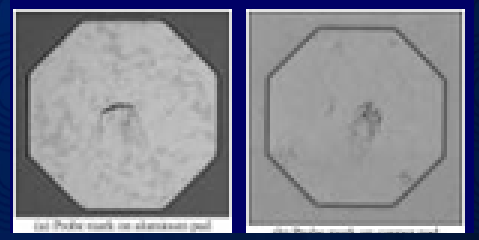
Technical Application

Object Detection
(machine learning)



Feature identification
(Algorithm analysis)

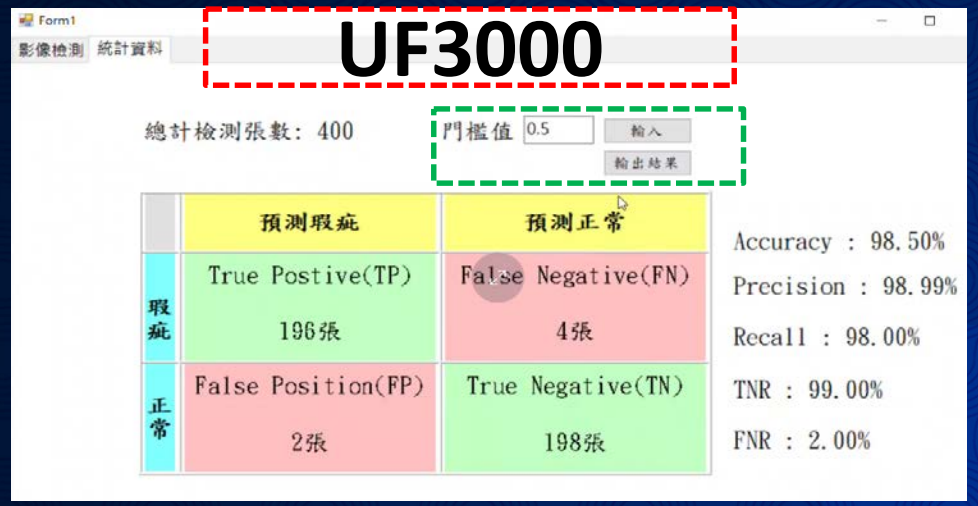
Similarity comparison
(Algorithm analysis)

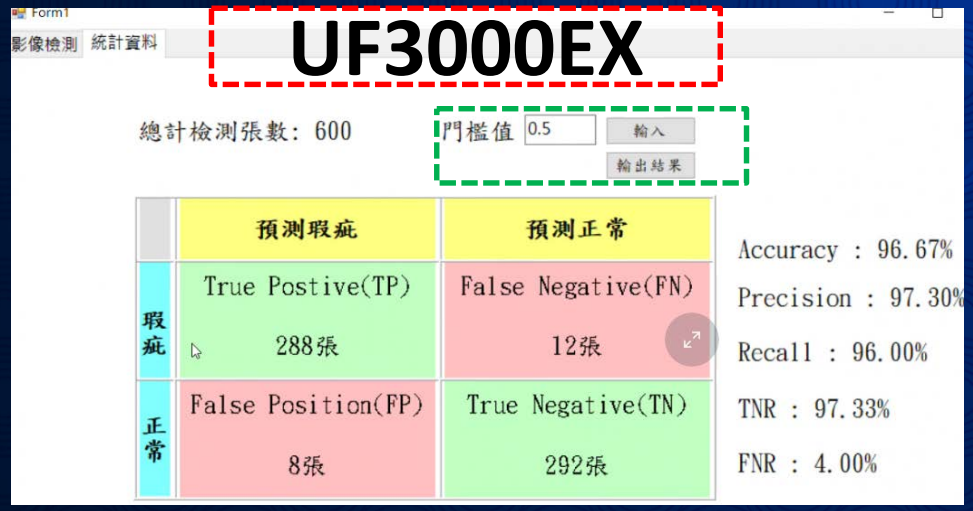


Judge & Forecast

1. Deep Probe Mark (67%)
2. Probe mark deviation (28%)
3. Incorrect setting of touch down (11%)

ITRI Verify Information (Phase1 – 2018/2/5)





UF3000 (B/W)

Total: 400 Pcs image(Pass 200)(Fail 200)

(Fail 200) misjudge→4pcs

(Pass 200) misjudge→2pcs

Accuracy Calculate

100 % -{(F4+P2)/(F196+P198)}*100

=98.5%

UF3000EX (Color)

Total: 600 Pcs image(Pass 300)(Fail 300)

(Fail 300) misjudge→12pcs

(Pass 300) misjudge→8pcs

Accuracy Calculate

100 % -{(F12+P8)/(F288+P292)}*100

=96.5%

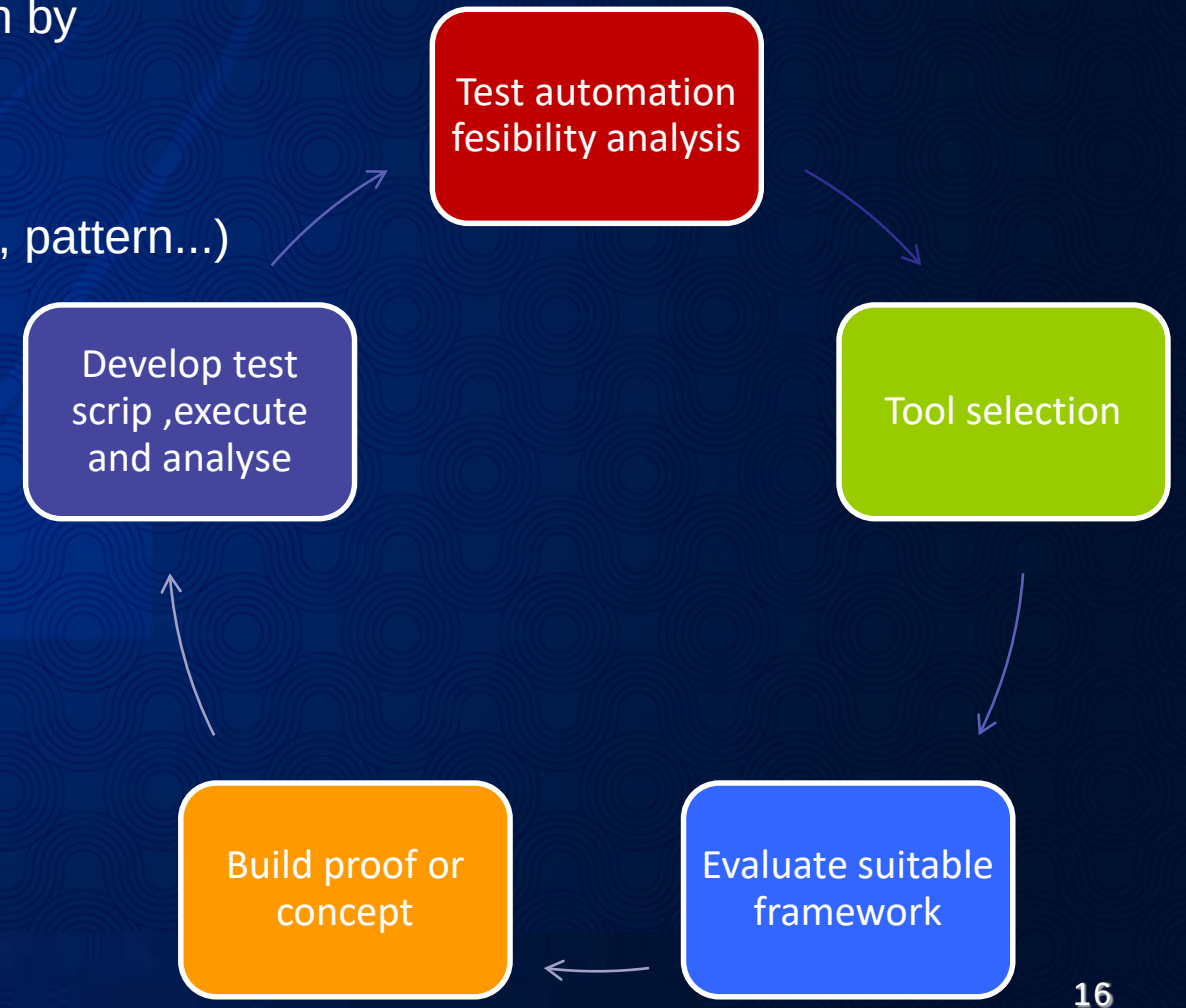
ITRI : Industrial Technology Research Institute

Application of POC ; Proof of Concept

POC application in IoT :

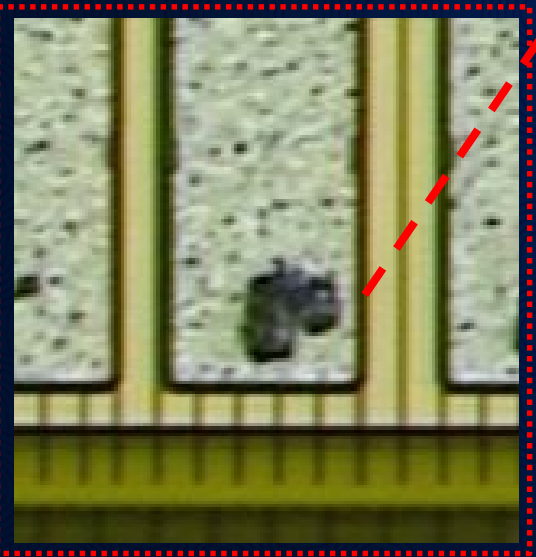
To make model for behavior of opeation will follow as expection by pciture or deductive method.

- Set operation prototype
- Use chart or image for related technologies (Framework , pattern...)
- Use SW to sminulate the solution and expected result
- Use UML syntax to set sketch of model for solution



Color image analysis

Margin Defect



480.jpg	3 μm
481.jpg	3 μm

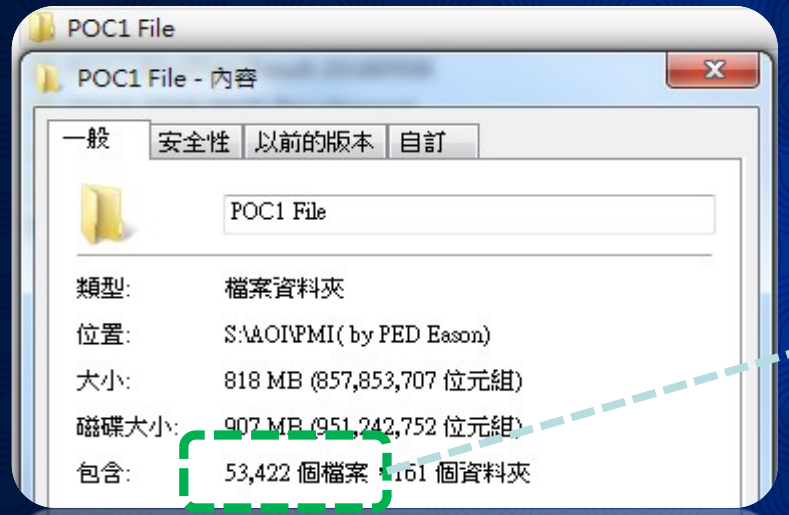
Particles defect

	744.png	Particle touch the line
1	747.png	Particle no touch the line
	748.png	Particle touch the line

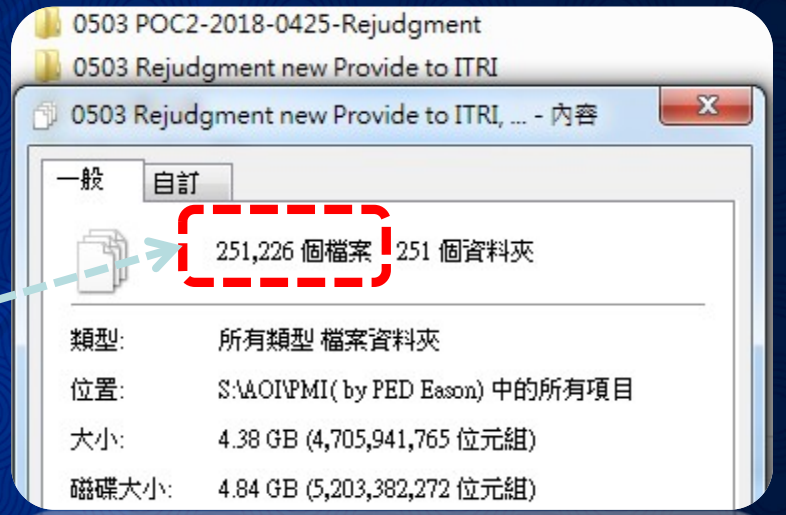
Margin & Particle was judged as No defect

Big Data Improves Accuracy Trends

POC1



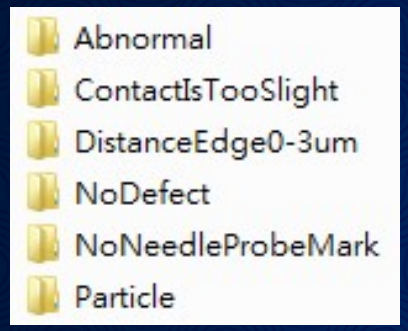
POC2



Increased image data & enhance teaching model

ITRI Verify Information (Phase2 – 2018/5/8)

UF3000

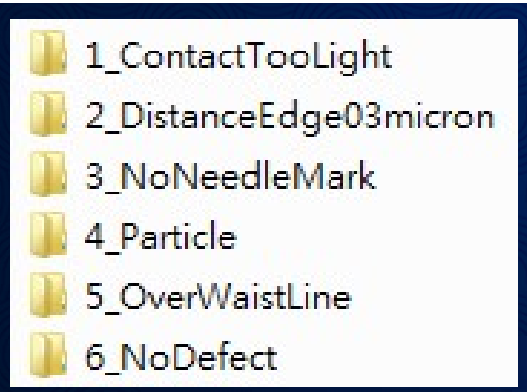


Judgment & Recognition Rate

100%

UF3000 (Black / White Image)			
Total: 300 ea image (6 Feature)			
Category	**Quantity**	**Misjudge**	**Classification correction**
Abnormal	10	0	0
Contact IsTooSlight	0	0	0
DistanceEdge0~3μm	150	0	0
No Defect	0	0	0
No Needle Mark	50	0	0
Particle	90	0	1
Each Quentity	300	0	1
Accuracy Calculate	100%		
Reinforce suggestions	Big Data		

UF3000EX



Judgment & Recognition Rate

98.1%

UF3000EX (Color Image)			
Total: 700 ea image (6 Feature)			
category	**Quantity**	**misjudge**	**Classification correction**
Contact IsTooSlight	100	2	33
DistanceEdge0~3μm	100	1	0
No Needle Mark	150	0	0
Particle	150	0	1
Over the middle waist line	59	6	4
No Defect	141	4	79
Each Quentity	700	13	117
Judgement Recognition rate	1.0		
Reinforce suggestions	Big Data ->> Over the middle waist line + Filtering No defects		

Follow on work

- ✓ How to enhance accuracy ?
- ✓ How to enhance the efficiency of AI processing ?
- ✓ Application for other process ?

How to enhance accuracy

✓ **Check item & complexity will impact accuracy of judgement**

Check items more will make rigorous condition in feature learning and cause accuracy dropping.

Check item	Database for teching	Accuracy of judgement
Particle (粉塵汙染)	2000 ~ 5000 pictures	99.8%
Scratches (刮痕)	2000 ~ 5000 pictures	99.8%
P/M shift (針偏)	2000 ~ 5000 pictures	99.8%
Any two check items	10000~ 30000 pictures	98%
Particle + Scratches + P/M shift	50000~ 100000 pictures	95%

How to enhance accuracy

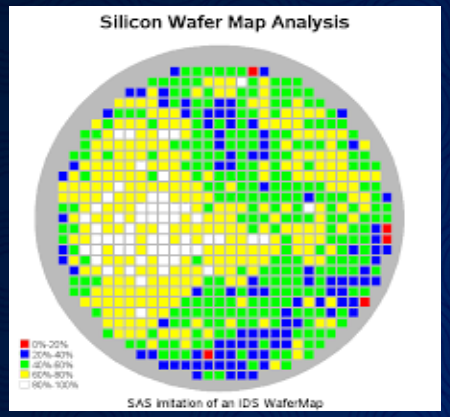
✓ **Image resolution 、color saturation and identification area will impact accuracy of judgement**

Pictures from different platform , instrument may have some difference. And it is better to set identification system (including database) by each platform.

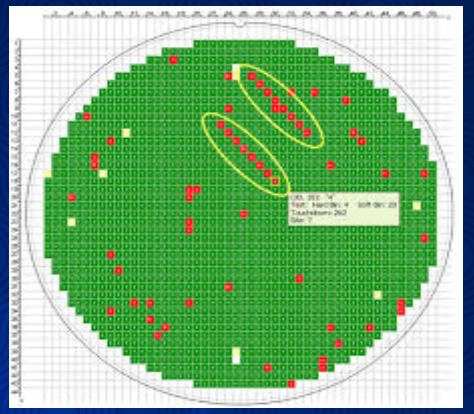
Color VS **Monochrome**

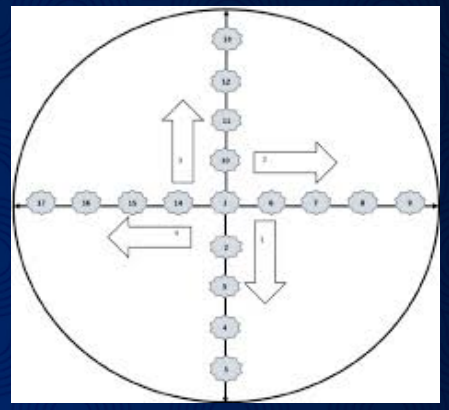
Monochrome VS **Monochrome**

Application for wafer map



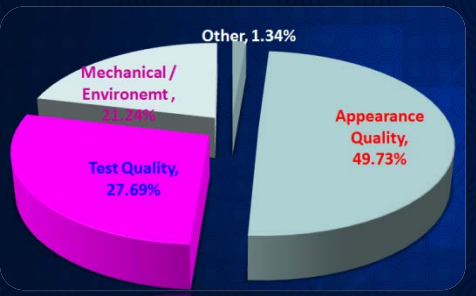
Object Detection
(machine learning)





Feature identification
(Algorithm analysis)

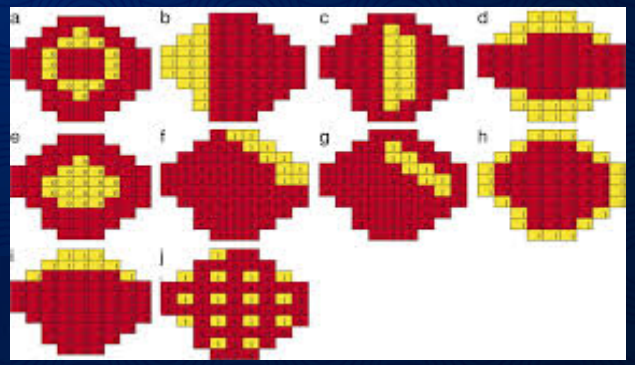
Map & SUB (Overkill) Analysis



Judge & Forecast

1. Pass (67%)
2. Defect Mode I (45%)
3. Defect Mode II (23%)

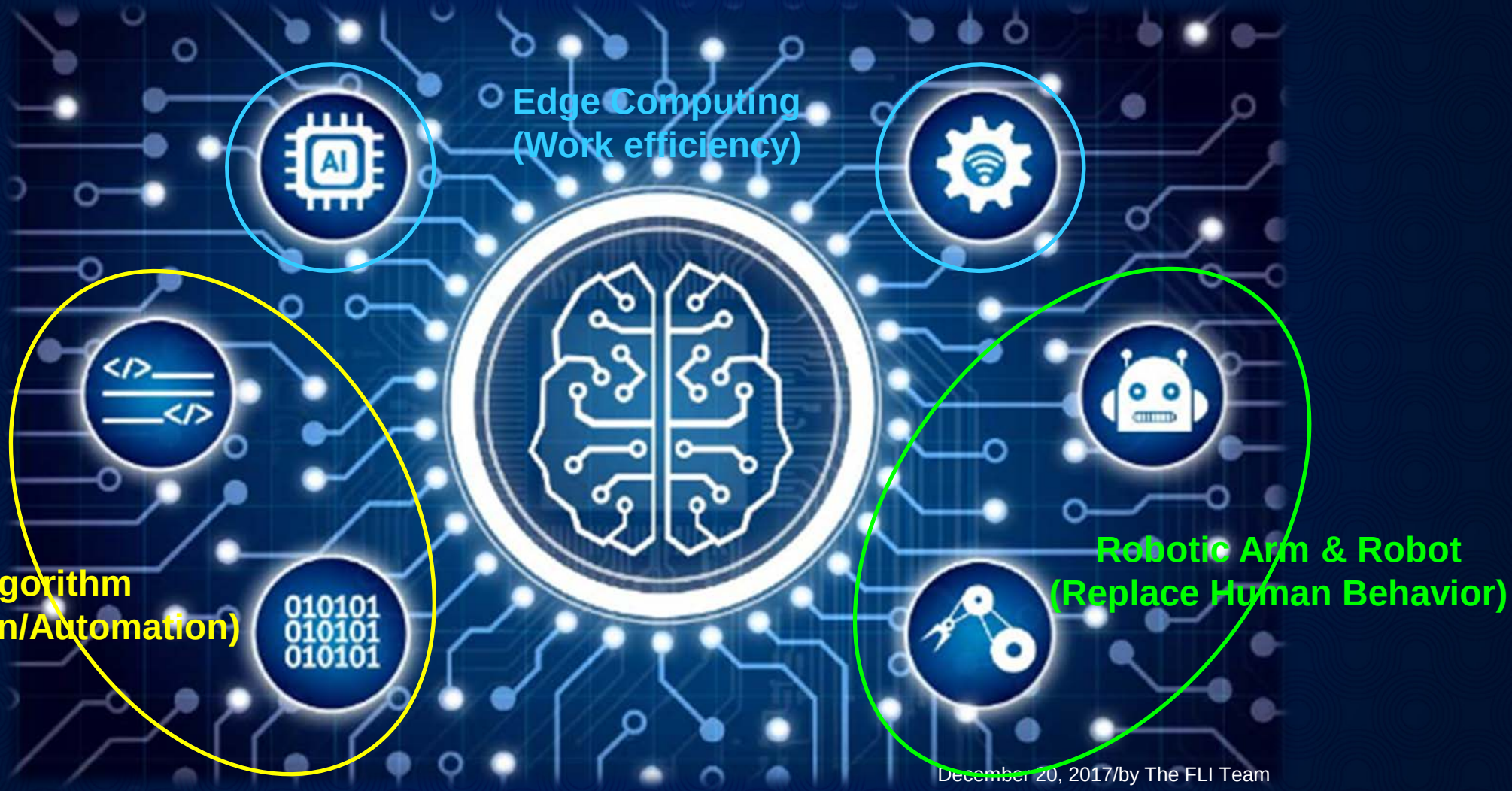
Similarity comparison
(Algorithm analysis)



Future Development (Next Generation OSAT)

- ✓ Integration of different technologies (Image Technology, Algorithm, Edge Computing, Robotic Arm & Robot) for innovation testing
- ✓ It is not pipe dream to dramatically drop production loading by AI development
- ✓ Industry 4.0 + AI will make real time & most efficient in production (Smart Manufacture)
- ✓ Quality level will keep enhancing due to real time disposition & less manual operation
- ✓ Accurate forecast make more benefit for enterprise

Elements of AI



Wafer Level Efficient Testing of MRAM

Siamak SALIMY, Ph.D. – Chief Technical Officer

Hantsun CHUNG – Sales & Application Manager

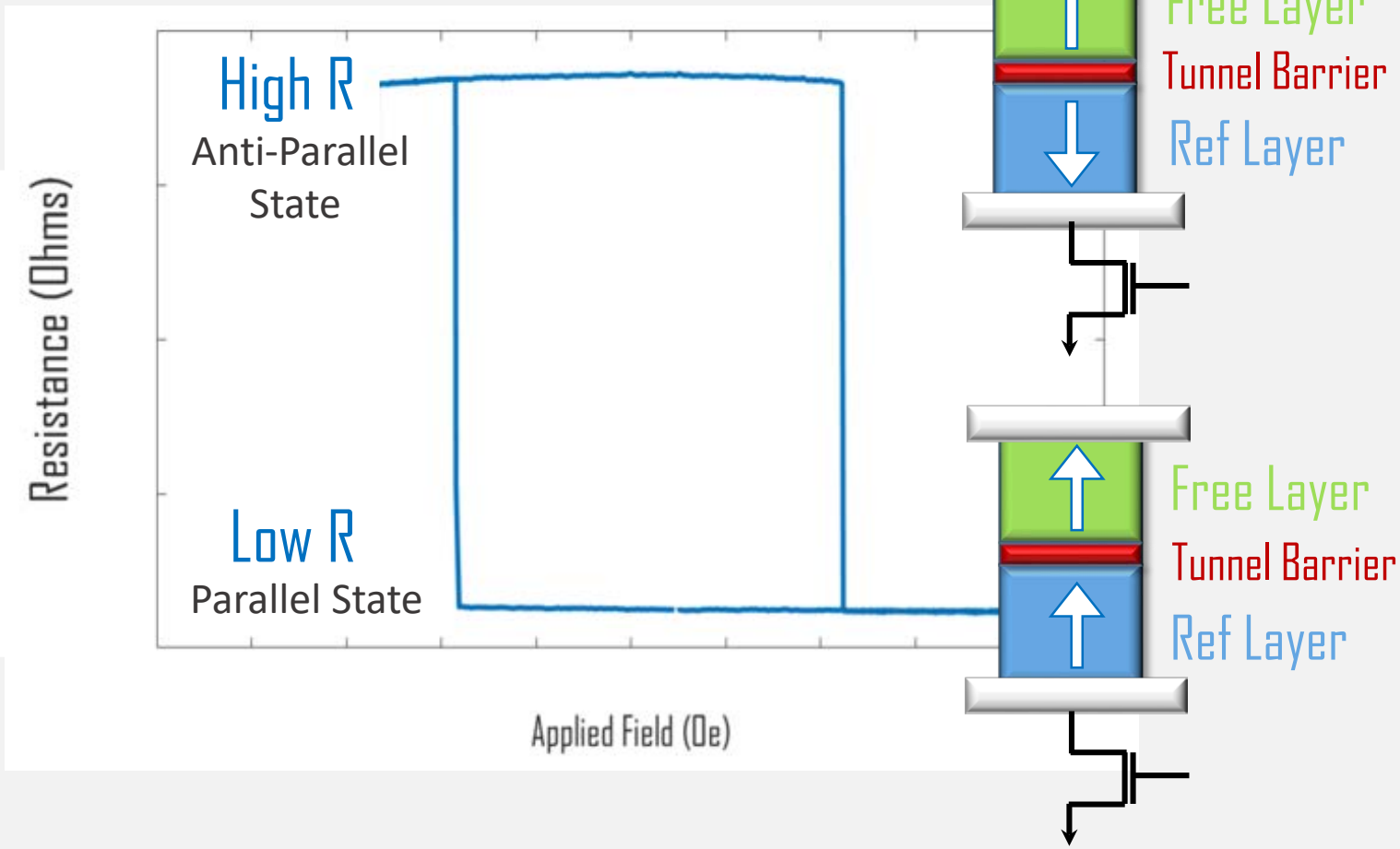
Taiwan, October 18-19, 2018

The top class properties of MRAM

High Performances: DRAM like write perf.

- Non-Volatile
- Fast Read/Write : DRAM&SRAM like
- Scalable at low technology nodes
- Data requires no refresh

Bi-state magnetic device
Switching with current pulses



Flying for many applications

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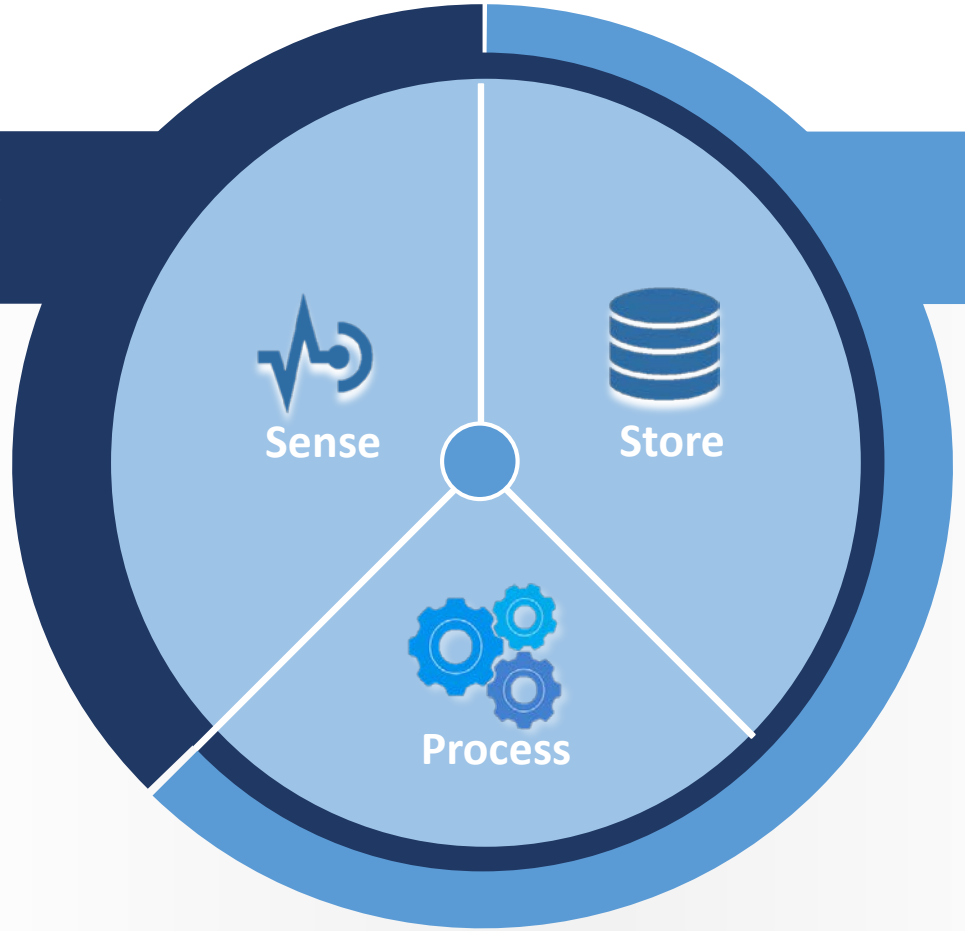
High Density

- Nomad applications
- Encryption and ECU
- Mobile Phone



Low Latency

- Data Center Buffer
- Low Level Cache Memory
- Persistent memory for sensors and wearables

Driven by Internet of Things, Artificial Intelligence and Big Data

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Hprobe

Overview

Magnetic Automated Test Equipment

3D	Magnetic Generator	High Field Amplitude Ultra-Fast Sweeping
MTJ	Parametric Tester	MRAM Sensors
SoC	Functional Tester	Full ATE integration Memory Tester

Hprobe is spin-off company of spintec SPIN IN ELECTRONICS

Hprobe Magnetic Tool Application

MTJ Formation

FEOL

Tunnel Ox

Metal Dep

Magnetic Dep

Blanket Test

P-MOKE

MTJ Etch

Pad

Initialization

DUT/Wafer Initialization

WAT/PCM Parametric

Device Test

Packaging

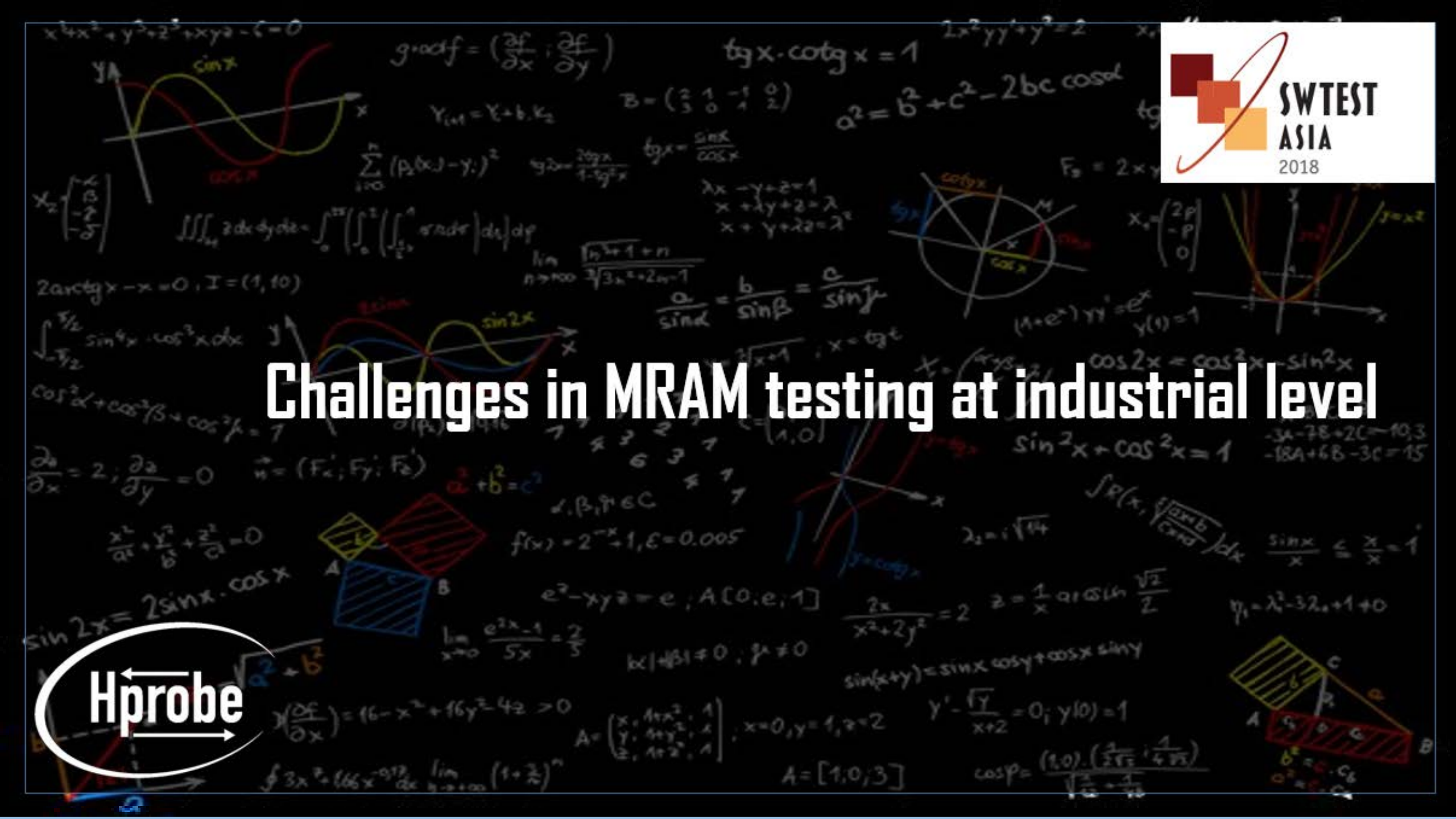
SoC Test

WS/Binning Functional

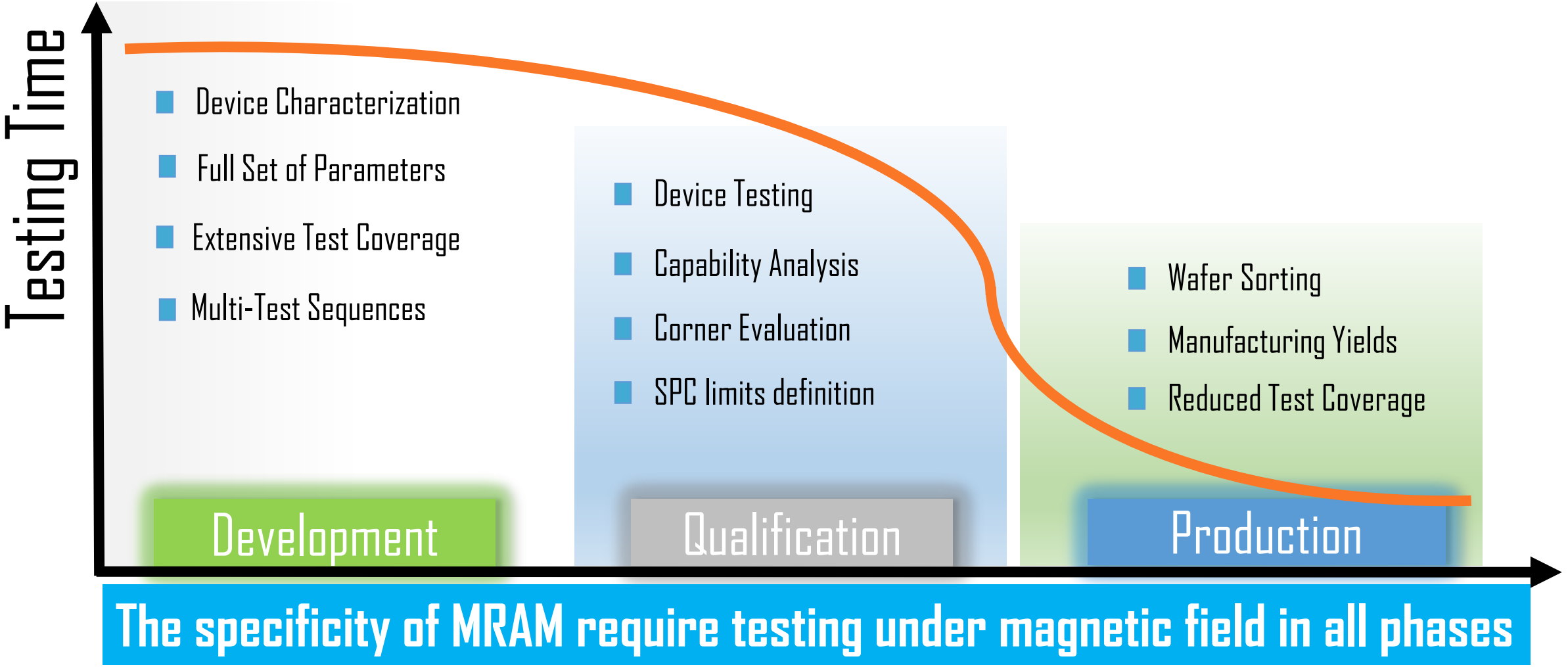
Final Test

Clients

- Foundries
- Integrated Device Manufacturer
- Original Equipment Manufacturer
- Research Lab and Institute


SWTEST
ASIA
2018
Challenges in MRAM testing at industrial level
Hprobe

From Development To Production



How to test MRAM devices ?

Under Magnetic Field

- Sweeping Magnetic field in perpendicular direction up to 0.5 Tesla (FL switching)
- Extracting the switching field, switching probability and energy barrier

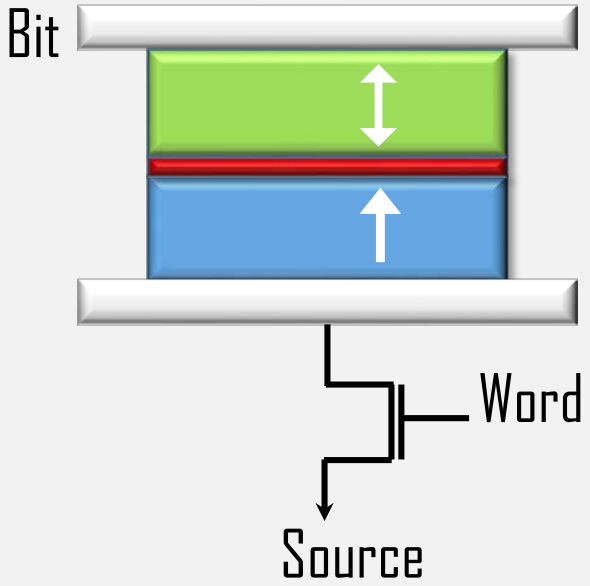
Challenge: High Field with Fast Amplitude Sweeping

With Ultra Narrow Voltage Pulses

- Sweeping Voltage Pulsed Amplitude down to 200psec at 2.5V
- Extracting the switching probability vs pulsing parameters

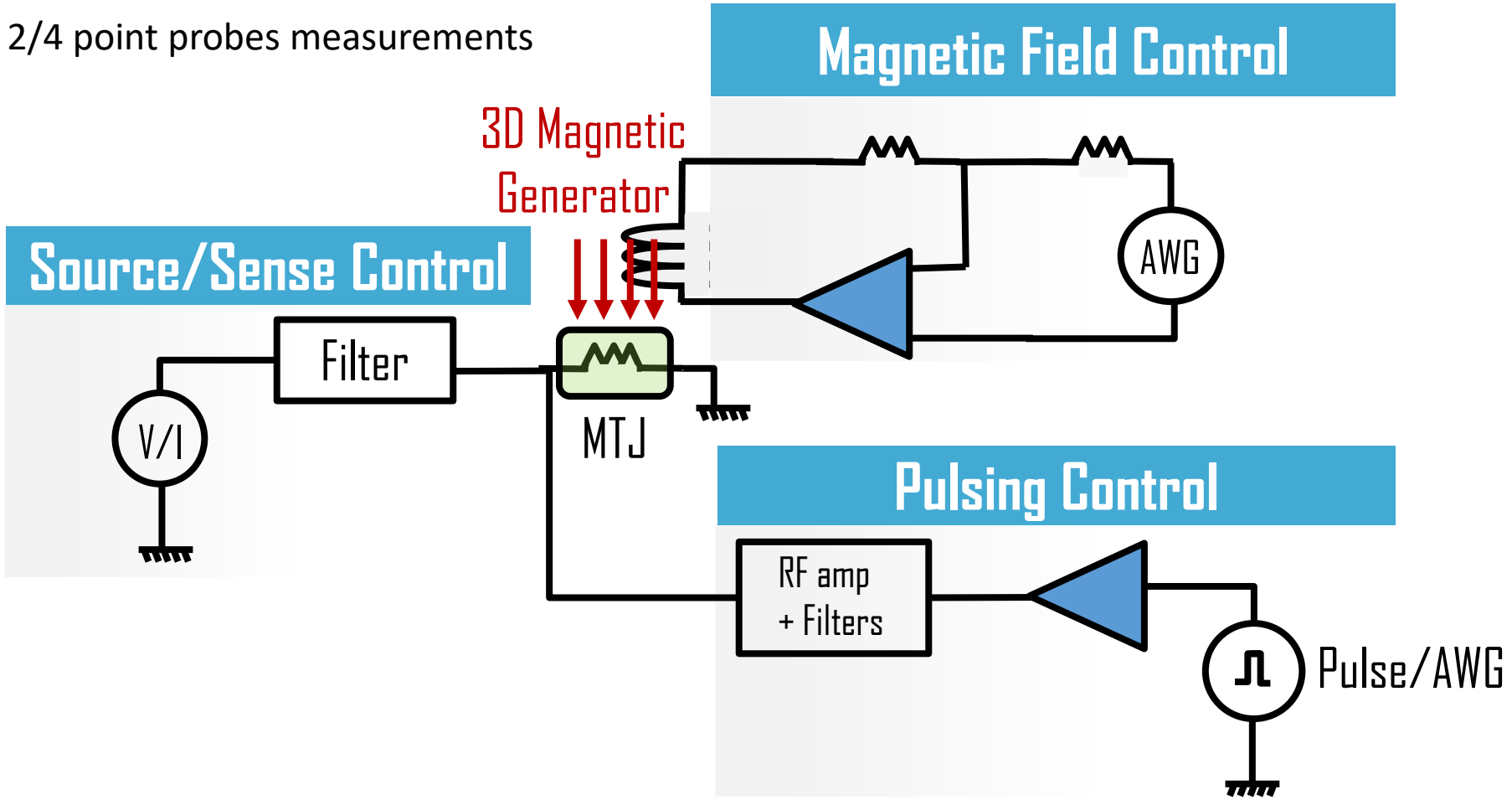
Challenge: Sweep Fast Amplitude of Ultra-Narrow Pulse Width

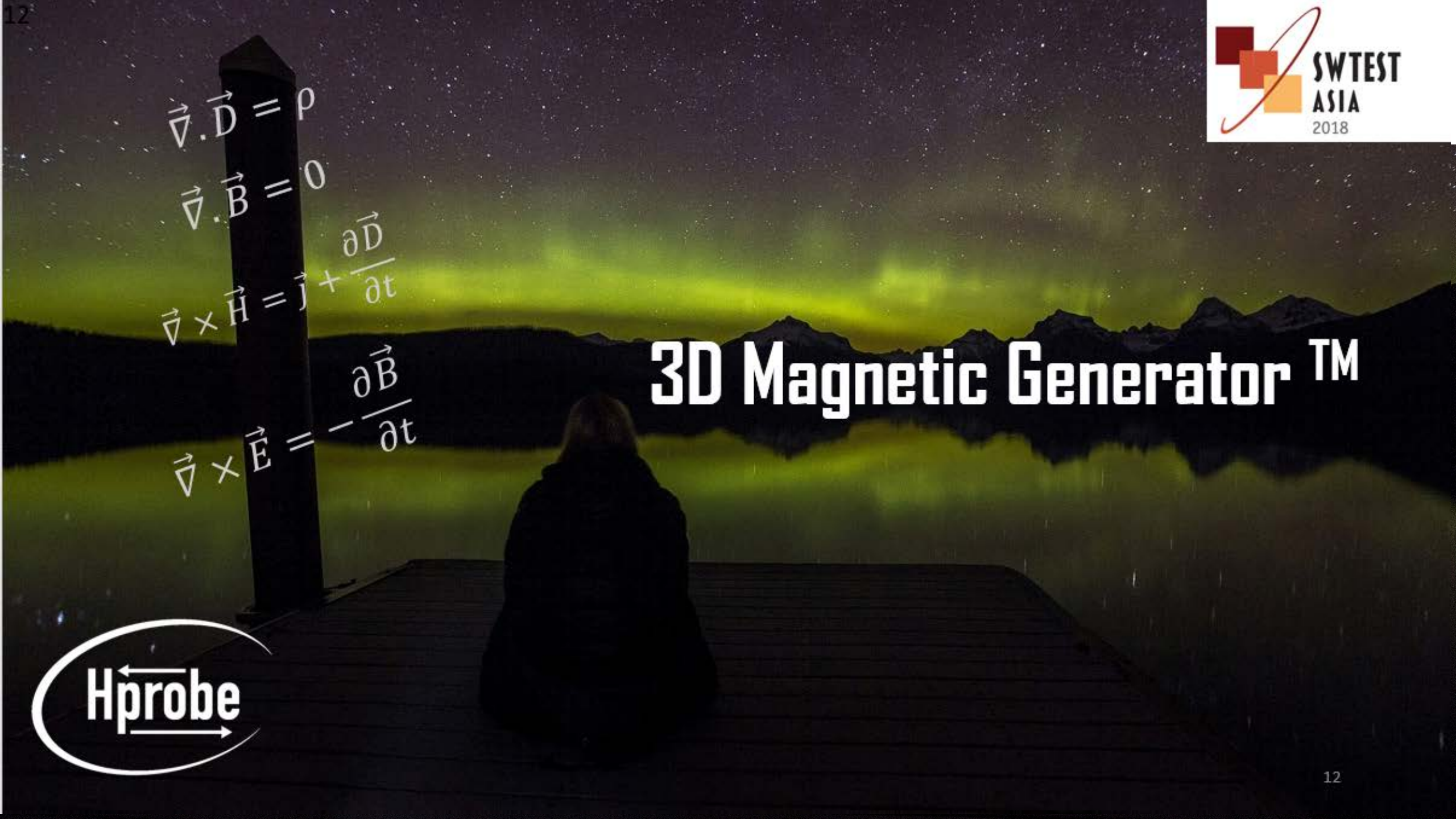
STT-MRAM



Proposed Setup for MRAM Parametric Testing

- RF path down to the probe on pulsing side
- Probing done by 2/4 point probes measurements





3D Magnetic Generator ™

SWTEST ASIA 2018

Hprobe

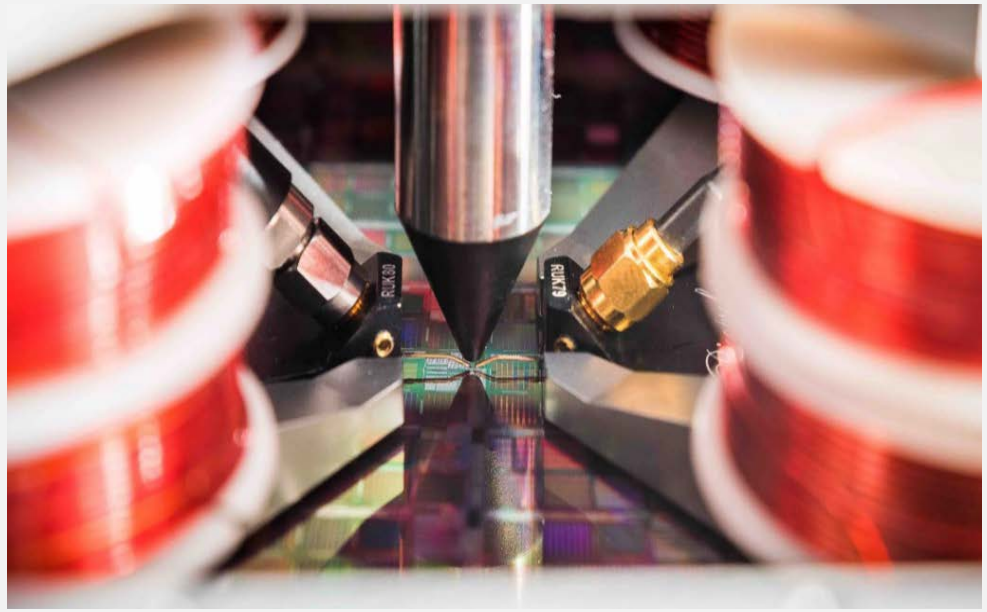
Magnetic Field Generation

	Supra conductors	Standard Coils	Permanent Magnets	Hybrid Ferro Magnets + Coils
Field Amplitude	HIGH	LOW	LOW	HIGH
Sweep Speed	LOW	HIGH	LOW	HIGH
Heating	HIGH	HIGH	LOW	LOW

Hprobe Magnetic Generator ™

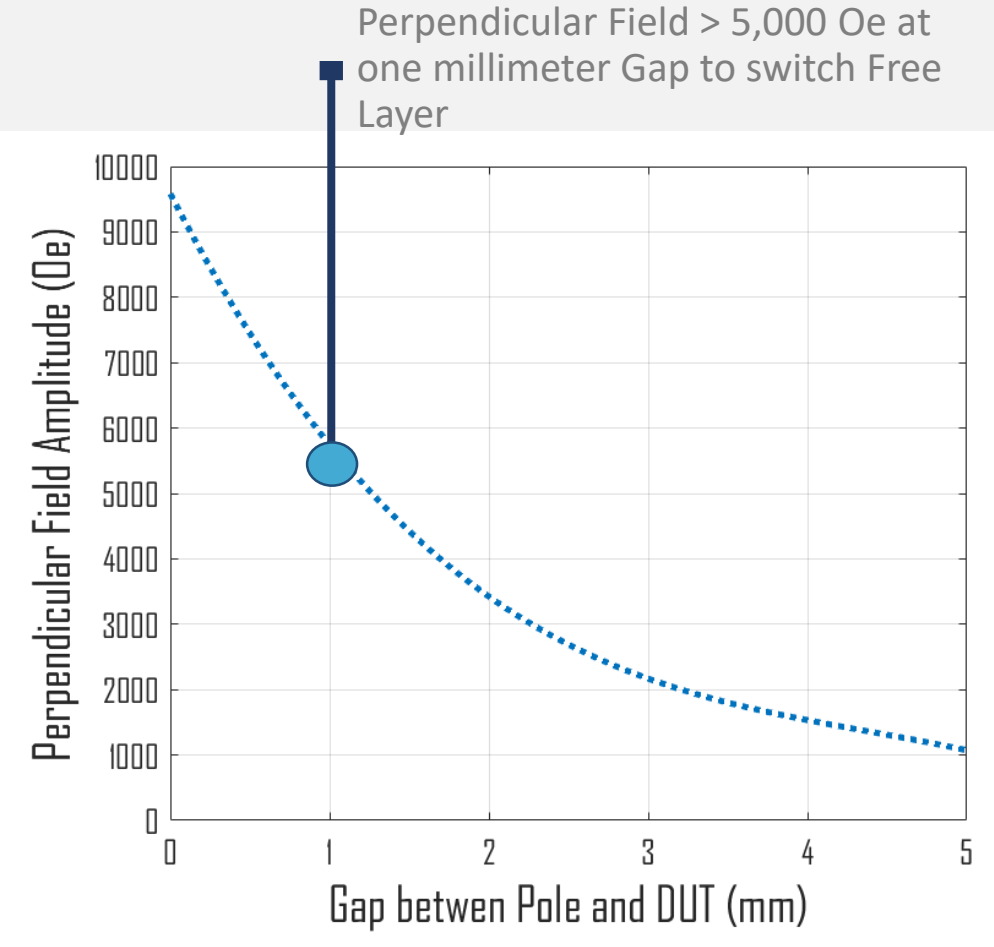
- Full 3D Magnetic Field
- Single Axis Field
- Rotating Field
- Perpendicular Field up to 750mT
- Planar Field up to 350mT
- No liquid cooling system

Unique Patented Design

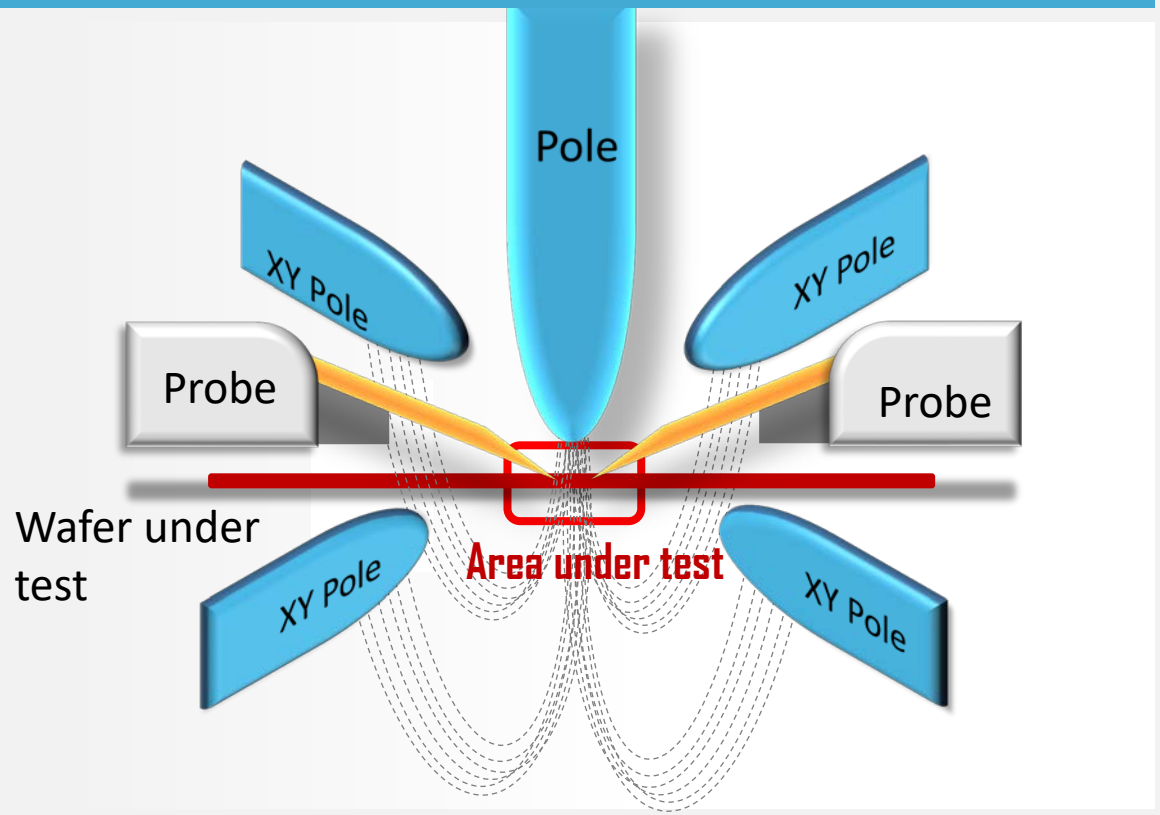


Controllable Field Over the 3 Directions of Space

Out of Plane Field



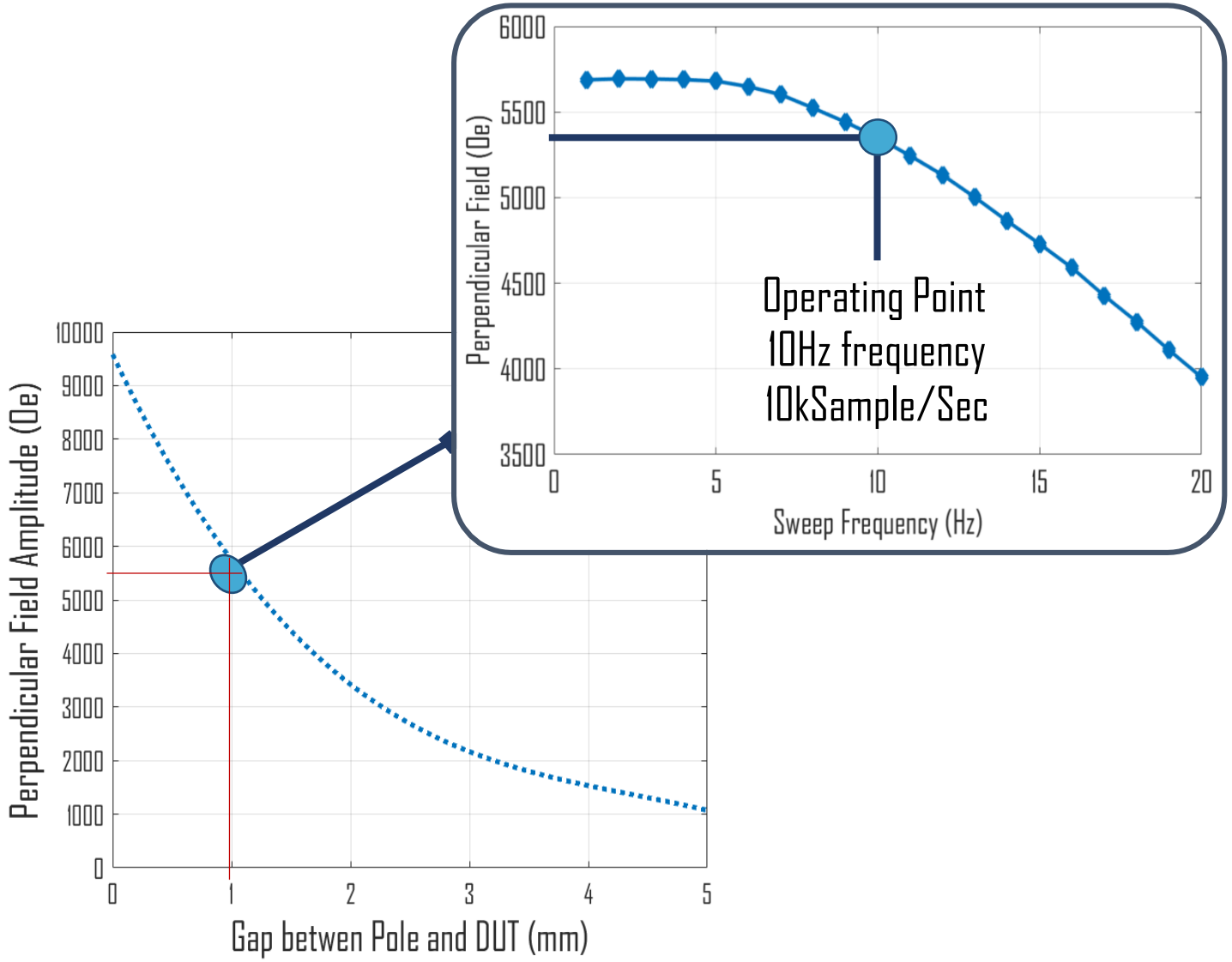
Perpendicular Configuration



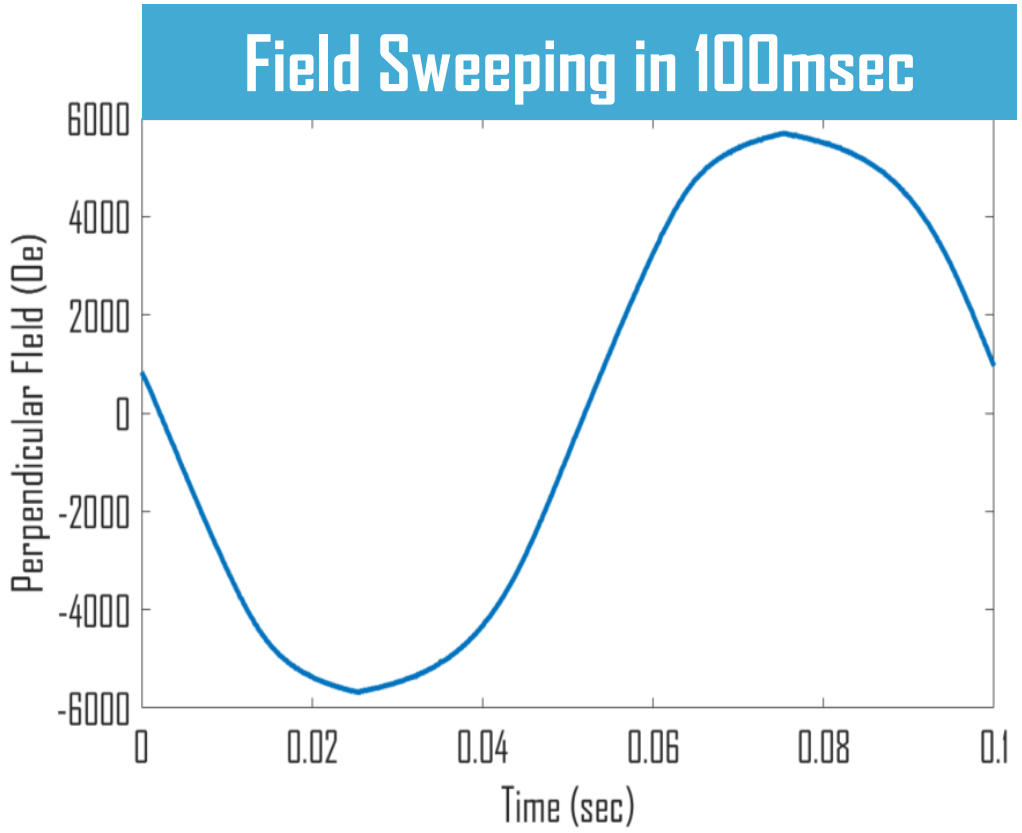
Magnetic field lines

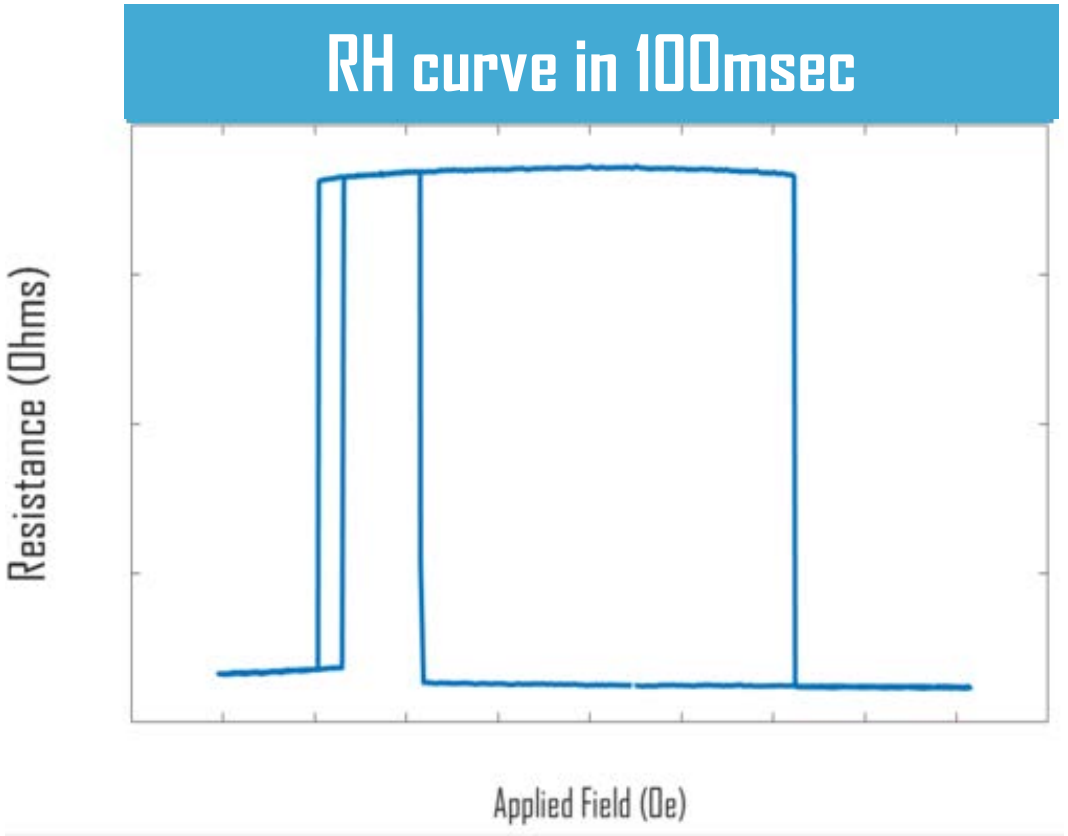
Fast Field Sweeping Capability

- Variable Sweeping Rate
- Synchronized Measurement of MTJ resistance at each field steps
- Fast sweeping in any field configuration



Ultra-Fast Field Sweeping

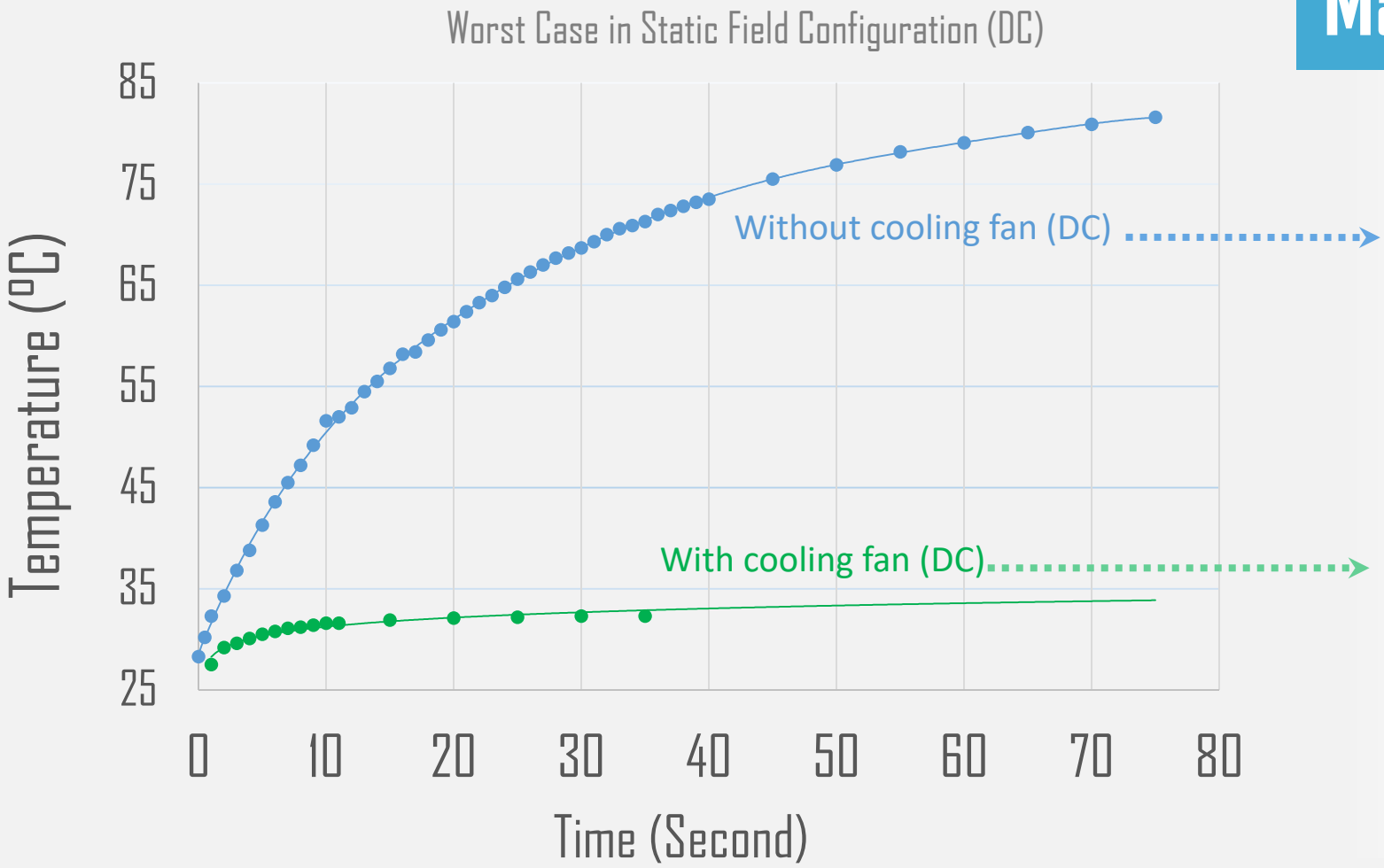


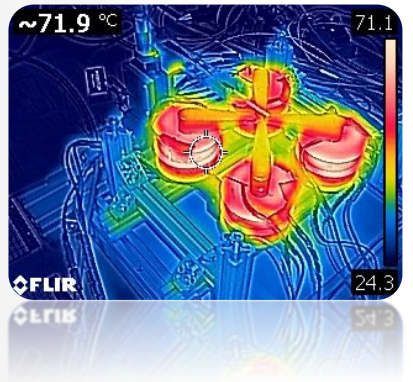


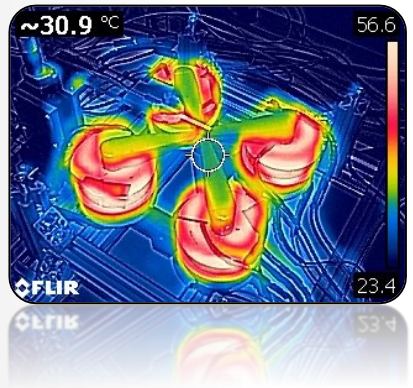
Full R-H sweeping curve in down to 50msec per MTJ

Temperature

Magnet Heating







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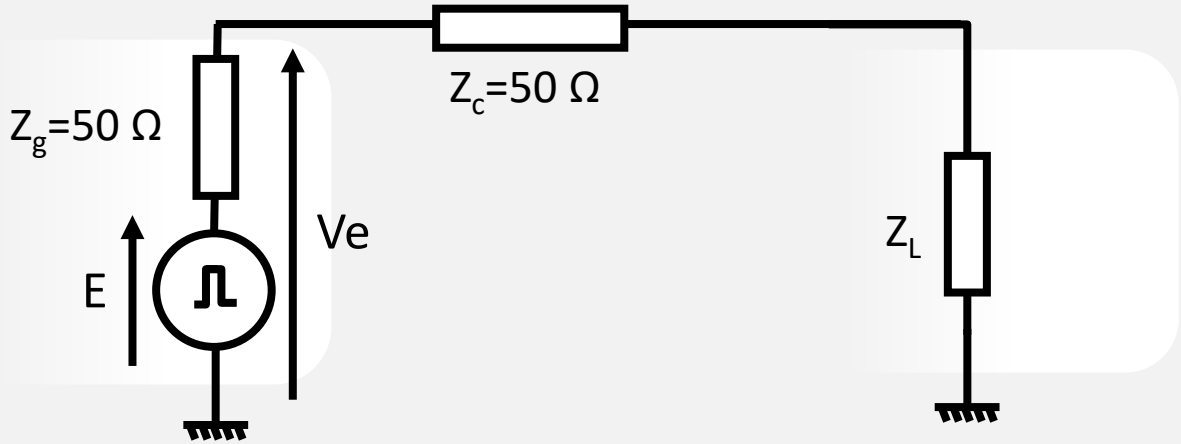
RF Ultra Fast Pulsing Channels

Hprobe

Options To Generate Ultra-Narrow Pulsed Width

	Pros.	Cons.
Pulse Generator	Amplitude > 2.5V Bipolar on 50Ω load	No sweep Amplitude Capability Need to activate mechanical relay at output to sweep amplitude
RF AWG	Ultra-Fast Amplitude Sweeping	Amplitude Limited to <+/-1V on 50Ω load

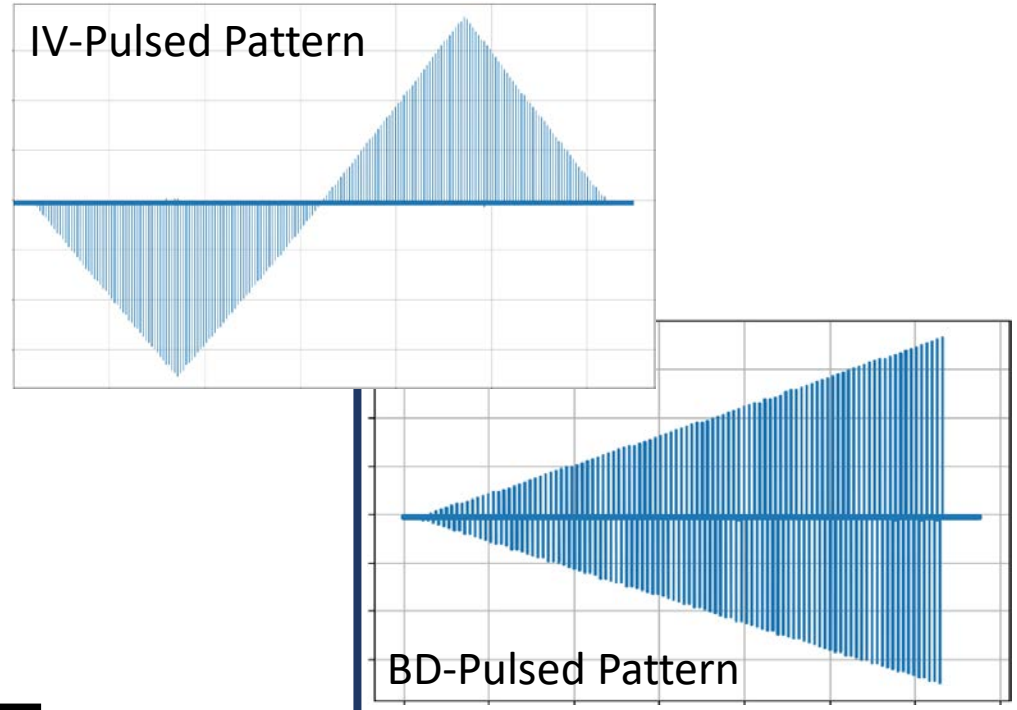


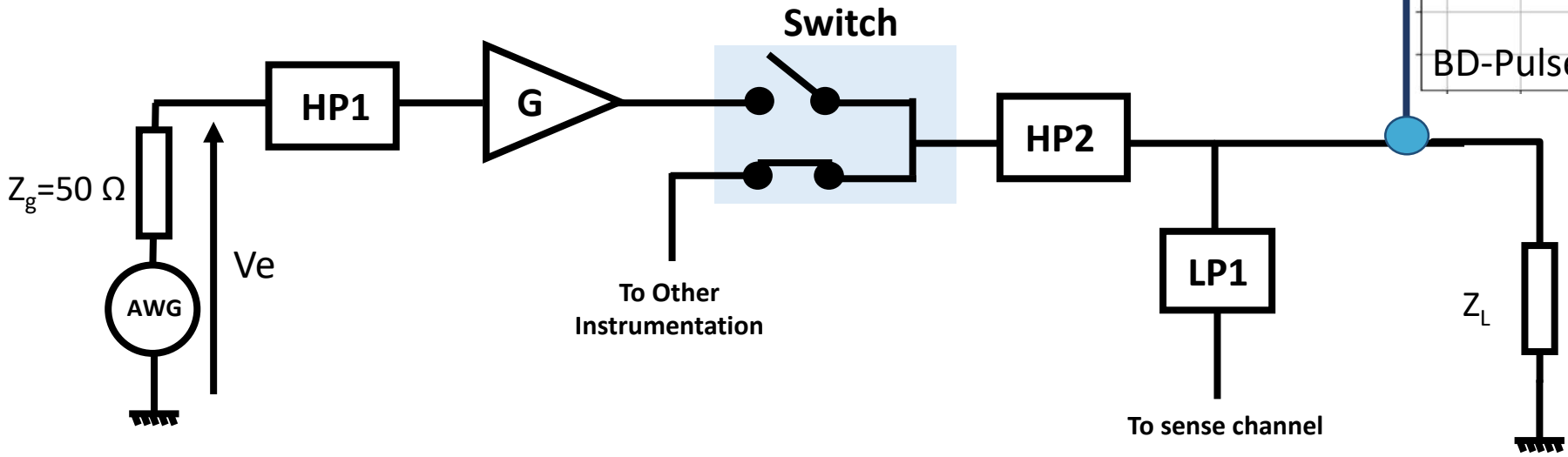
$$Ve = E.\frac{Zc}{Zc + Zg} = \frac{E}{2}$$

Choice of RF ultra-Fast AWG

Design of the RF path down to the DUT

- Bandwidth > 6 GHz
- Amplitude of +/-2.5V Bipolar
- Pulse Width down to 200psec





Pulsed Shape at PW of 10nsec and 200psec

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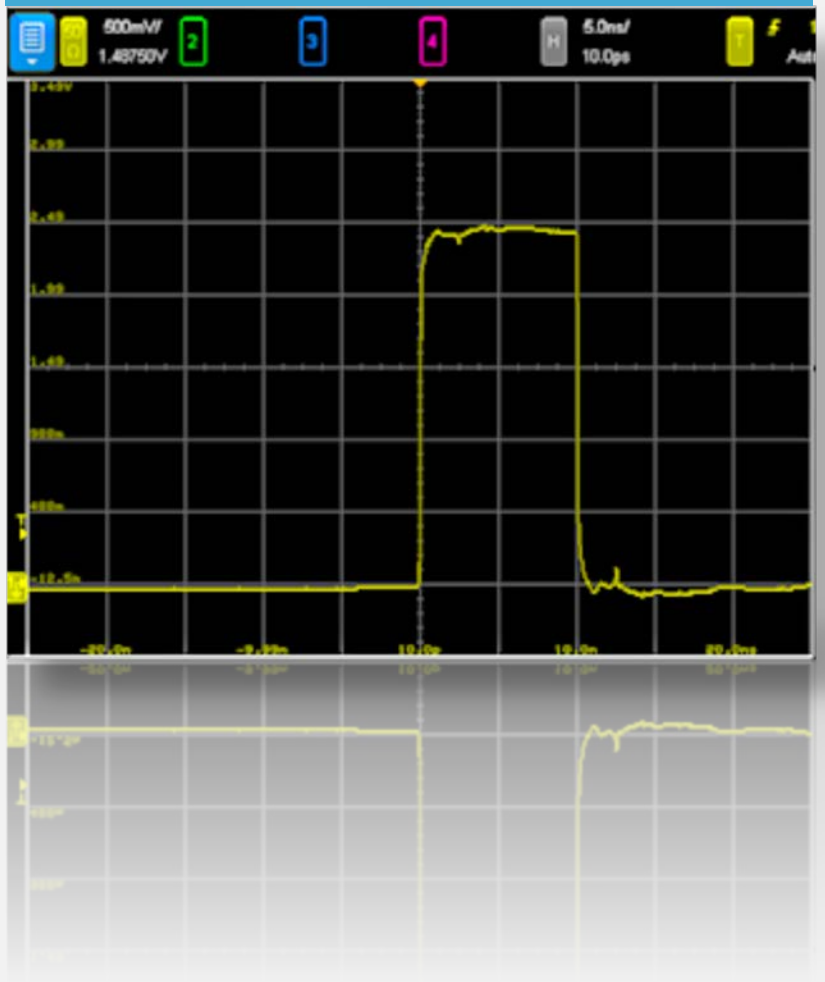
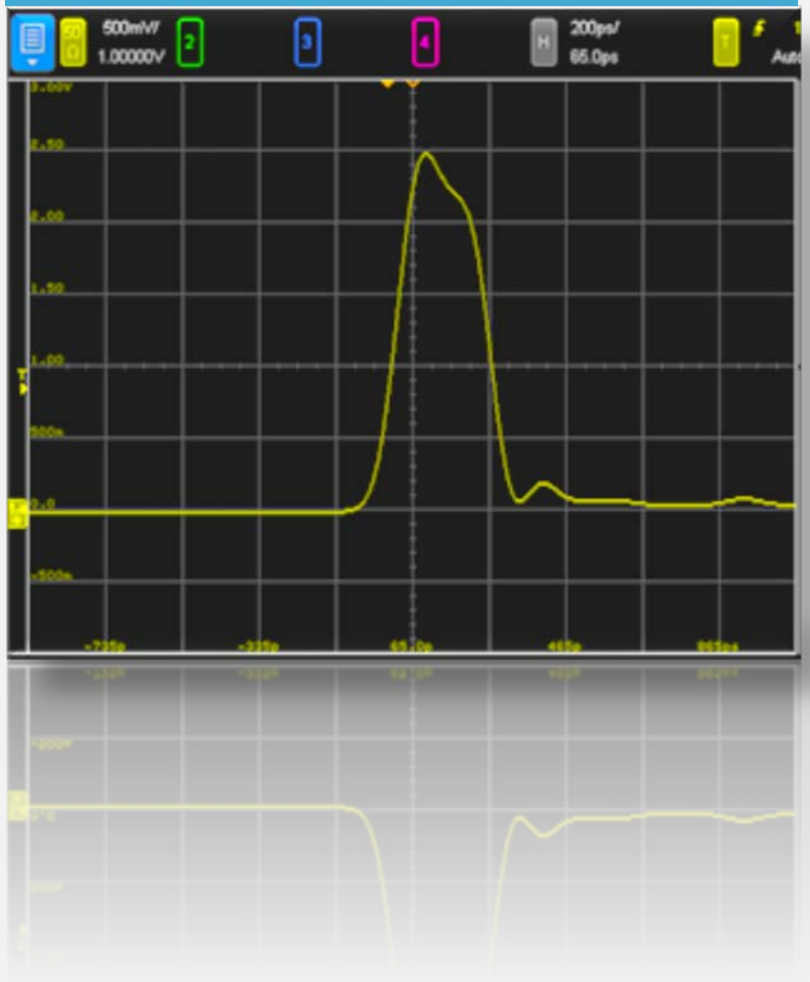
10nsec @ 2.5V



200psec @ 2.5V



Summary

Designed of a Test System for wafer level testing under magnetic field for MRAM devices

- With High perpendicular field (>500mT) and ultra-fast sweeping capability 10kSa/sec
- Large bandwidth, fast amplitude sweeping and pulsing capability down to 200psec
- Compatible with all phases from development to production of integrated magnetic devices

Hprobe

Speed Up Magnetic Testing

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Thank You

Contributors

Hprobe

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- Laurent LEBRUN
- Jean-Pierre NOZIERES

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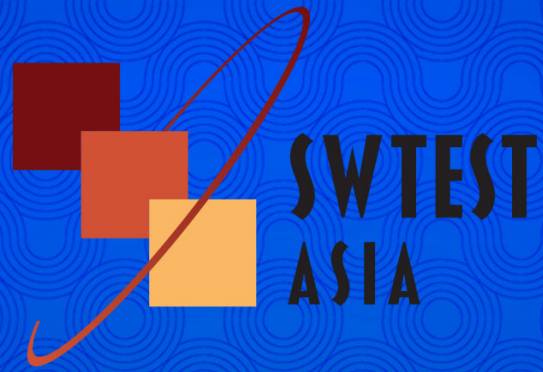
- Isabelle JOUMARD
- Antoine CHAVANT
- Ricardo SOUSA

HTSi Hermes Testing Solutions Inc.

- Lambert LAI
- Elva CHANG

Taiwan, October 18-19 2018



Overcoming Challenges for 5G Production Tests

Choon Beng Sia Ph.D.

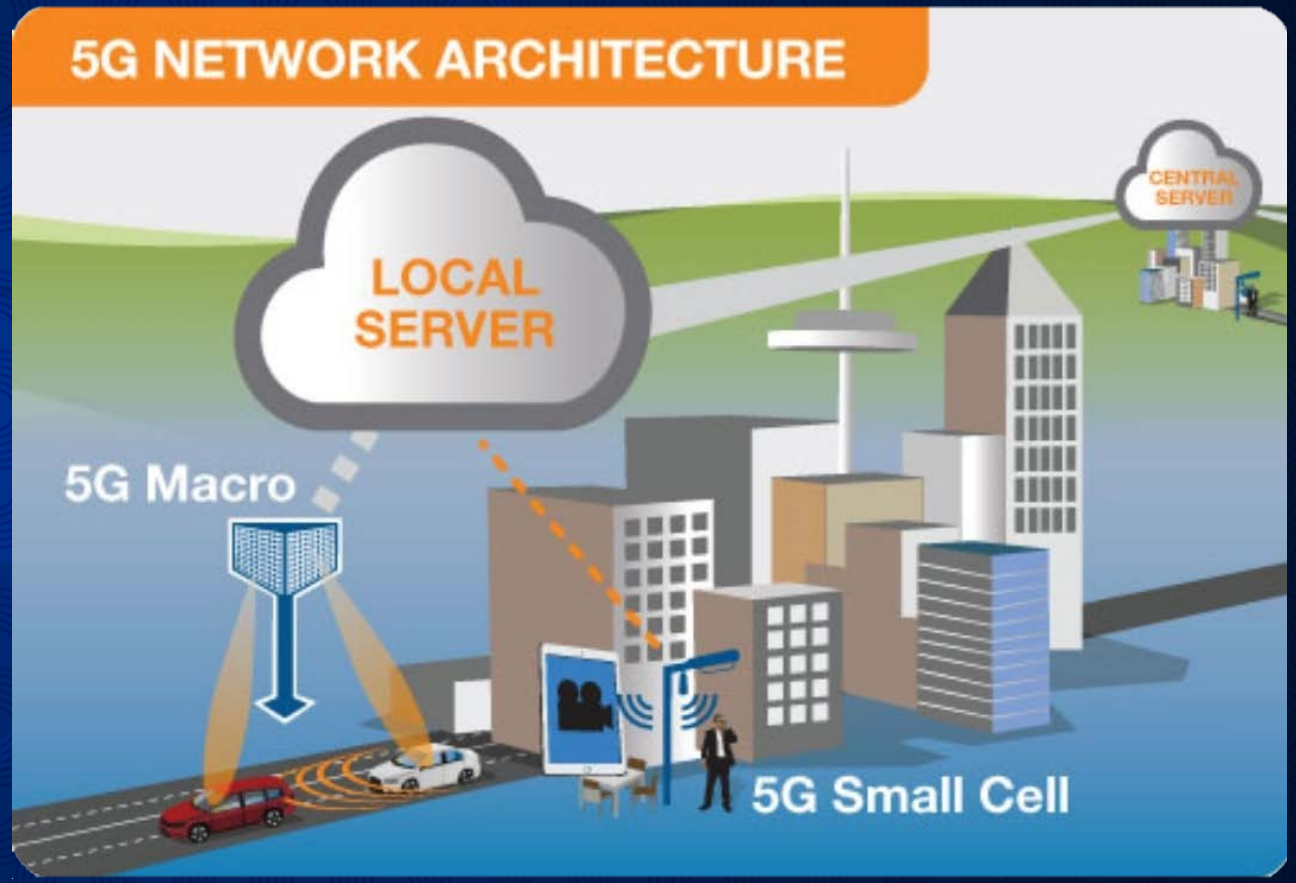
Taiwan, October 18-19, 2018

Overview

- **What is 5G?**
- **Economic Impacts of 5G**
- **Key Challenges for 5G Production Tests**
  - Handling Large Number of RF Test Channels
  - Ensuring Excellent Signal Integrity
- **Possible Solutions**
  - In-membrane Antenna OTA Tests
  - Dedicated Calibration Substrate & Power Calibration
- **Summary**
- **Acknowledgements**

What is 5G?

- **Communication Network for 4th Industrial Revolution**
  - 5G RF, Optical, High Speed Digital
- **Extremely Fast Data Rates**
  - 10Gbps (5G) vs 100Mbps (4G)
- **Ultra Low Latency**
  - 1ms (5G) vs 50ms (4G)
- **Huge No. of Connections**
  - 100 billion (5G) vs 1000 (4G)
- **Higher Energy Efficiency**
  - Always Stay Connected
- **Connect Everyone, Everything**



Sources: https://www.quora.com/What-is-5G-Will-5G-technology-bring-new-dimensions-to-wireless ; http://www.emfexplained.info/?ID=25916 ; https://en.wikipedia.org/wiki/Fourth_Industrial_Revolution

5G Use Cases

- **Enhanced Mobile Broadband**
  - Enterprise/Team Collaborations, AR/VR, Enhanced Wireless Broadband, Education, Mobile Computing, Enhanced Digital Signage.
- **Massive Internet of Things (MIoT)**
  - Smart Cities, Energy/Utility Monitoring, Asset Tracking, Smart Agriculture, Physical Infrastructure, Smart Homes, Remote Monitoring, Beacons & Connected Shoppers.

- **Mission Critical Services (Low Latency Requirement)**
  - Autonomous Vehicles, Remote Patient monitoring/TeleHealth, Industrial Automation, Smart Grid, Drones.
    - 4G - braking command makes a car at 100kmph to stop after 1.4m.
    - 5G - Same car stops within 2.8cm due to ultra low latency.

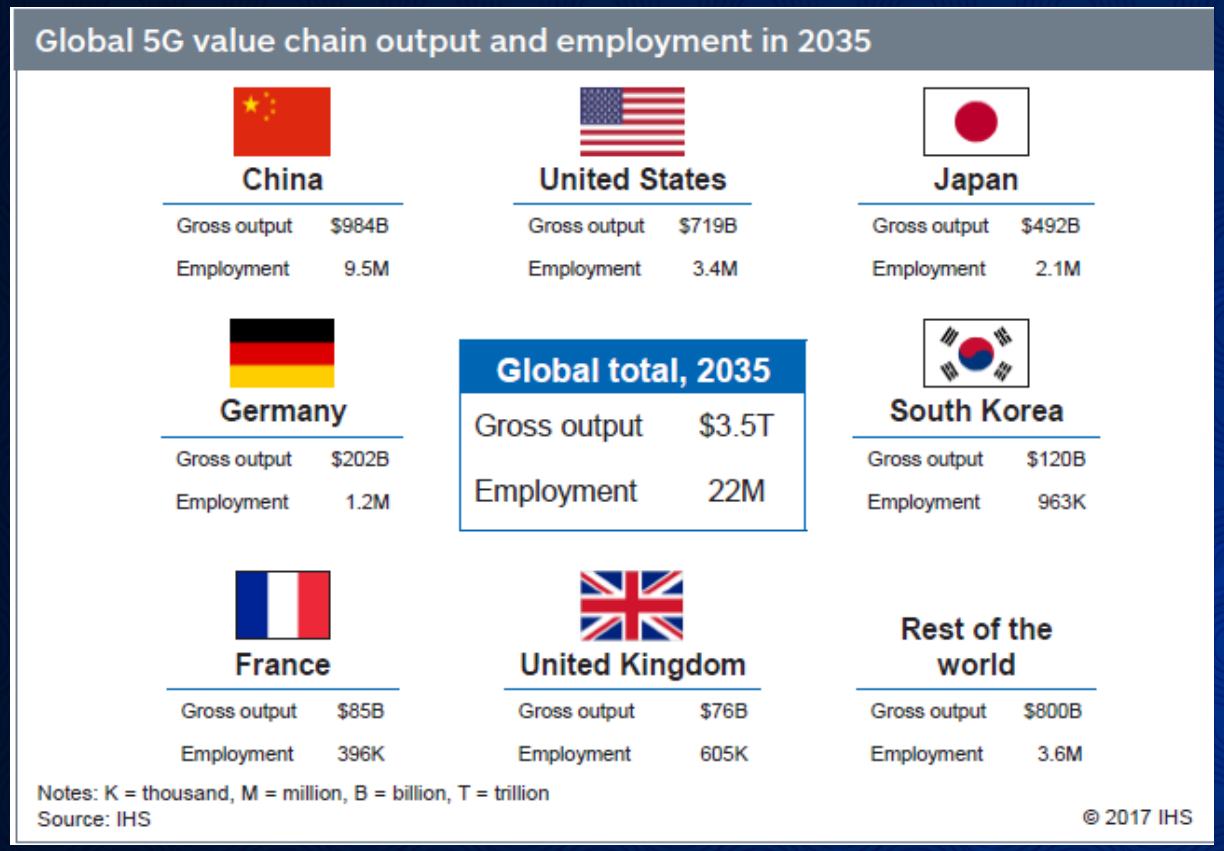
Source: The 5G Economy: How 5G Technology will contribute to the Global Economy, Jan 2017 for Qualcomm
https://www.independent.ie/business/technology/news/the-need-for-speed-is-ireland-ready-for-5g-the-next-big-thing-in-cellular-technology-36629260.html

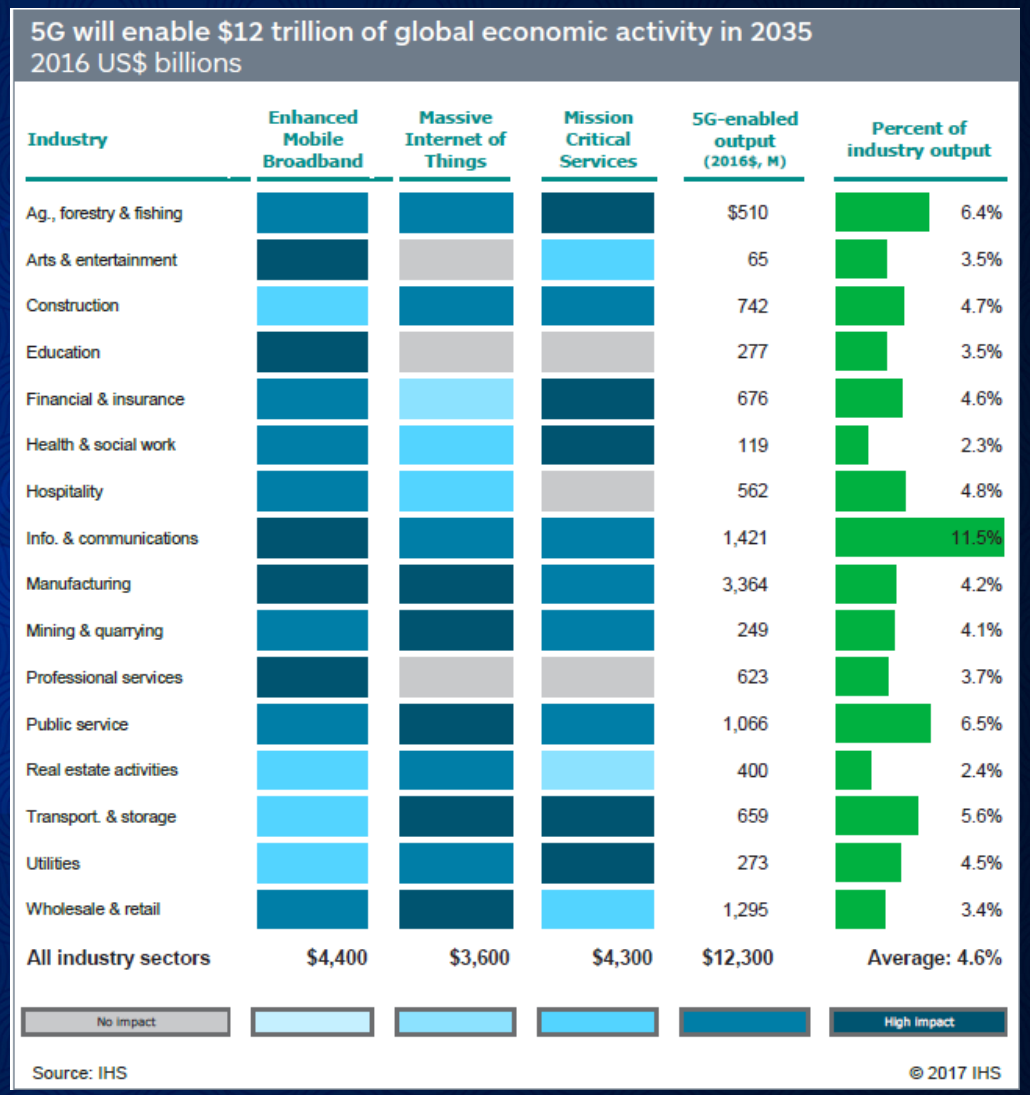
Economic Impacts of 5G (USA)

- **5G → 3 million jobs, US$275B investments, US$500B economic growth**
- **Smart Cities**
  - US$160B in savings - ↓ Energy Use & ↓ Congestion.
  - Eg. Sensors monitor Health & Safety of critical infrastructure - Buildings, Roads & Bridges.
- **Transportation**
  - Self-driving cars ↓ 90% emissions, ↓ 40% Travel Time & Save 22,000 lives annually.
  - 5G will save US$450B annually in transportation costs.
- **Healthcare**
  - Remote Patient Monitoring & Surgery through connected healthcare devices
  - US$305B in Healthcare Cost-savings Annually.
- **Energy**
  - 5G allow Energy Grid to be more Accurately Monitored, Improving Management, Reducing Costs, adding US$1.8 trillion in revenue to the U.S. economy.

Source: https://www.ctia.org/the-wireless-industry/the-race-to-5g, Accenture

Economic Impacts of 5G (World)





- **By 2035, Value Chain US$3.5T, 20M Jobs**
- **CEO Qualcomm, "5G Impact similar to Introduction of Electricity or Automobile"**

Source: Prepared by IHS, The 5G Economy: How 5G Technology will contribute to the Global Economy, Jan 2017 for Qualcomm Inc.

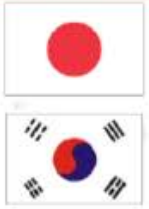
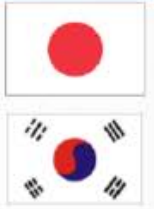
Global Race to 5G

- **5G Readiness Index**
  - Spectrum Availability
  - Infrastructure Planning
- **CTIA, consortium representing U.S. Wireless Communications Industry**
  - 250 companies

Ranking based on 5G Readiness Index

Source: Analysys Mason Report April 2018 @ https://www.ctia.org/the-wireless-industry/the-race-to-5g

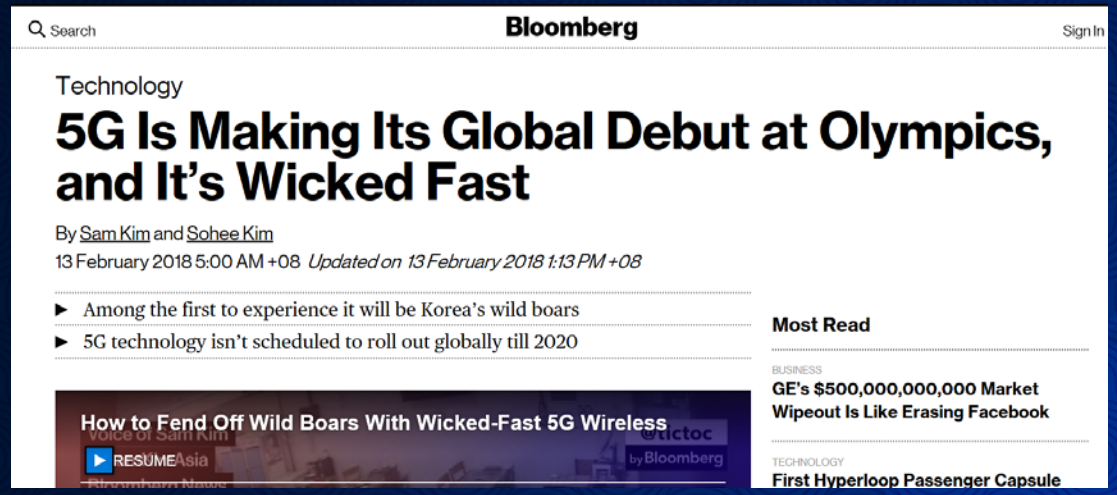
Global Race to 5G

	sub-6GHz						mmWave		
Spectrum	0.6GHz	2.5GHz	3.4 – 3.7GHz			4.4 – 4.9GHz	28GHz		39GHz
GEOGRAPHY									
CARRIERS	T-Mobile	Sprint	Orange Vodafone	China Mobile	NTT DoCoMo SK KT	NTT DoCoMo SoftBank	Verizon AT&T T-Mobile	NTT DoCoMo SoftBank SK | KT	Verizon AT&T T-Mobile
COMMERCIAL SERVICES	2019	Late '19	TBD	2020	2020	Mid-2020	2H18	2020+	2H18

- 2020 appears to be commercialization target for 5G
- Focus on Sub-6GHz, Expect Challenges in mmW Tests

Source:- Keysight World 5G Presentation, Shanghai June 2018

5G Field Trials



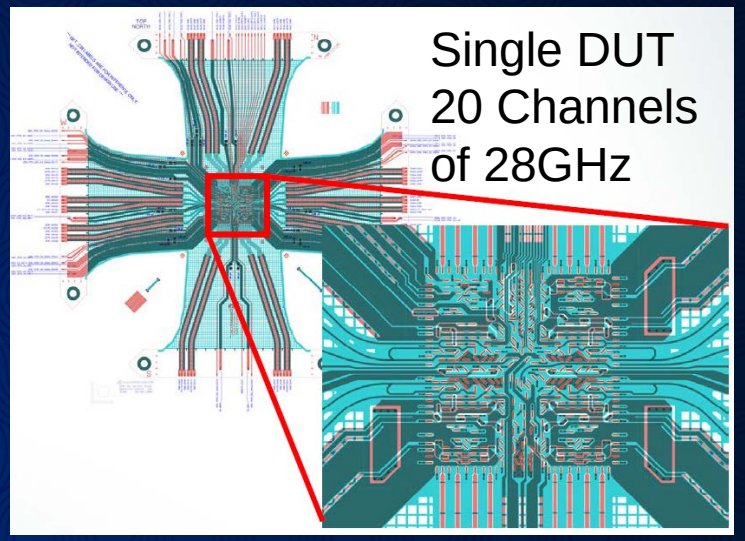
- **Intel & NTT Docomo 5G Trial at Japan 2020 Summer Olympics:**
  - 8k 360 degree video streams
  - 5, 24-28, 37-40, 64-71 GHz Proposed

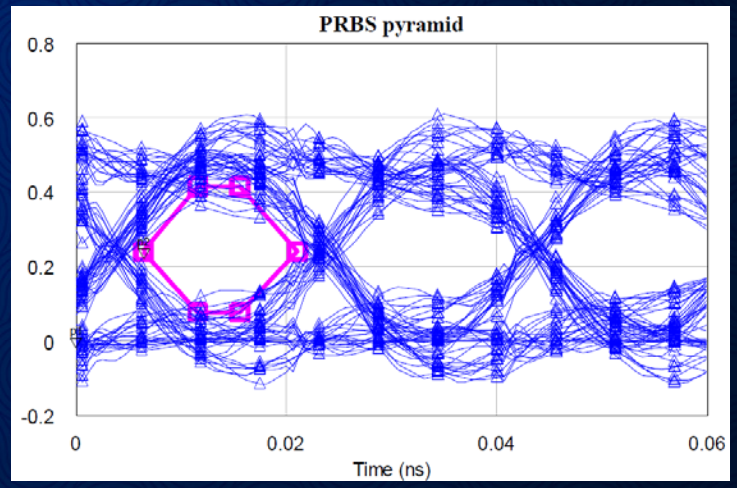
Requirements for 5G Production Tests

- **New Test Equipment Needed**
  - Higher Test Frequencies (> than most ATE testers can handle)
  - Very Large Number of Channels
- **Short Time of Test with High Throughput**
  - Parallel test (multi-site)
- **High Accuracy is needed to Validate Performance**
  - Good Signal Integrity at high RF frequency
  - Prevent packaging bad devices due to yield

Key Challenges in 5G Production Tests

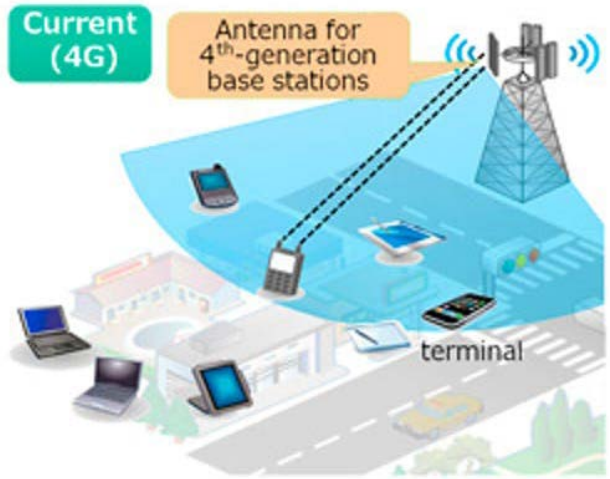
1. **Handling Very Large Number of RF Test Channels**
   - Parallel Tests require even larger no. of Channels in RF Tester = $$$$
   - Challenges in Routing RF Channels in Parallel Test setup (X8 DUT, >160 Channels, >25GHz)
2. **Ensuring Excellent Signal Integrity**
   - Post-Calibration Verifications & Use of Dedicated Calibration Standards Substrates.
   - Maintaining Calibrated State for as long as possible (esp. with Frequency Extenders).
     - Throughput impact if frequent recal. needed.

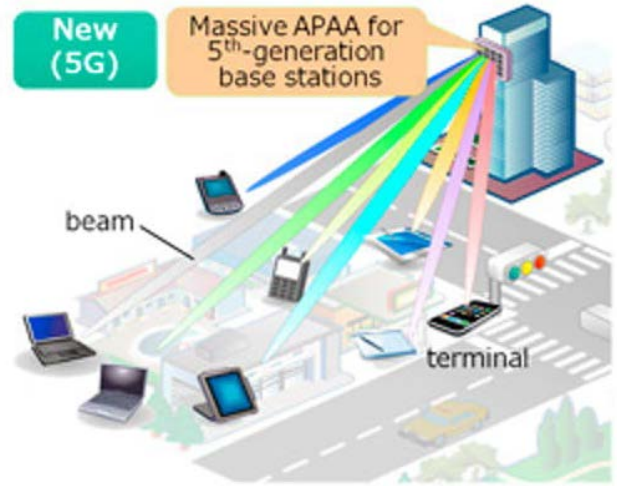


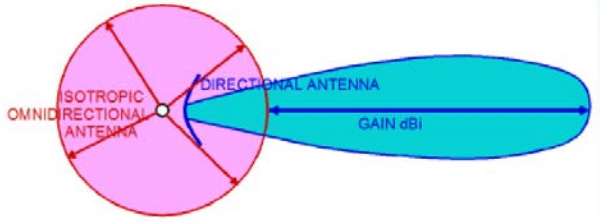


1. Handling Very Large Number of RF Test Channels

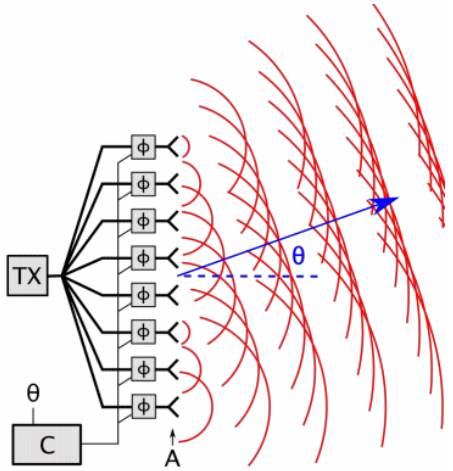
- **5G is using higher freq.**
- **Larger Attenuation at Higher Frequencies.**
  - Omnidirectional Antenna cannot support
- **Directional Antenna needed**
  - Active Phased Arrays & Beamforming
  - Up to 64 lines at 70 GHz in a single device
- **Massive MIMO with Active Phased Array Antennas for 5G.**

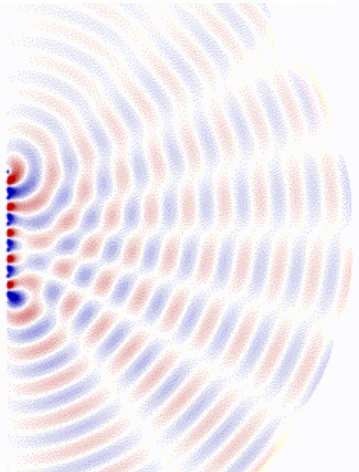






Omnidirectional vs Directional Antenna

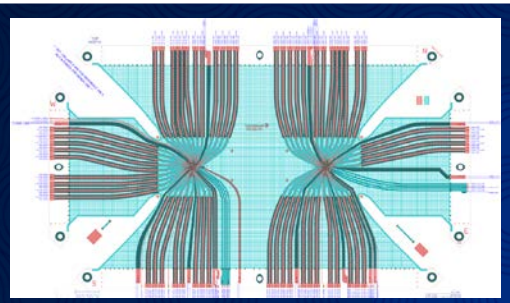
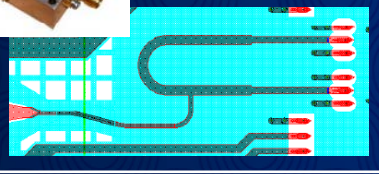
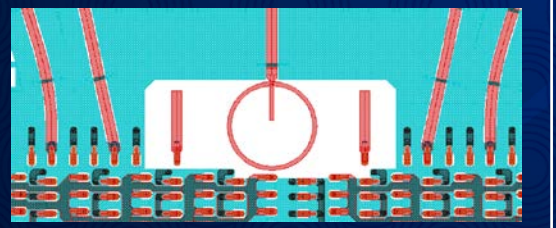




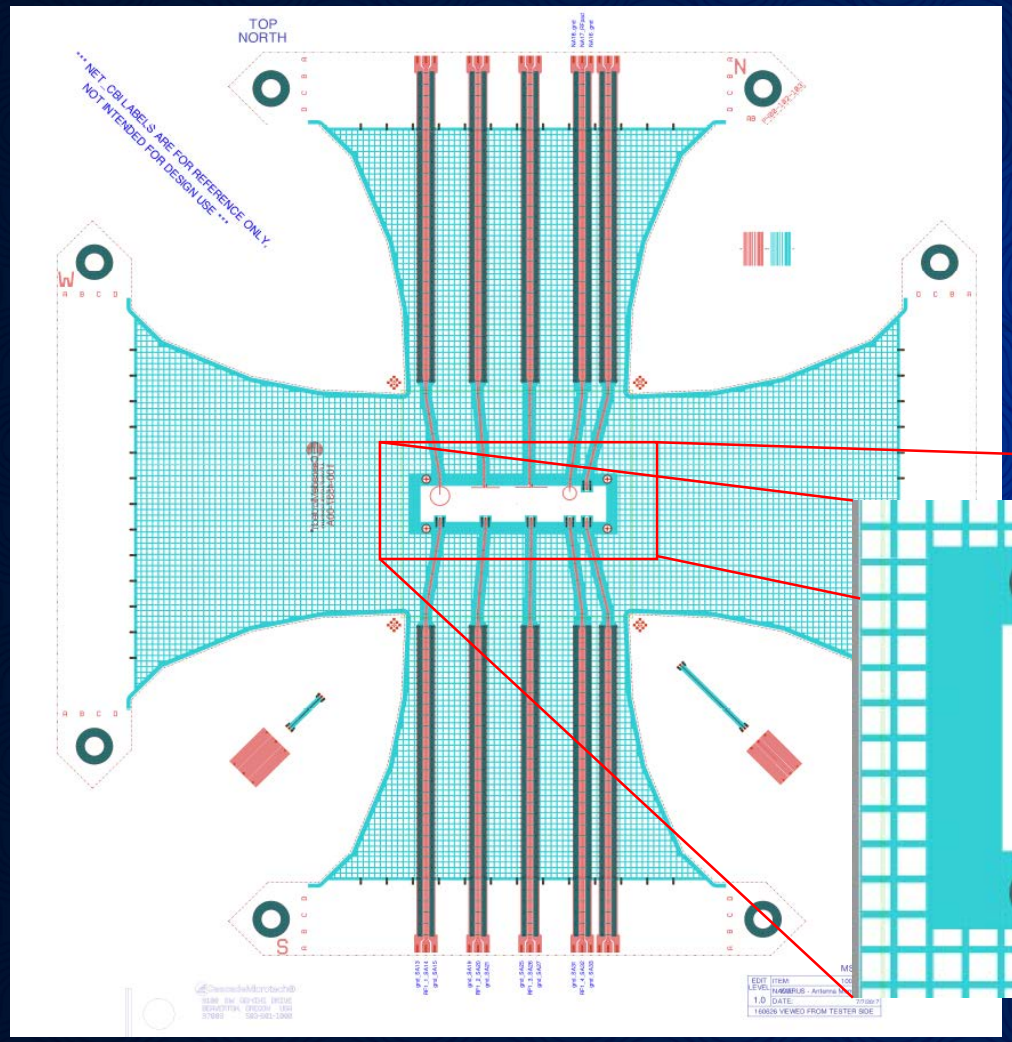
15 Antennas, ¼λ apart
Phase swept -120° to 120°

https://en.wikipedia.org/wiki/Phased_array
https://www.mitsubishielectric.com/en/about/rd/research/highlights/communications/5g.html

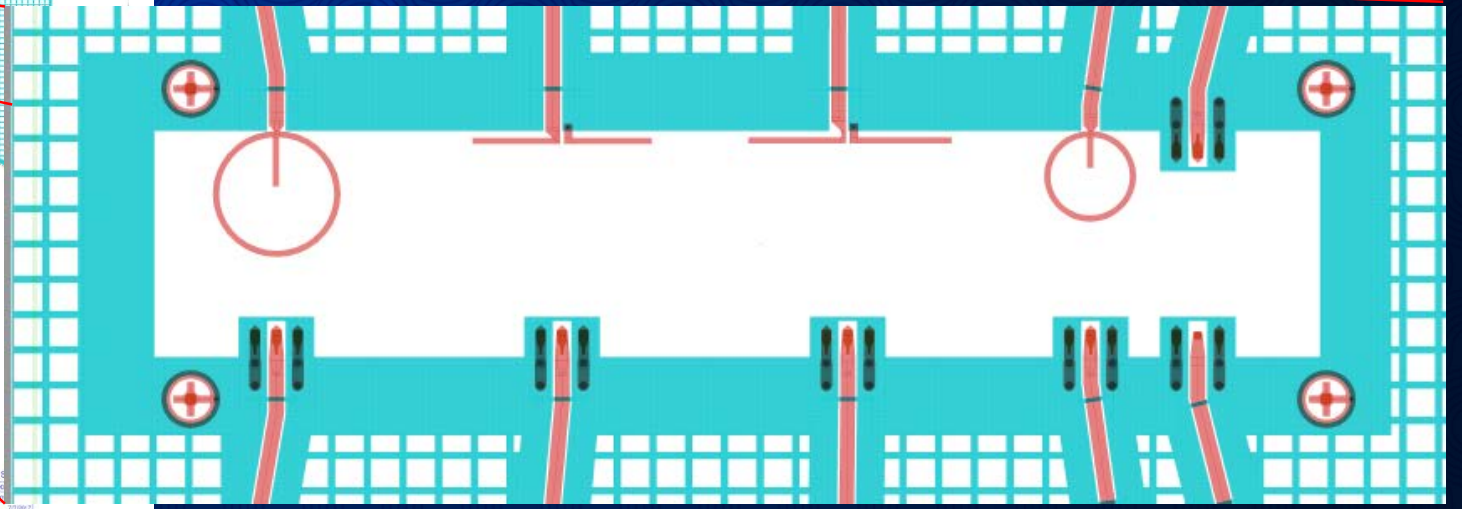
1. Handling Very Large Number of RF Test Channels

Test Method	Advantages	Disadvantages
Full Channel 	• Full RF Coverage • Fast	• Expensive Tester • Routing/Space Transformation Difficulties
Balun, Switches, Combiners  	• Established Methods	• Discrete Components – High Loss, Large & Bulky • On-ProbeCard – Narrowband & High Loss
Antenna Coupling 	• Reduce Channel Count (4:1 combining)	• > Loss than Conducted Tests • Space needed for Antenna

Membrane Probe Head & Antenna Test Structures

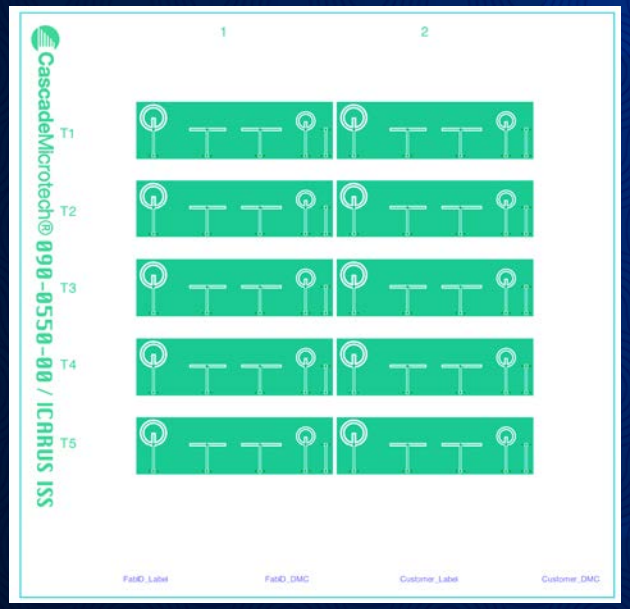


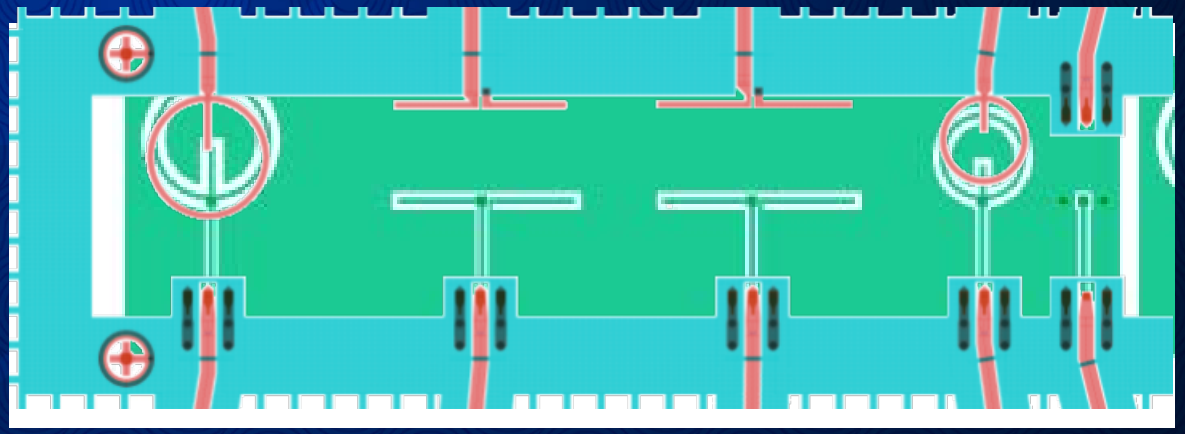
- **2 dipoles & 2 ring antennas are Designed & Tested**



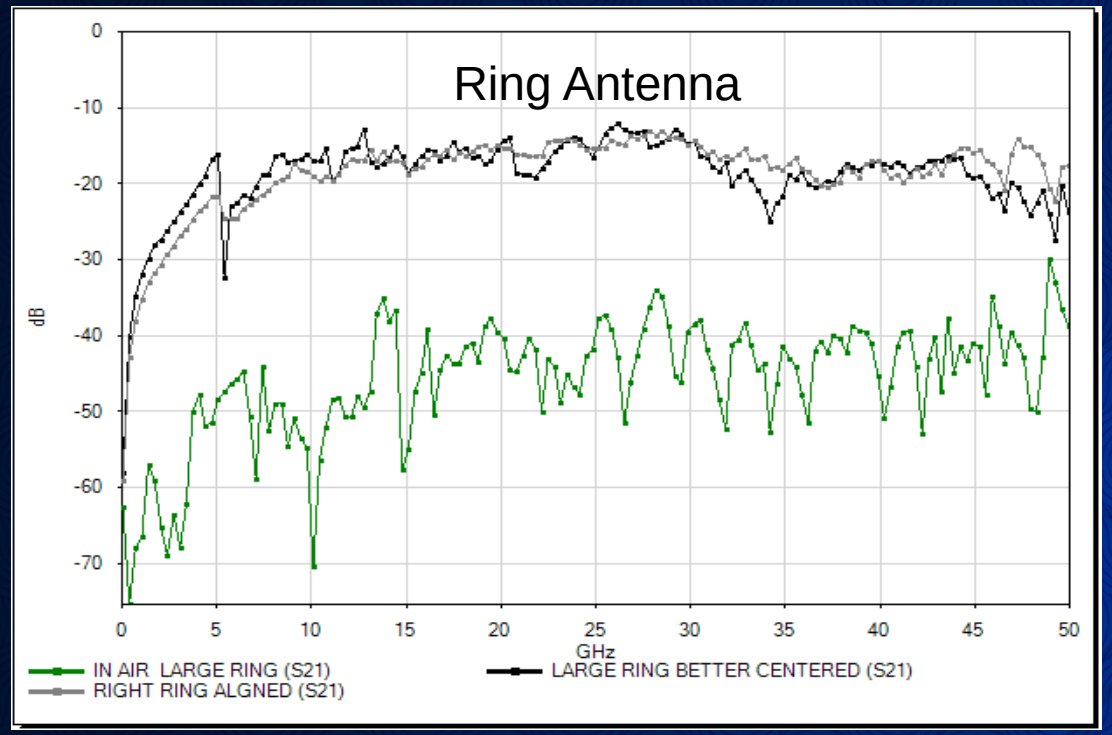
Ceramic Substrate for Reception Tests

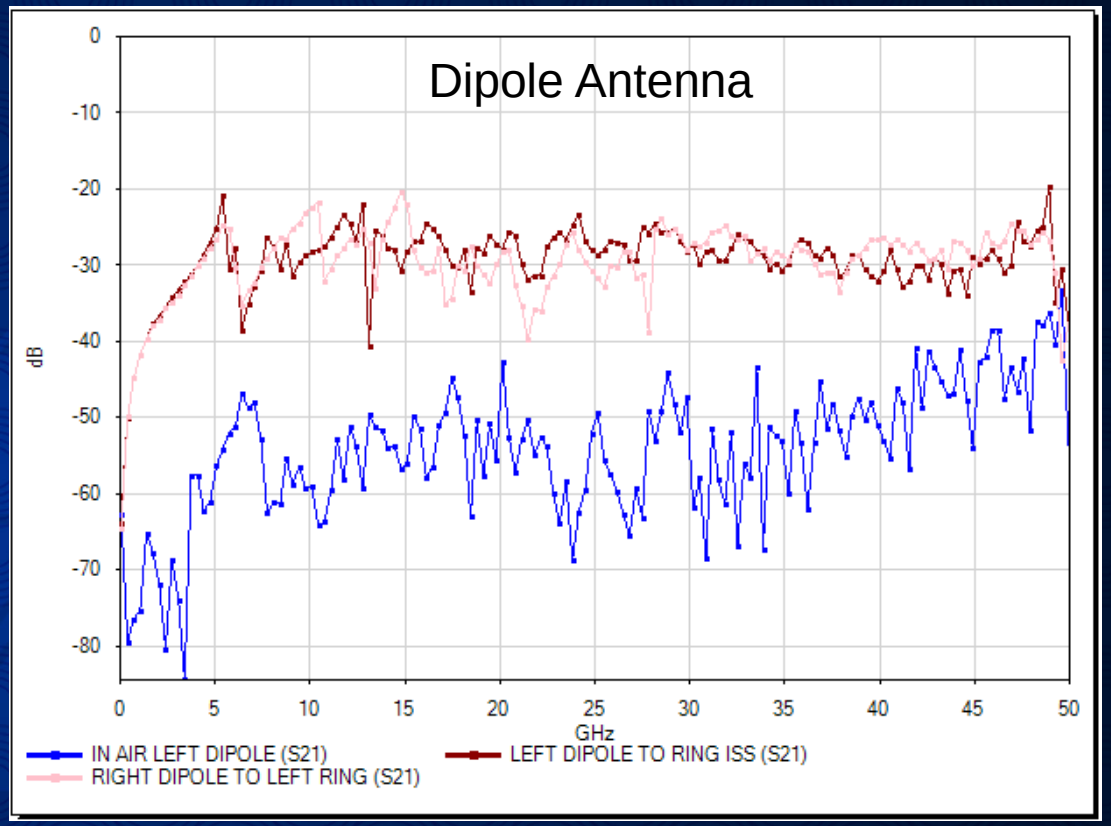
- A substrate was fabricated for reception of the signals.
- Signal goes back to the probe head (membrane) through GSG tips.





Insertion Loss for Ring & Dipole Antenna



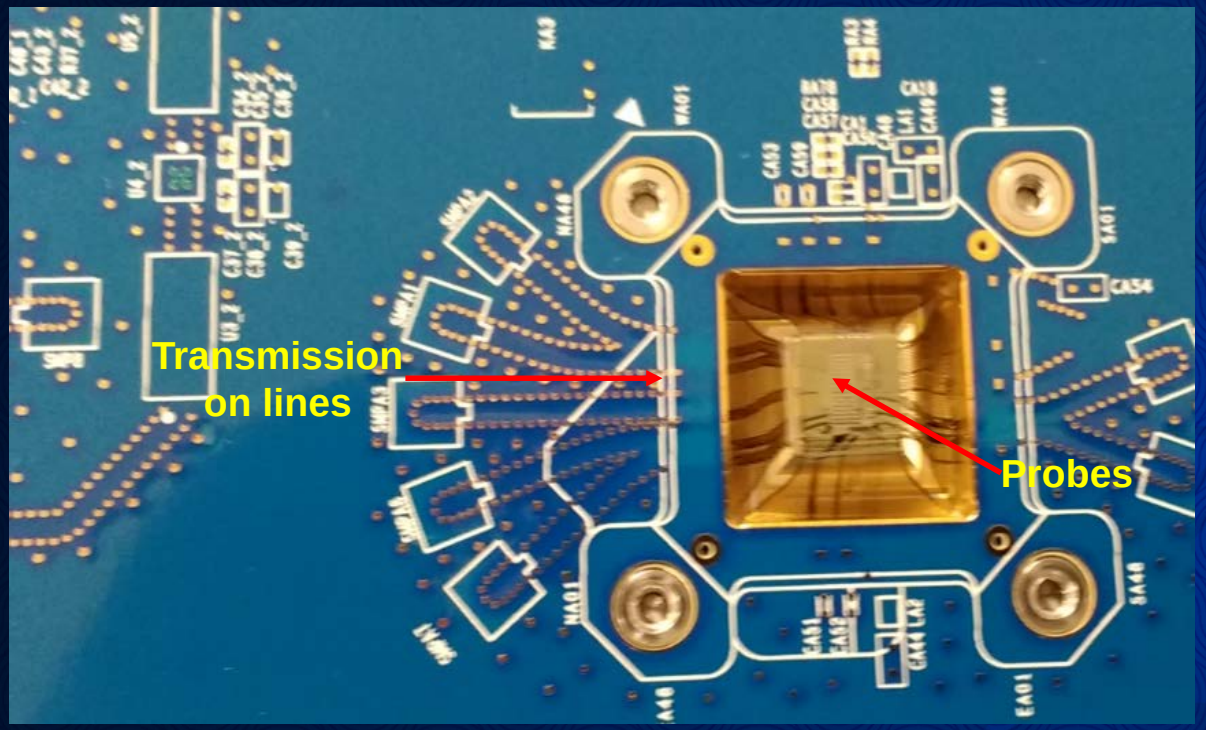


- Insertion Losses higher than noise by about 20dB.
- Wide bandwidth observed due to near field coupling (>100μm).
- Ring Antenna has better performance than Dipole Antenna.

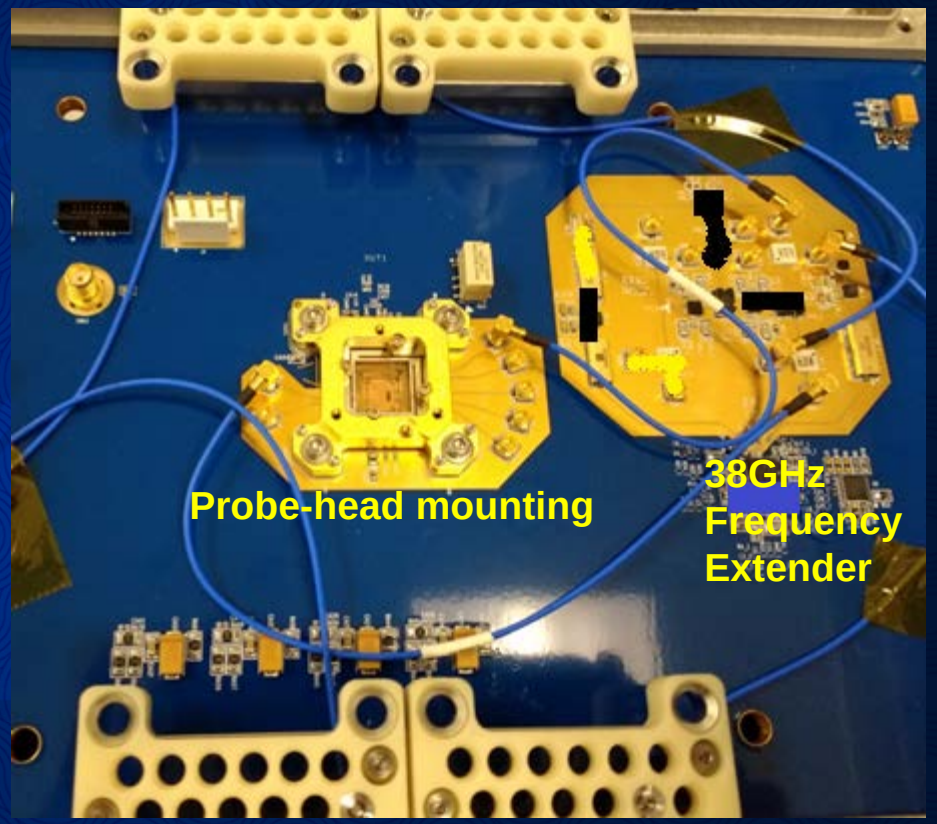
Intel's ATE mmW Test Setup

- **Advantest 93000 PSRF ATE System**
  - generates 6 GHz for device testing
- **SIU PCB (Wafer Sort Interface Unit)**
  - mmW Frequency Extender developed using off-the-shelf components.
    - Up-converts RF Test Signal from the ATE → 38 GHz CW signal.
    - Down-converts 38 GHz RF signal from the DUT to a signal manageable within the measurement range of the ATE (< 6GHz)

Intel's ATE mmW Tests – Membrane Probe Head



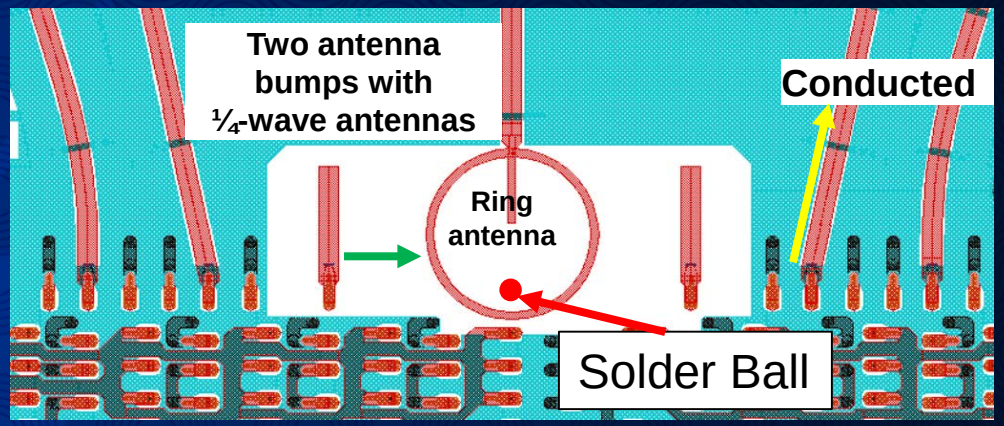
Wafer Side of Wafer Sort Interface Unit



ATE Side of Wafer Sort Interface Unit

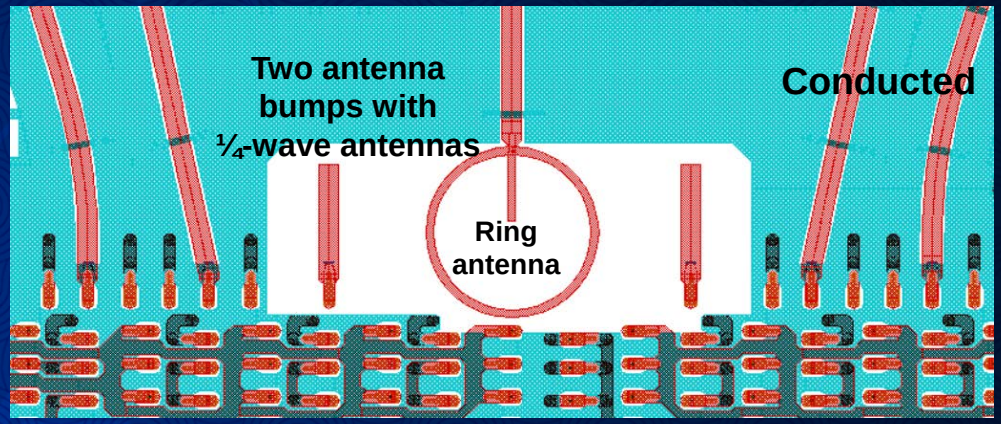
Intel's ATE mmW Test – Test Setup

- **Fully Conducted Test**
  - Electrical contact
- **¼ wave Antenna Transmitting to Ring Antenna**
  - ¼ wave makes contact with solder ball and then transmits to ring antenna
- **Solder Ball Transmit to Ring Antenna**



Intel's ATE mmW Test – Results

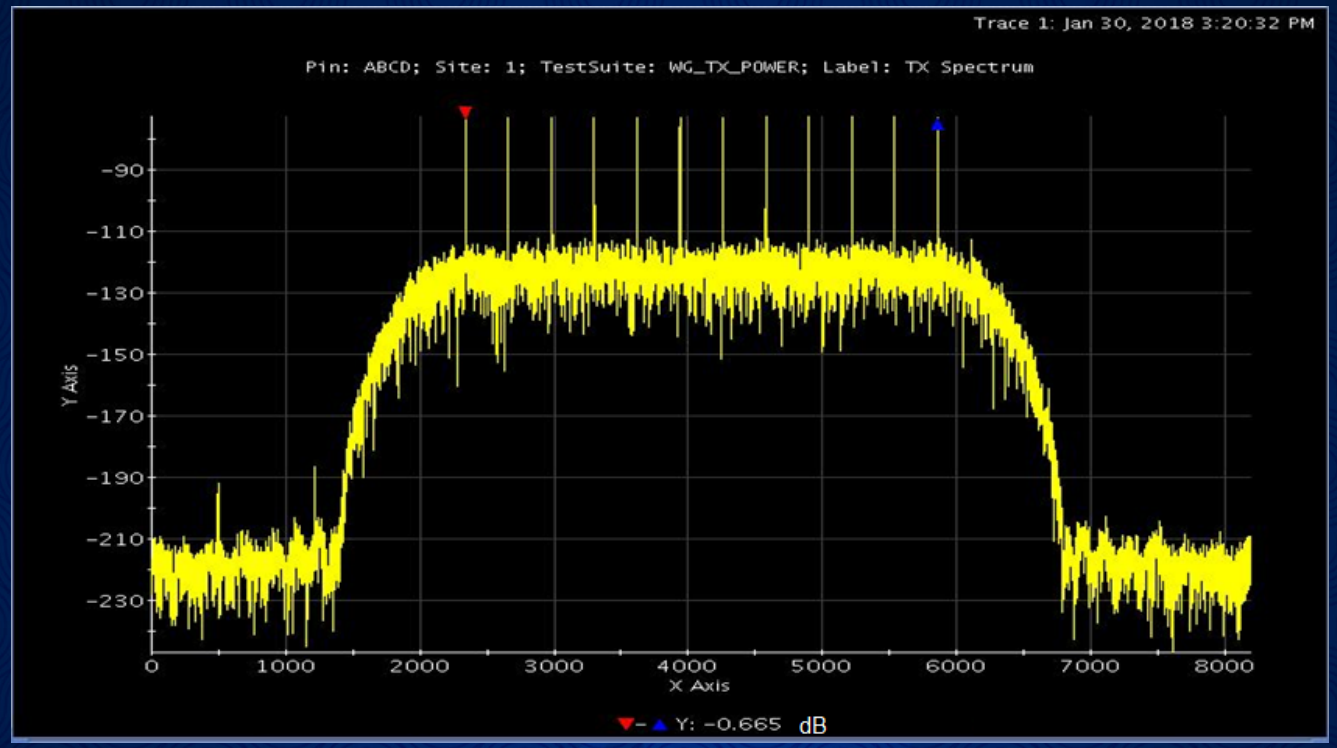
Probe touchdown	Transmit Power from Same DIE (dBm)		
	1/4λ to Ring Antenna	Ring Antenna only	Fully Conducted Path
1	-63.27	-86.67	-38.593
2	-63.169	-85.95	-38.594
3	-63.8	-86.68	-38.588
4	-63.825	-86.62	-38.589
5	-63.636	-85.63	-38.59
6	-63.687	-85.51	-38.597
7	-63.793	-86.62	-38.602
8	-64.043	-86.23	-38.61
9	-64.728	-85.14	-38.616
10	-64.673	-85.98	-38.615
11	-64.955	-86.69	-38.634
12	-64.866	-85.43	-38.649
13	-65.111	-85.95	-38.648
14	-65.785	-84.65	-38.698
15	-65.826	-84.25	-38.711
16	-65.854	-84.13	-38.757
17	-65.748	-84.32	-38.762
18	-65.831	-84.61	-38.766
19	-65.696	-84.21	-38.753
20	-65.692	-84.74	-38.778



mm Wave Probe Connection: 2 to 1 combining with ¼-wave antennas

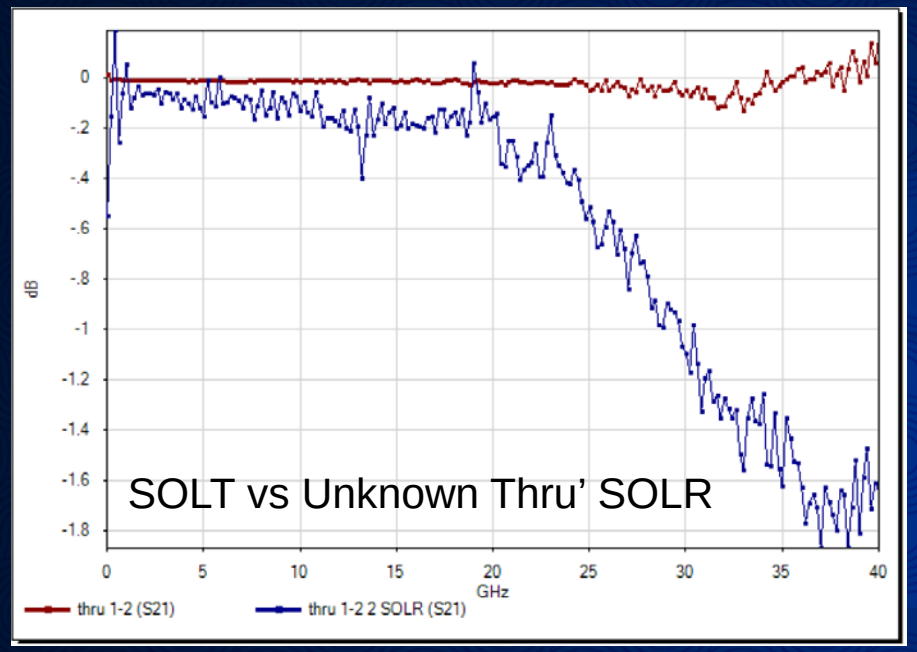
- **Very Repeatable Measurements at 38.56 GHz**

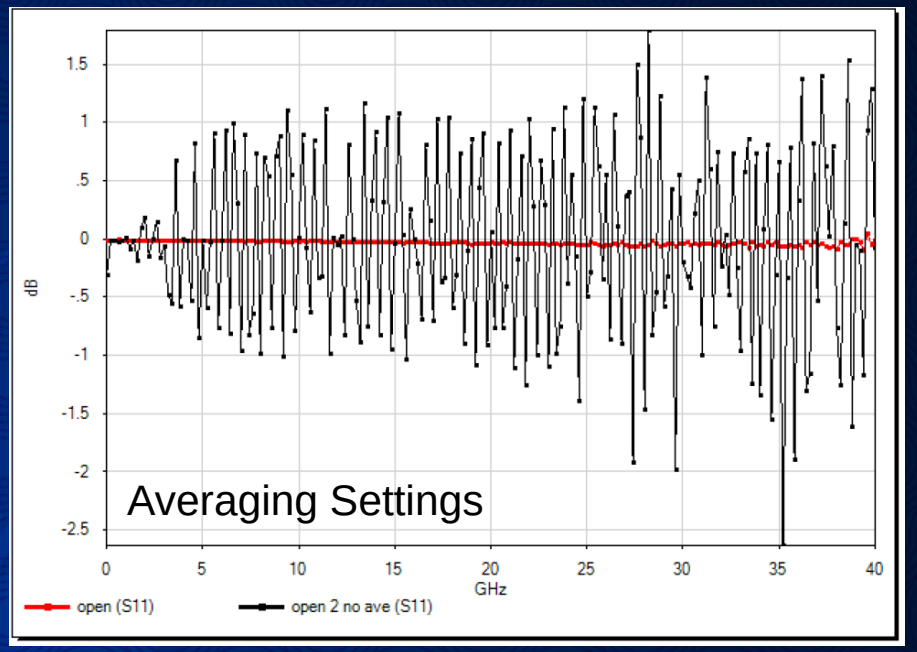
Intel's ATE mmW Test – Results



- **Spectrum measured with the ¼-antenna**
  - Multi-tone Spectra at 38 GHz using an IQ waveform (modulated signal)
- **In-membrane Antennas is feasible for 5G Production Tests.**

2. Ensuring Excellent Signal Integrity

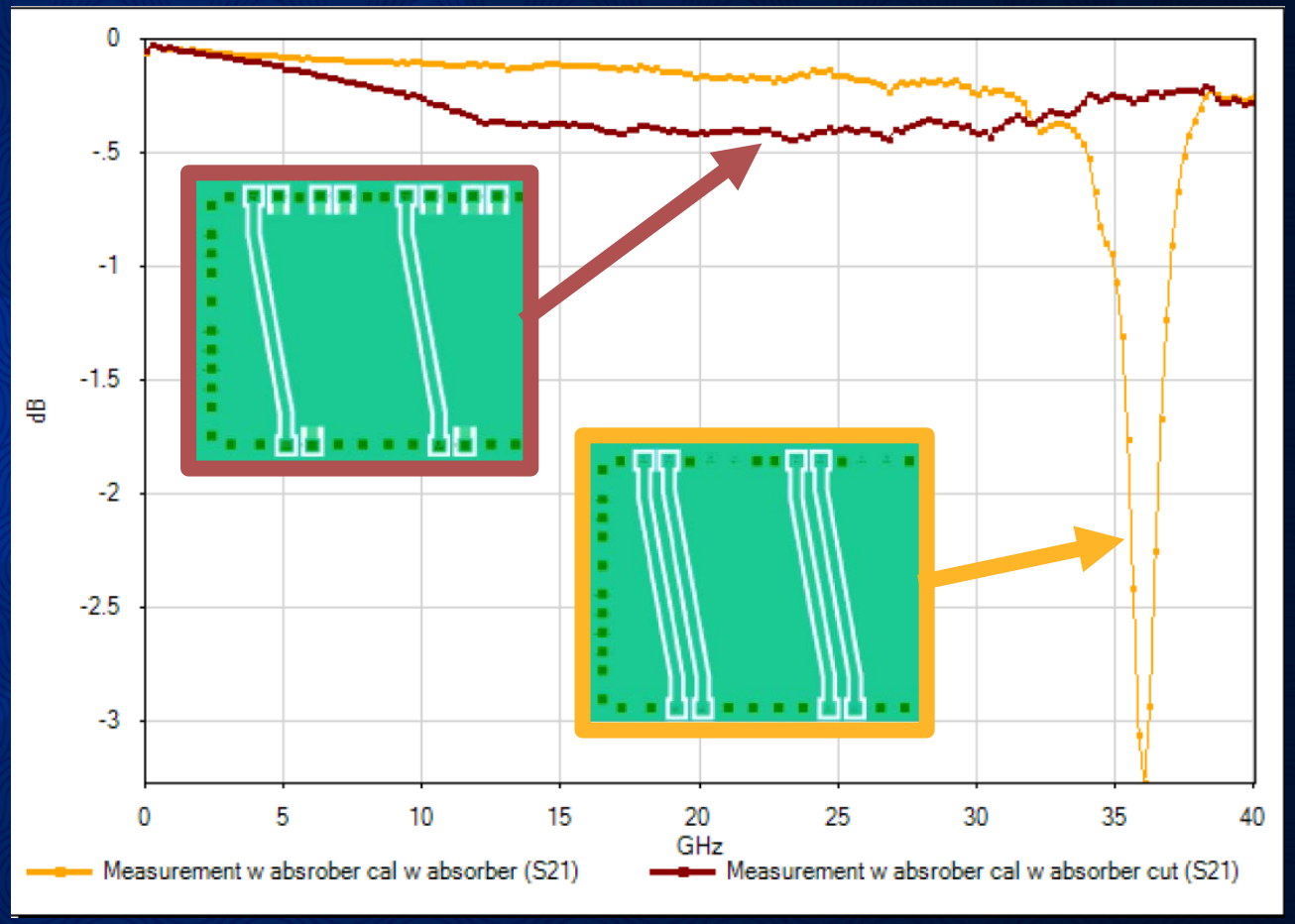




- **Post-Calibration Verification Checks are strongly recommended**
- **It is the only way to reveal Calibration Anomalies**
  - SOLT vs SOLR on thru', SOLT appears better
  - Open check with Gain (Optimize with IFBW settings)

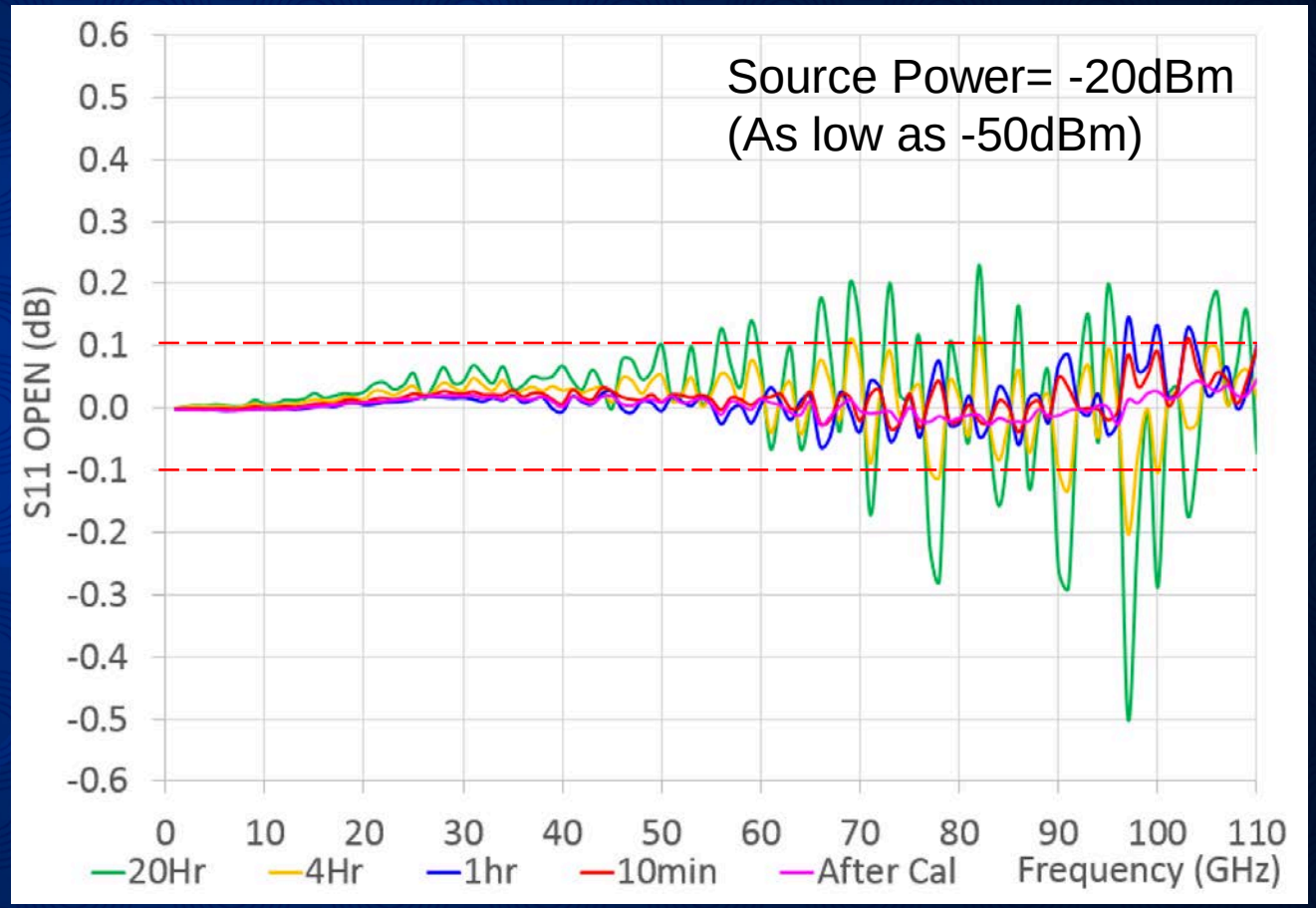
Dedicated Calibration Standards

- **Dedicated Calibration Substrates for 5G**
  - Higher Test Frequencies
- **Narrow Pitch GSSG Layout**
  - Results in 36 GHz resonance for Thru' standards.
  - Calibration fail at 36 GHz.
  - Adjacent thru' removed improves calibration performance.
- **Experience & Know-How are Critical.**



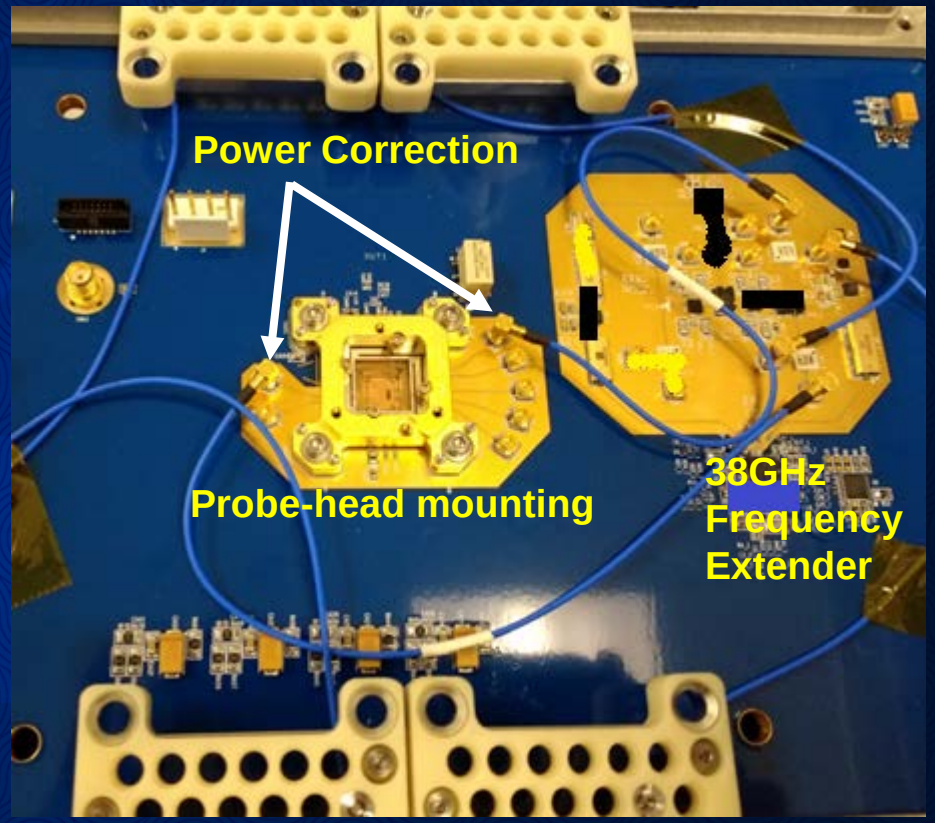
Post-Calibration System Stability

- **As Freq ↑, System Post-Calibration Stability↓.**
- **Worse off when Freq. Extenders are used.**
- **Eg (67-110 GHz Extender)**
  - Open is a Convenient Check.
  - Open After Cal. (< ±0.1 dB).
    - 110 GHz – 10 minutes
    - 90 GHz – 60 minutes
    - 70 GHz – 4 hours
  - Re-calibration is required & Throughput ↓.



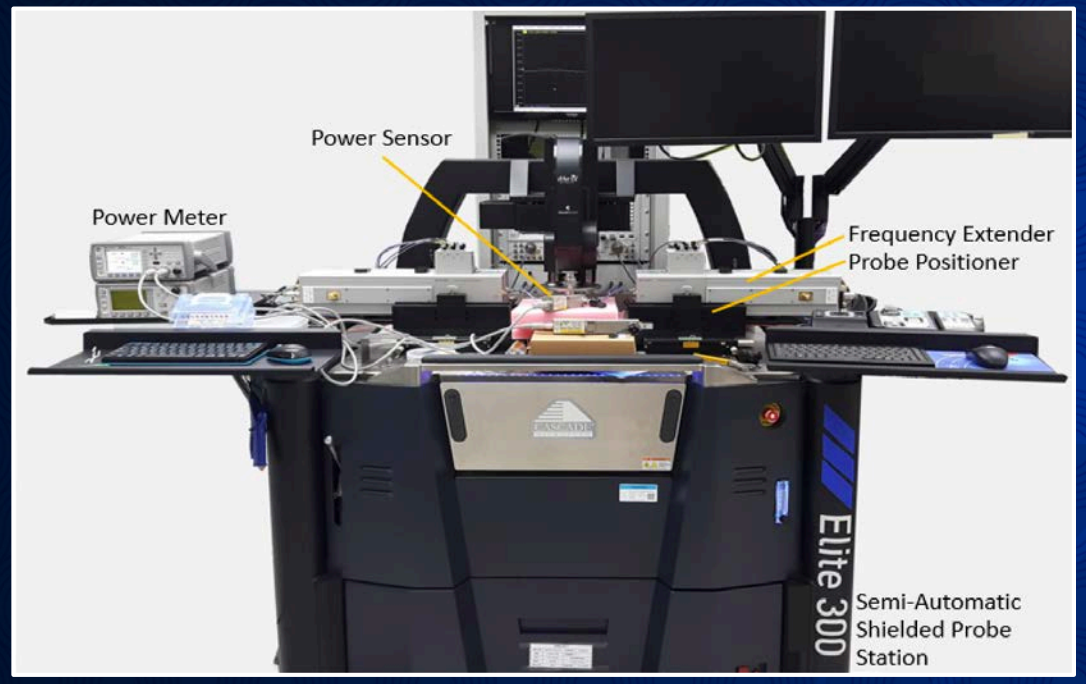
Power Calibration with Frequency Extenders

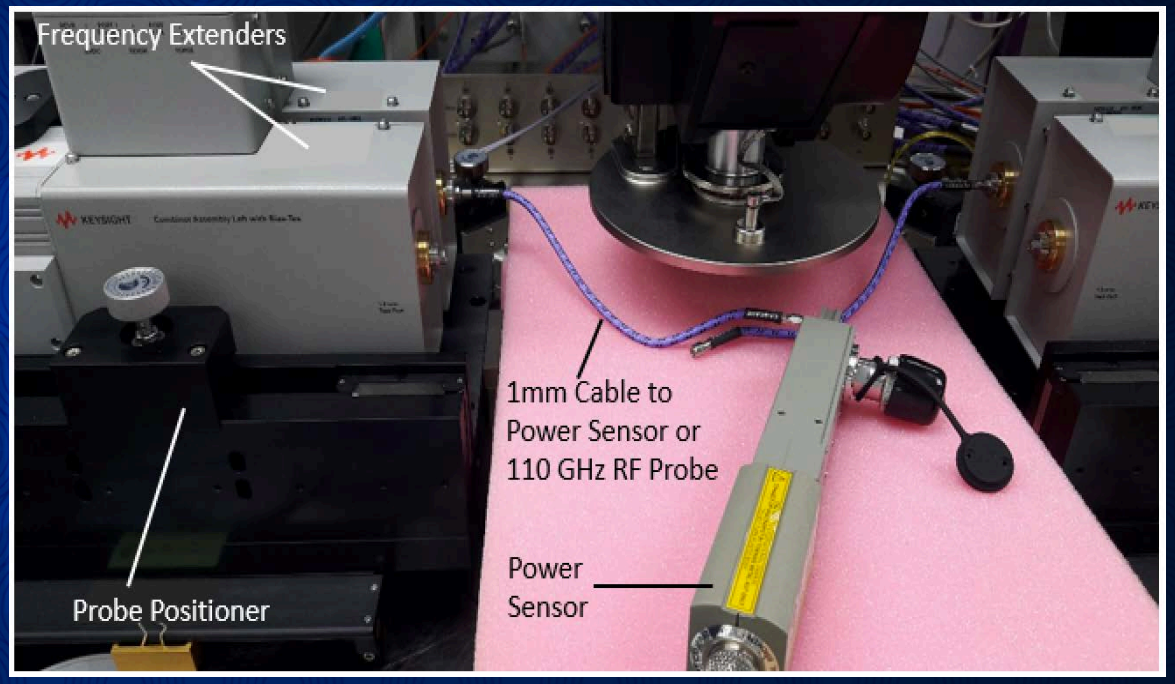
- **Power Cal. not perform on Intel Test Results but if ATE supports…**
- **Source Power Cal.**
  - Characterize Actual Source Power after Frequency Extenders with Power Meter.
  - Account for the Losses of Probecard.
  - Perform Source Power Correction from instrument to probe tips.
- **Receiver Power Cal.**
  - Put Probe Head on Thru' Standard.
  - Perform Receiver power Correction to Probe Tips.



ATE Side of Wafer Sort Interface Unit

Power Calibration with Frequency Extenders

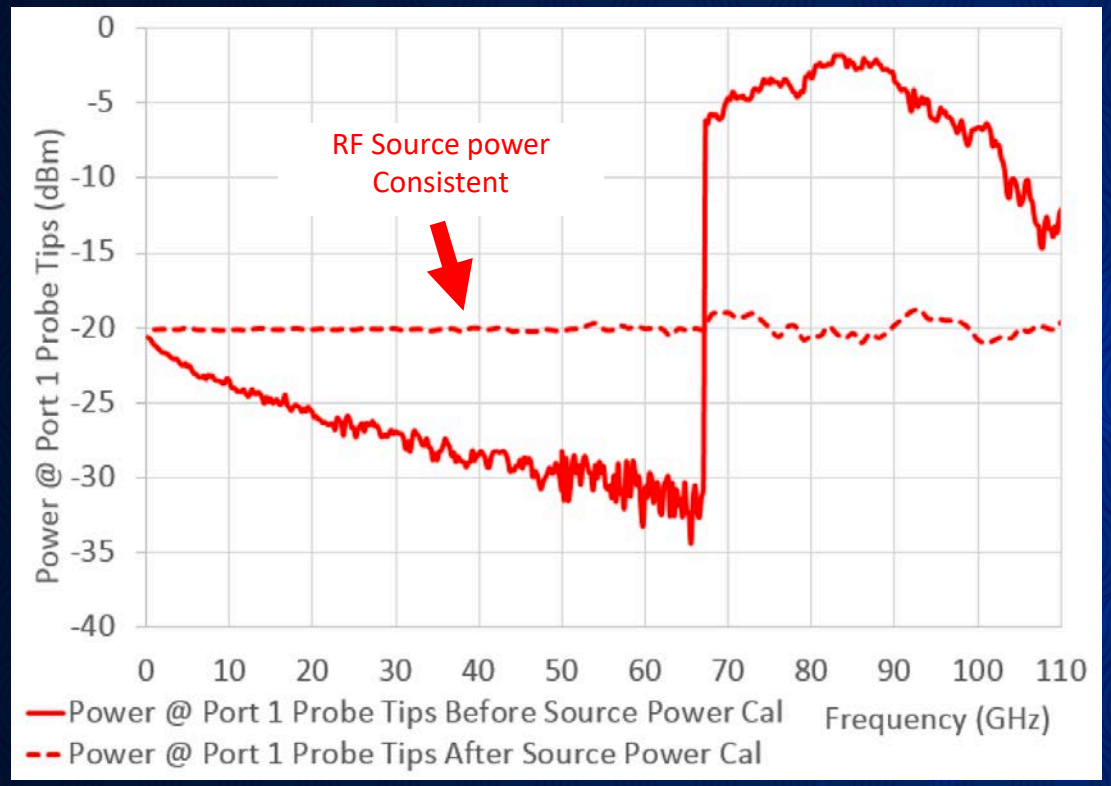




- **110 GHz Engineering Setup for 5G Device Characterization**

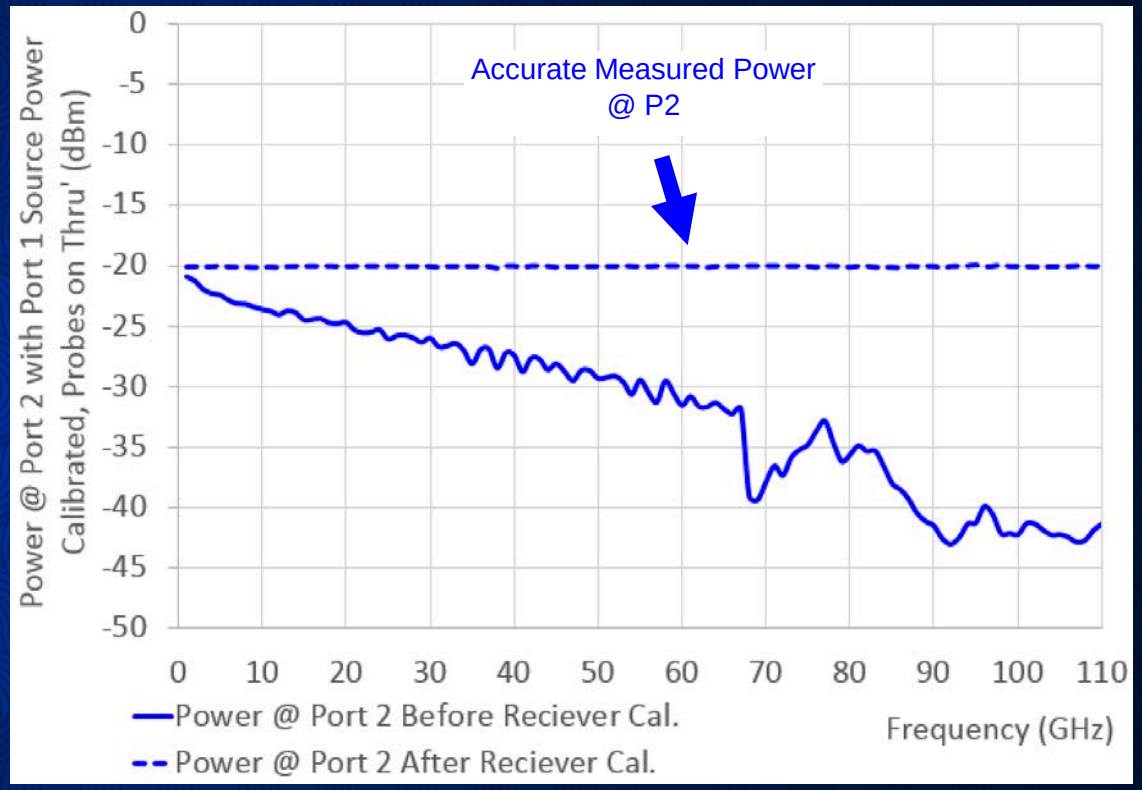
Power Calibration with Frequency Extenders

Source Power @ Tips



- Before Cal. – Loss↑ with freq. & freq. extender Influence power settings.
- After Cal. – Consistent Source Power.

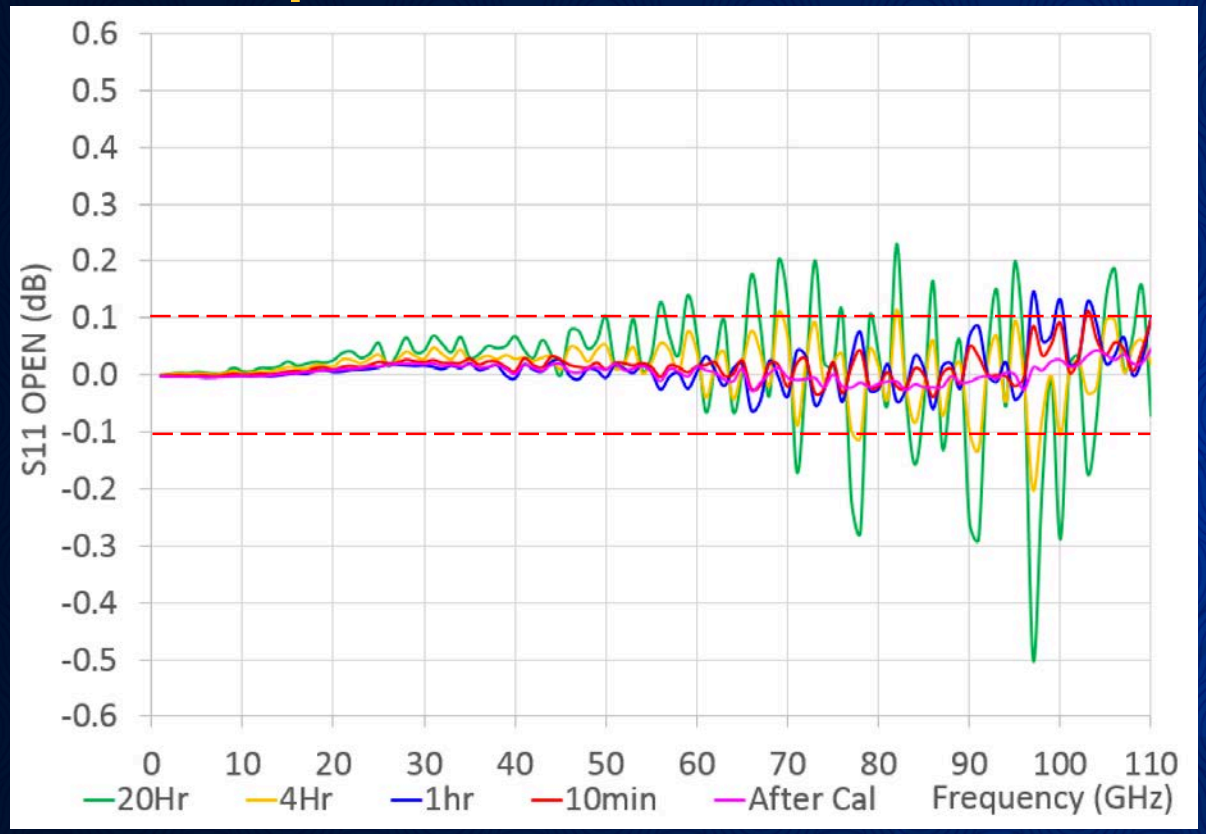
Measured Power @ P2 Receiver



- Before Cal. – Huge Losses at Receiver
- After Cal. – Consistent Power of -20 dBm regardless of freq.

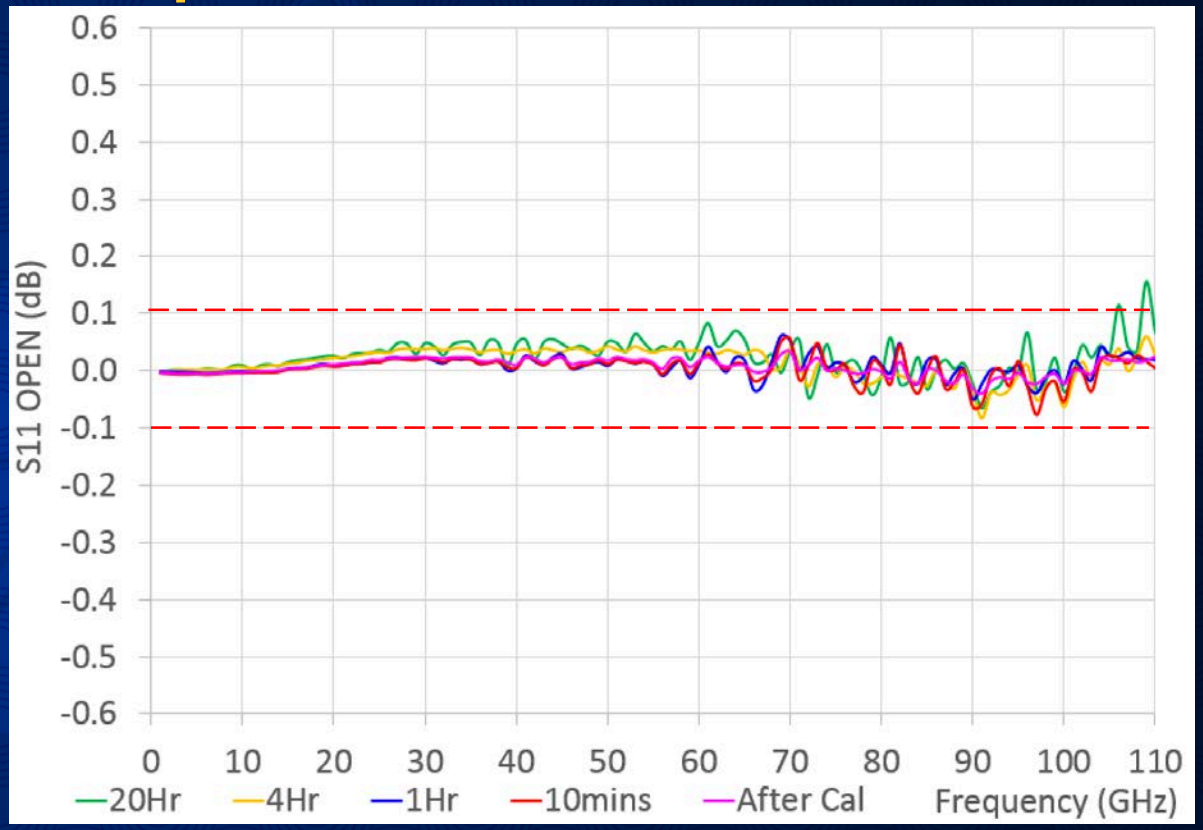
Improved Post-Calibration Stability

S-parameters Calibration



110 GHz – 10 minutes
90 GHz – 60 minutes
70 GHz – 4 hours

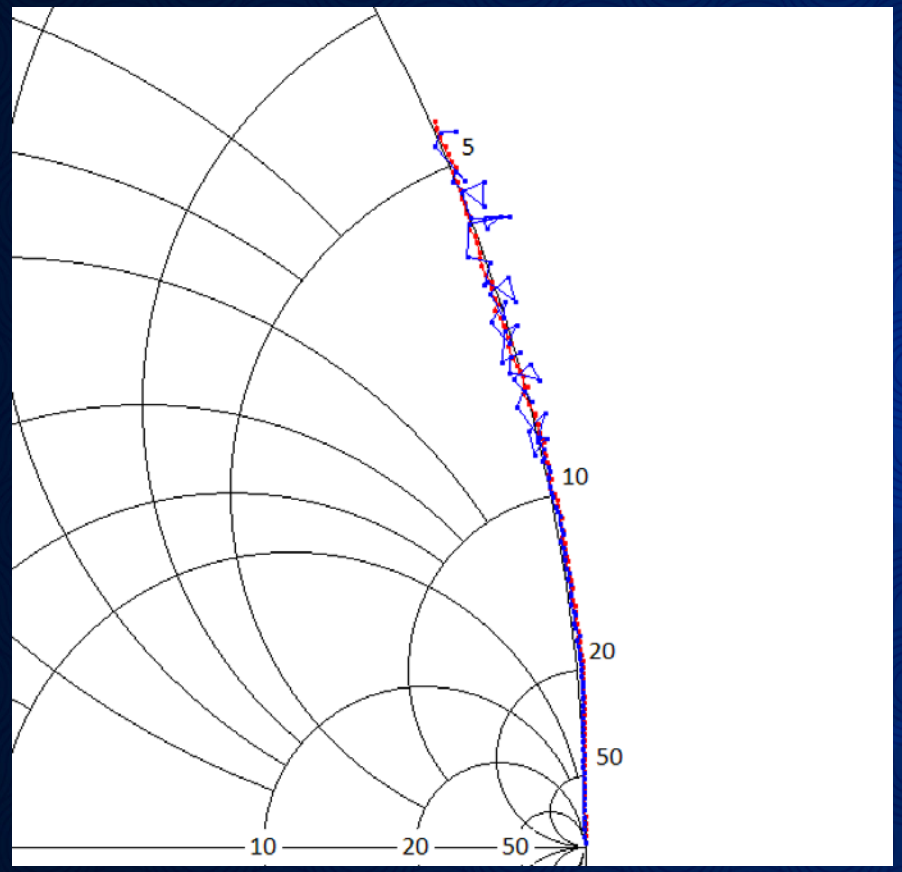
S-parameters+Power Calibration



110 GHz – >4 Hours
90 GHz – >20 Hours
70 GHz – >20 Hours

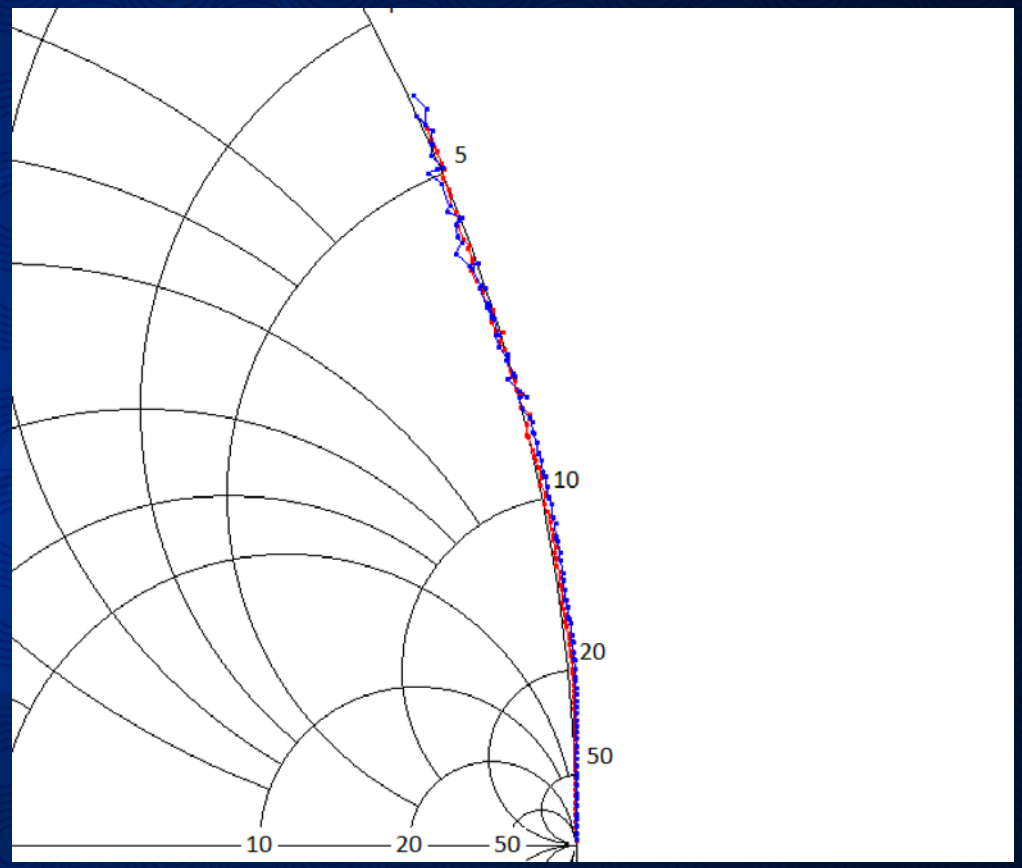
Improved Post-Calibration Stability

S-parameters Calibration



110 GHz Cal. Valid for only 10 mins

S-parameters+Power Calibration



110 GHz Cal. Valid for 4 hours

Summary

- **What is 5G and its Impacts.**
- **Identify 2 Key Challenges for 5G Wafer-Level Tests.**
  - Handling Large RF Channels ; Ensuring Excellent Signal Integrity
- **In-membrane Antennas is feasible for 5G Production Tests.**
  - Reduce RF channels without expensive tester upgrades
  - Good signal integrity that will support 5G production test
    - More designs are now being experimented at Intel
- **Excellent Signal Integrity is Critical for Accurate 5G Tests.**
  - Strongly Recommend Dedicated Calibration Substrates & Post-cal. Verifications.
  - Periodic System Stability Checks are Essential.
    - Power Calibration improves Stability Performance & Test Throughput.

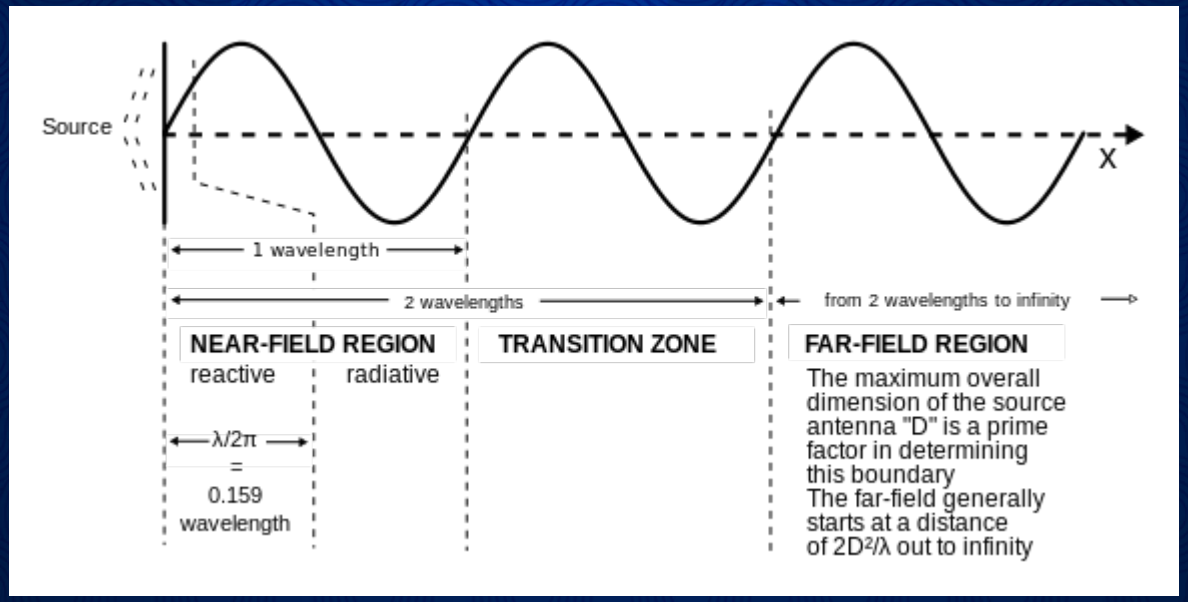
Acknowledgements

- **Colleagues at FormFactor USA**
  - Dr Daniel Bock
  - Amy Leong, Chief Marketing Officer
- **Colleagues at Intel**
  - Michael Engelhardt, Michael Hemena, Robert Murphy, and Balbir Singh

Additional Slides

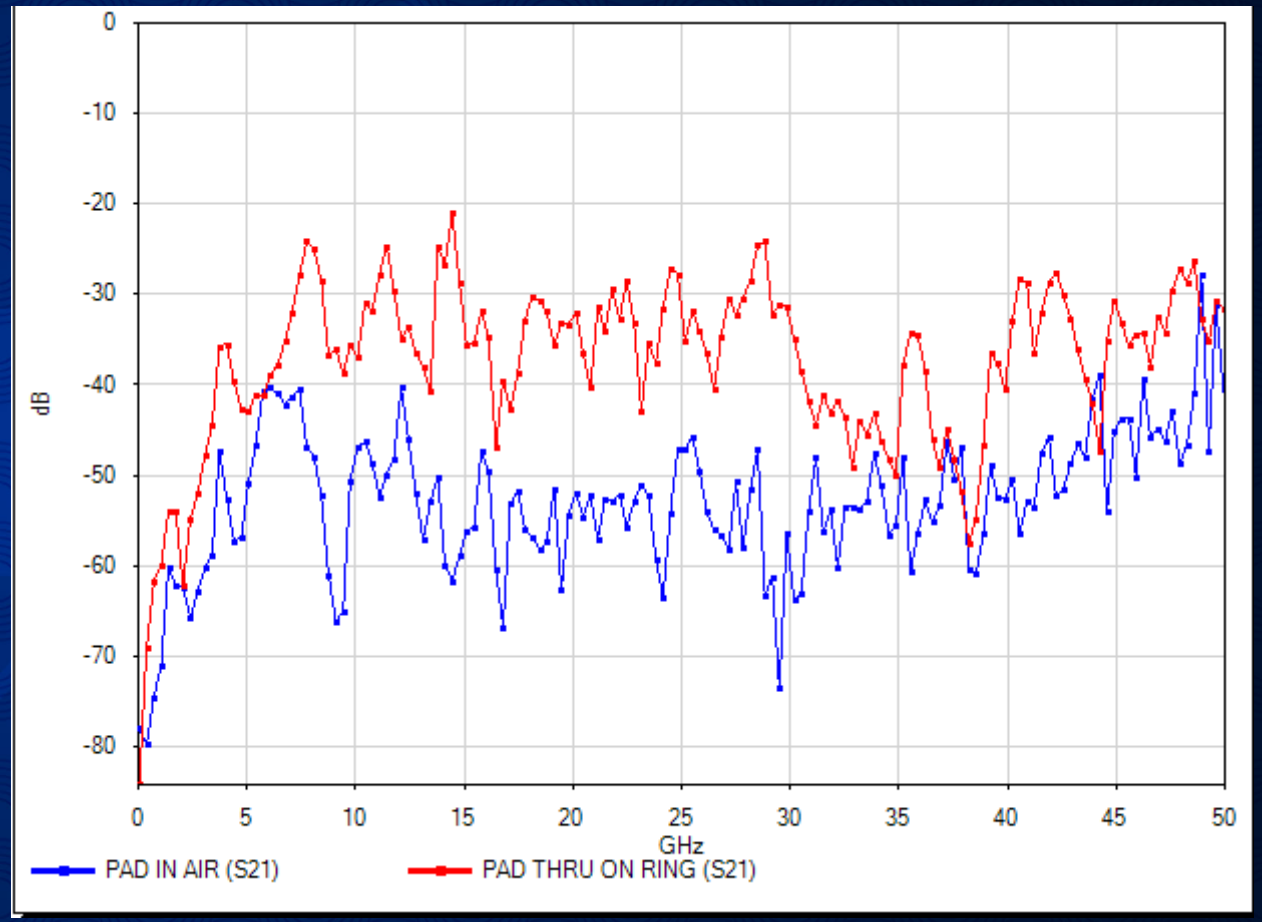
Distance to Antenna – Near field vs. Far-field

- **A Full Antenna needed?**
  - Typical Separation = 100μm, at 30GHz Wavelength = 10 mm
  - Less than 1 wavelength, so the field distribution will depend upon the distance from the antenna



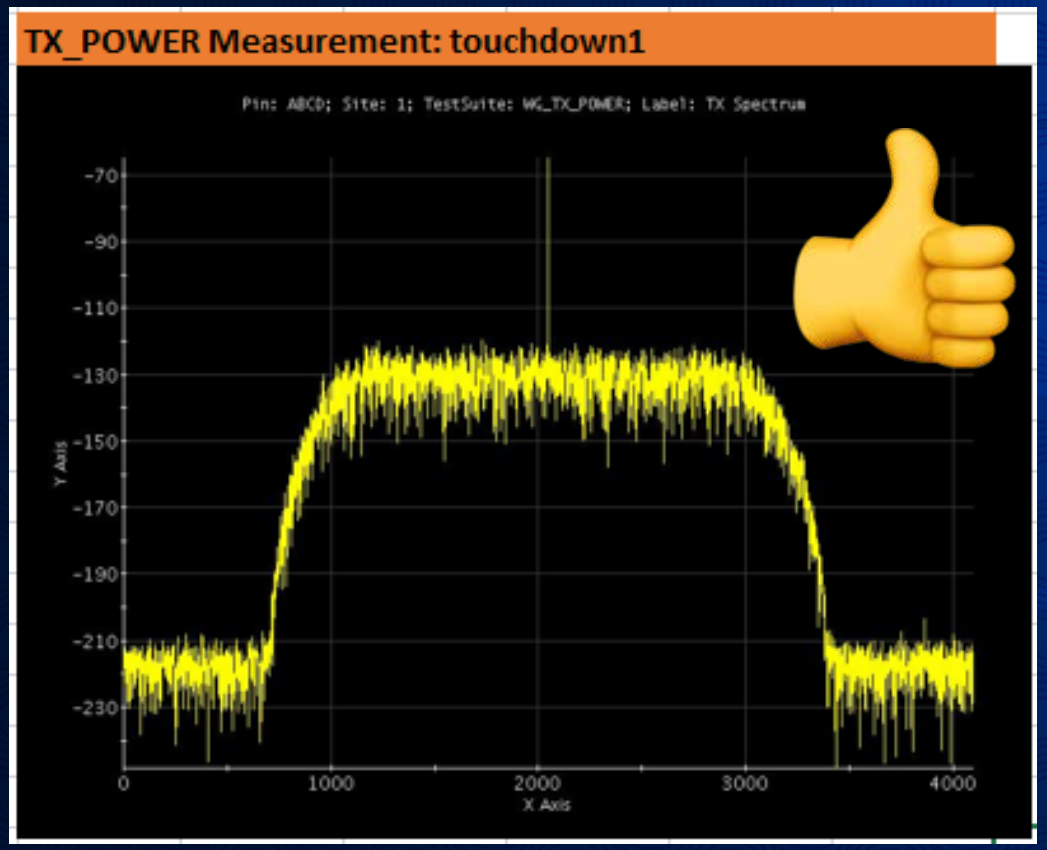
Insertion Loss on Pad

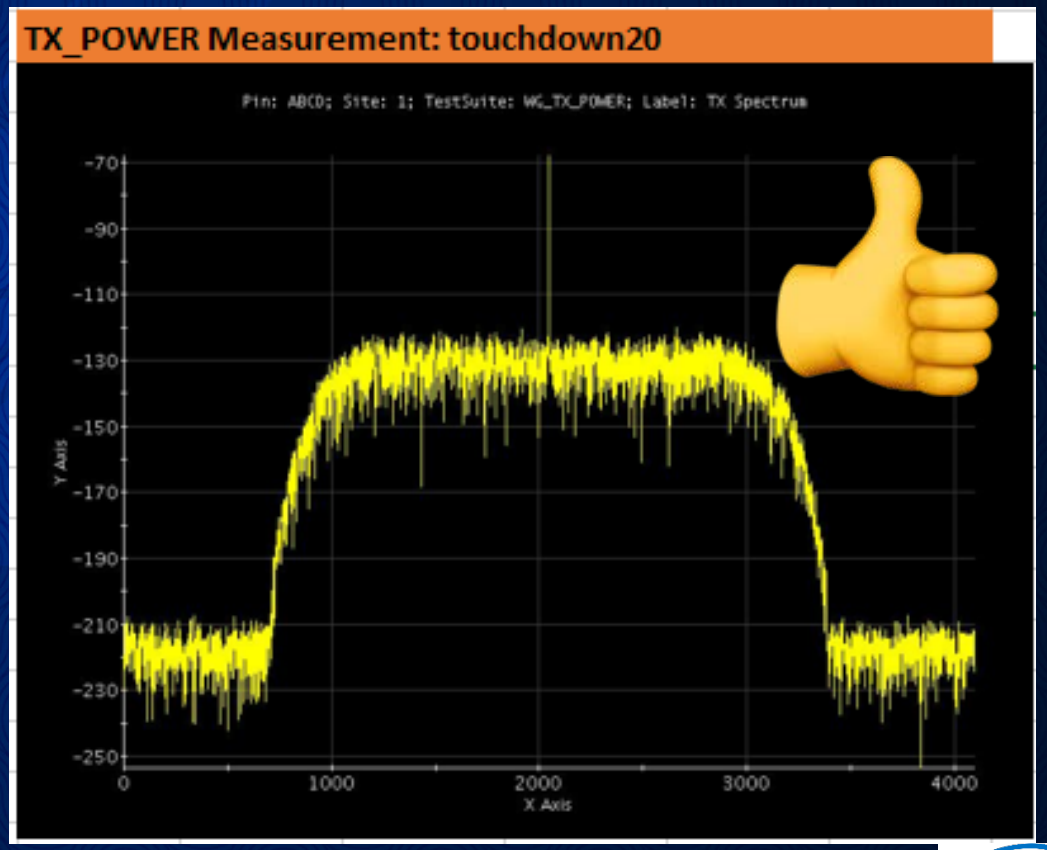
- Some Signal gets through on the Standard Test pad
- But the reception is not as clean across frequency

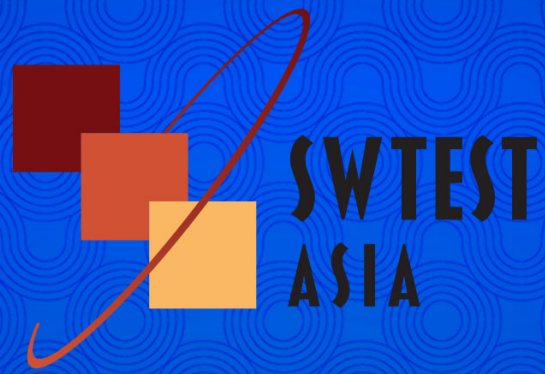


38 GHz CW Spectrum showing repeatability

- **This is Continuous Wave (CW) Spectrum measured with the ¼-antenna signal path**







Simulation of FeinProbe® Probe Card Model for a 5G WLCSP Application

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Jose Moreira — ADVANTEST
Thomas Gneiting — AdMOS
Paul Hurst — HARBOR
Adrian Lim
Ali Abdallah

Taiwan, October 18-19, 2018

Overview

- Introduction
- Motivation
- 5G application test challenges
- FeinProbe® model simulation up to 30GHz
- Probe head design optimization
- Summary and Conclusion
- Follow-On Work

Introduction

- Diversification of semiconductor products
- WLCSP market drivers
- WLCSP electrical and mechanical requirements
- Internal qualification and various tests of spring pin as one of few technologies for WLCSP testing

http://www.swtest.org/swtw_library/2017proc/PDF

5G - Technology and Life Evolution

Source: Companies and government materials

5G Application Test Challenges

- **ATE**
  - Frequency range from 24 GHz to 44 GHz (might change!)
  - Modulation frequency in the range of 800 MHz
  - Devices with antennas integrated in package require over the air test at package level
  - Silicon vendors would like to keep testing infrastructure modifications as small as possible
  - Costs of test is critical
- **PCB**
  - PCB size (can be as larger than 600x500mm)
  - Material choice
  - Copper profile, micro-strip plating
  - Signal trace type
  - PCB stack-up

Wafer Probing Technologies for 5G

❑ Membrane Probe Technology

- Validated for mmWave frequencies and in use by several IC companies
- Good electrical performance
- High cost and long lead time
- Limited compliance
- Very limited repairability

❑ MEMS Probe Technology

- Very small probe size
- Tough to get controlled impedance
- Lower inductance than cantilever
- Not yet proven for mmWave frequencies

❑ Cantilever Probe Technology

- Uncontrolled impedance
- Very high inductance
- Bandwidth <2GHz
- Limited DUT bump and multi-DUT layouts
- Decoupling components far from DUT's
- Limited repairability

❑ Spring Contact Probe Technology

- Stable and consistent contact resistance
- Self-aligning crown plunger tip
- Bandwidth >20GHz
- High Current Carrying Capability (CCC)
- Low cost and lead time

5G Simulation WLCSP Project

Description

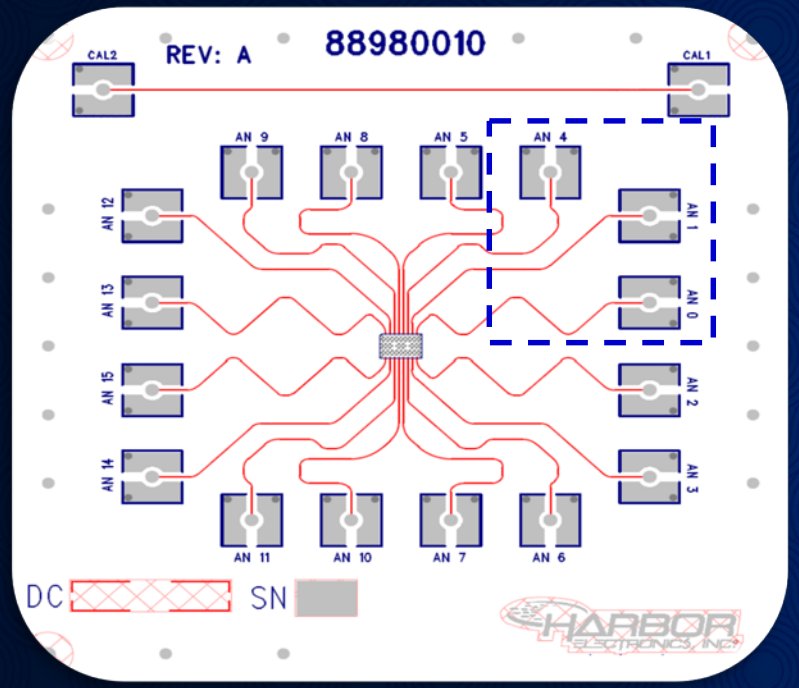
- The RF probe card simulation analysis includes the wafer solder bump, probe head and contact with the PCB and PCB traces up to perfect termination measurement interface
- The single die layout shows 16 RF peripheral ports

Scope

- The board is a single site WLCSP board which is for a 5G application operating at ~29 GHz.
- The transmission lines is connected from the probe head via a micro-strip trace to a suitable connector. A cable then makes the connection to a blind-mate connector
- Simulation includes BGA ball, probe head model, pad on PCB, 1.0 mm of transmission line with perfect termination
- In the probe head is used an uncompressed spring probe of 3.7mm length.
- Simulation shows the results for impedance, insertion/return loss and crosstalk

RF Simulation Project

RF pin locations



- Device pitch ~0.4mm
- Equal trace lengths 38.8mm

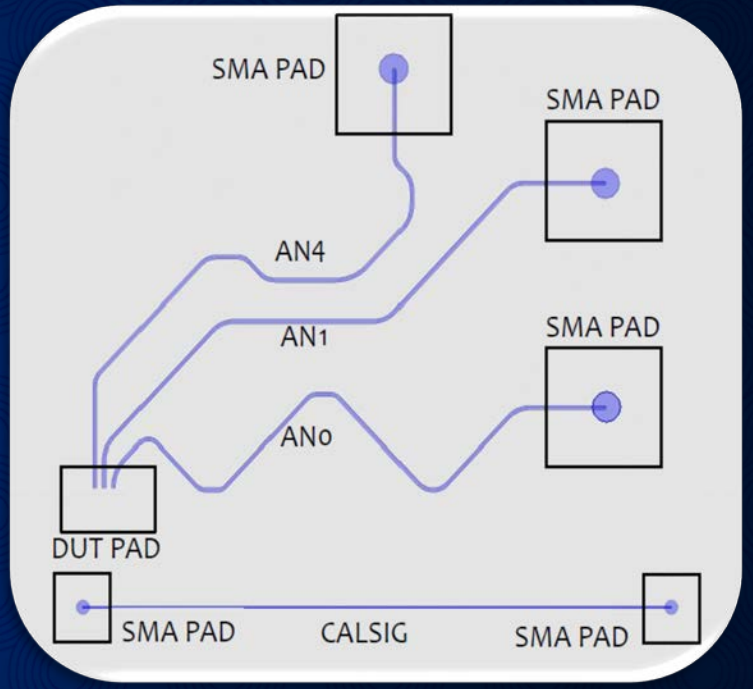
PCB stack-up

Layer Number	Layer Type Signal/ Plane	Layer Name	Cu Wt. oz.	Cu Wt. mils	Dielectric Material	Dielectric Thickness (mils)
1	Top	Top	0.5 oz.	0.7	Foil	
				Tachyon	Pre-Preg	4.2
2	Plane	GND	0.5 oz.	0.7		
				Tachyon	Core	5
3	Plane	GND	0.5 oz.	0.7		
				FR4	Pre-Preg	6
4	Signal	SIG	0.5 oz.	0.7		
				FR4	Core	5
5	Plane	GND	0.5 oz.	0.7		
				FR4	Pre-Preg	90
6	Plane	GND	0.5 oz.	0.7		
				FR4	Core	5
7	Signal	SIG	0.5 oz.	0.7		
				FR4	Pre-Preg	6
8	Plane	GND	0.5 oz.	0.7		
				FR4	Core	5
9	Signal	SIG	0.5 oz.	0.7		
				FR4	Pre-Preg	6
10	Plane	GND	0.5 oz.	0.7		
				Tachyon	Core	5
11	Plane	GND	0.5 oz.	0.7		
				Tachyon	Pre-Preg	4.2
12	Bottom	Bottom	0.5 oz.	0.7	Foil	

Thickness Requirement (inches)	Nominal	Upper	Lower	Stack-Up Estimate
	.150+/-.010	0.16	0.14	

- PCB material FR4 and Isola Tachyon® 100G
- PCB thickness 149.8 mils (3.8mm)

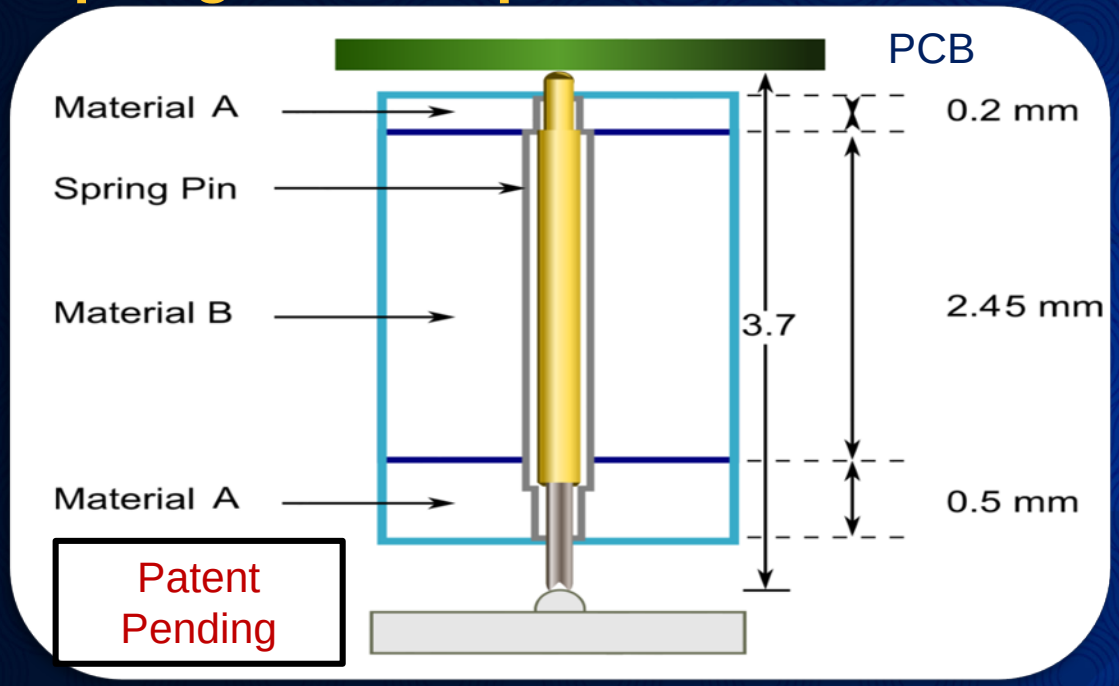
Simulated trace



- Simulation of trace AN0, AN1 and AN4

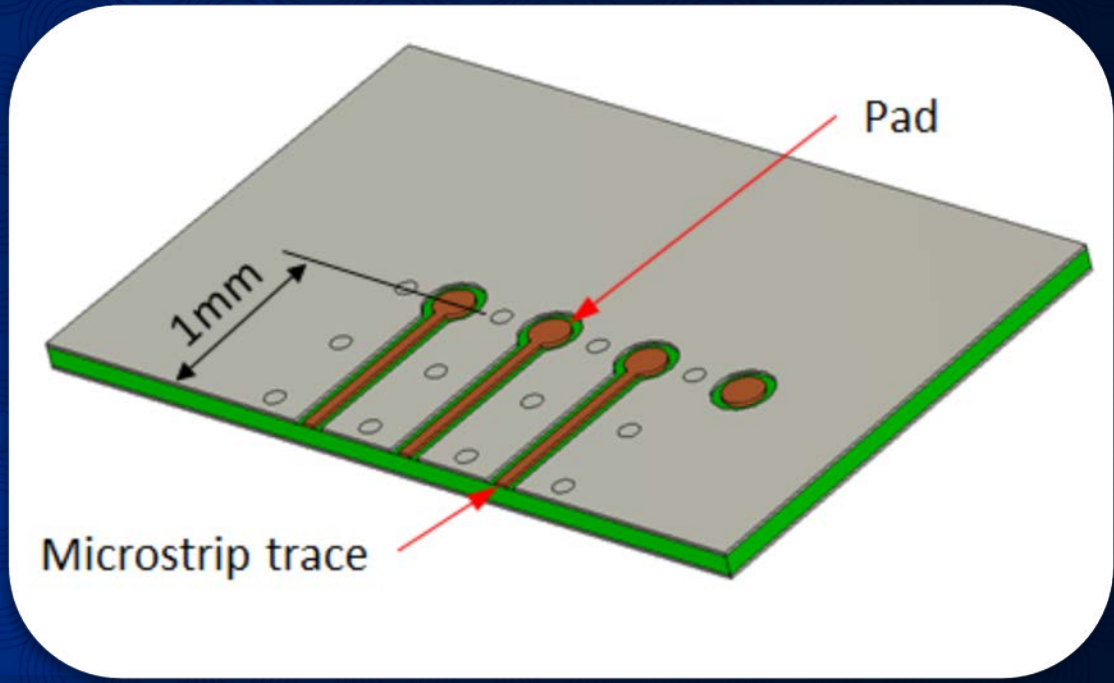
Spring Contact Probe Head Investigation

Spring contact probe head model



- Material choice critical for signal performance
- Different materials were investigated with air between guiding plates as a reference
- Probe length 3.7 mm uncompressed
- Maximum compressed length 3.4 mm

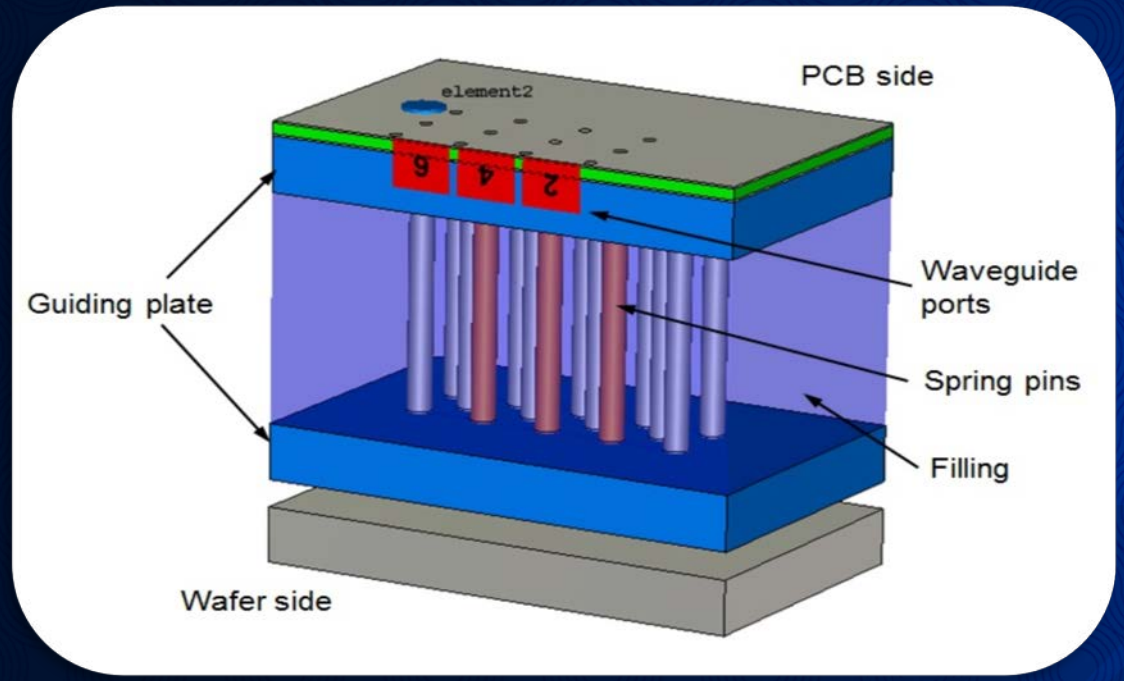
PCB simulation model



- The textbook micro-strip definition of a rectangular conducting cross-section between an inhomogeneous dielectric and air is far away from the reality of an ATE PCB micro-strip geometry

3D EM Simulation Model

3D probe head model



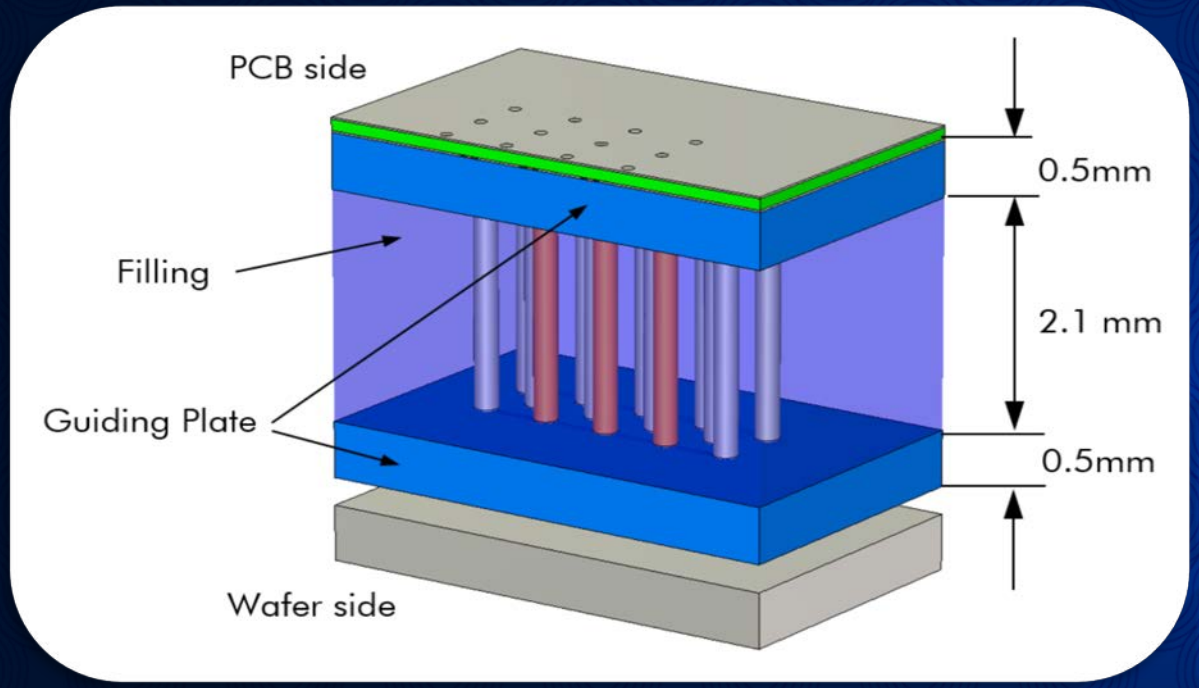
GND		AN1		AN2		AN3
	GND		GND		GND	
PWR		PWR		PWR		PWR

Component	Material	Dielectric constant ε_r	Loss tangent tanδ	Electric cond. (S/m)
Guiding plate	Material A	xxx	0.001	/
Pogo Pins	CuSn6	/	/	8e6
Ground	CuSn6	/	/	8e6
Bump	Sn (Tin)	/	/	8.7e6
Micro strip	Cu	/	/	5.96e7
Isolator PCB	Isola	3.5	0.005	/
Filling	Material B (with option)	1.0	0.002	/
PCB	Isola Tachyon	3.02	0.0021	/

- WLCSP DUT with ~0.4 mm pitch between antennas outputs and the two adjacent GND pads
- A microstrip trace with 1.0 mm length and 0.2mm wide in Isola Tachyon dielectric was also included
- Transition to the micro-strip trace included
- AN1, AN2 and AN3 are the RF outputs
- PWR pins were shorted to GND for simulation
- 3D EM simulation performed in CST

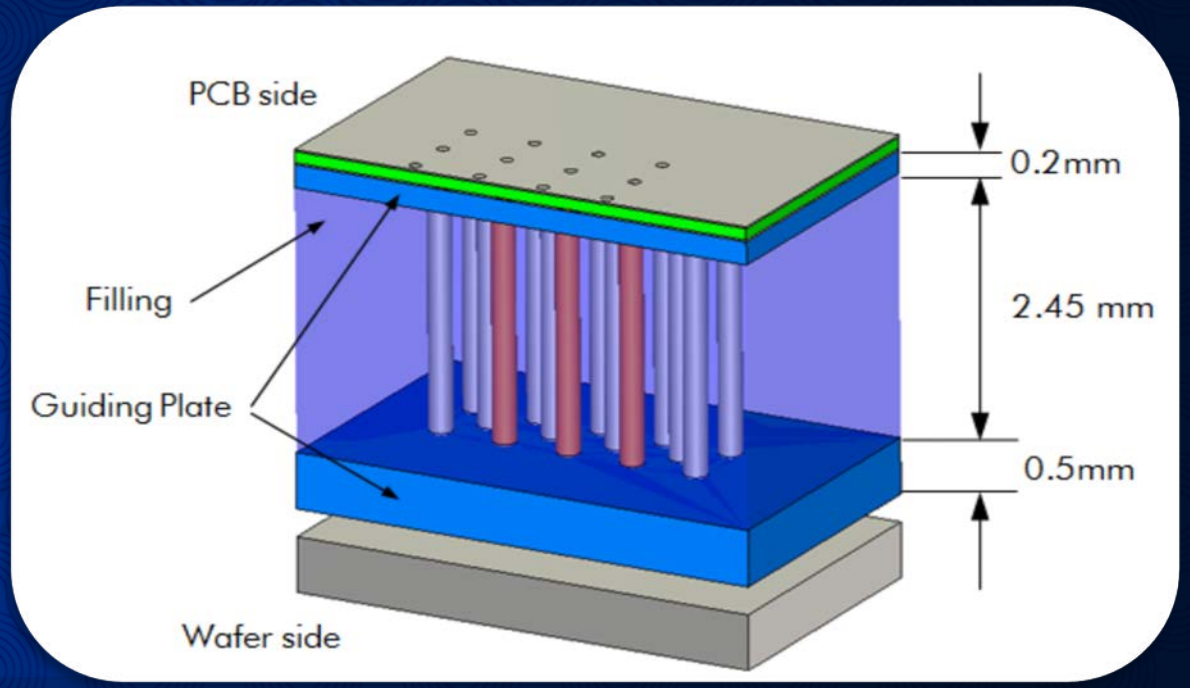
Probe Head Design Optimization

Before Optimization



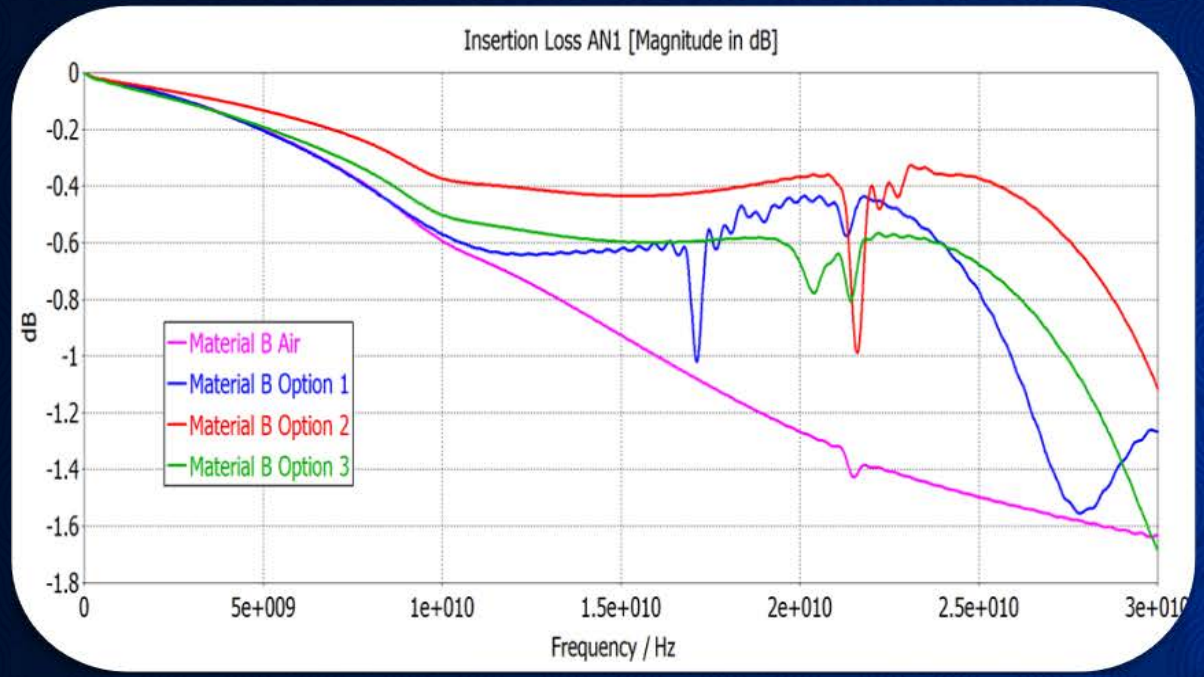
An initial probe head design with air as a filling between guiding plates

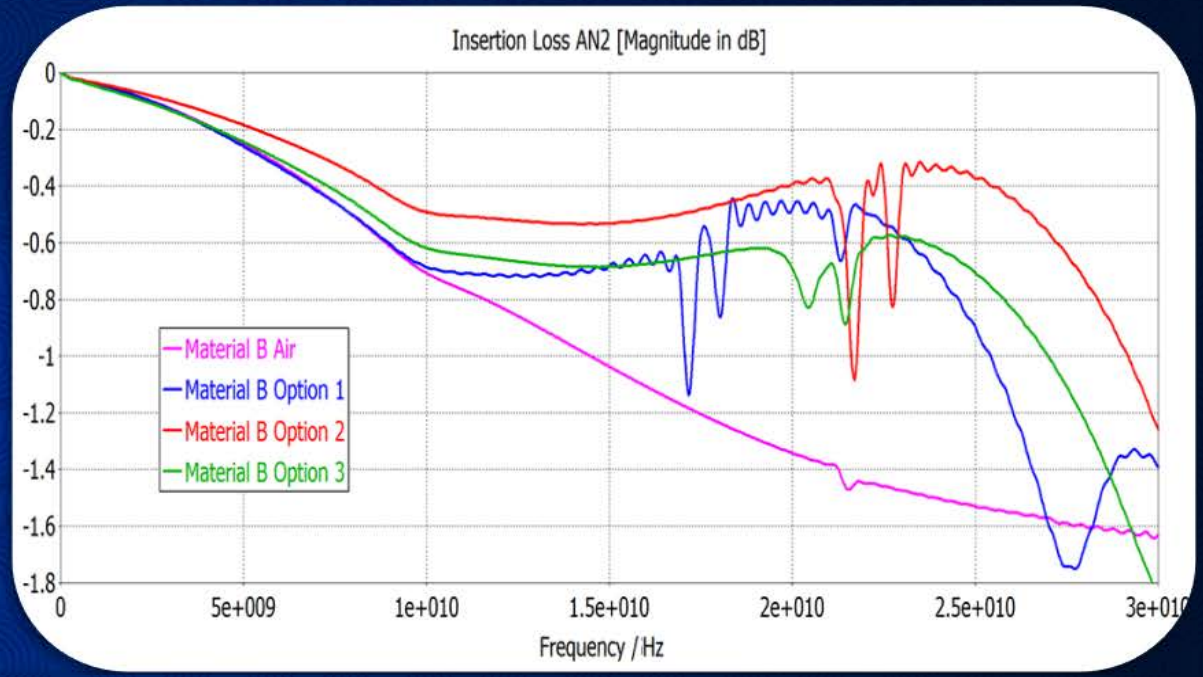
After Optimization



The optimized design with different filling materials and asymmetrical guiding plates

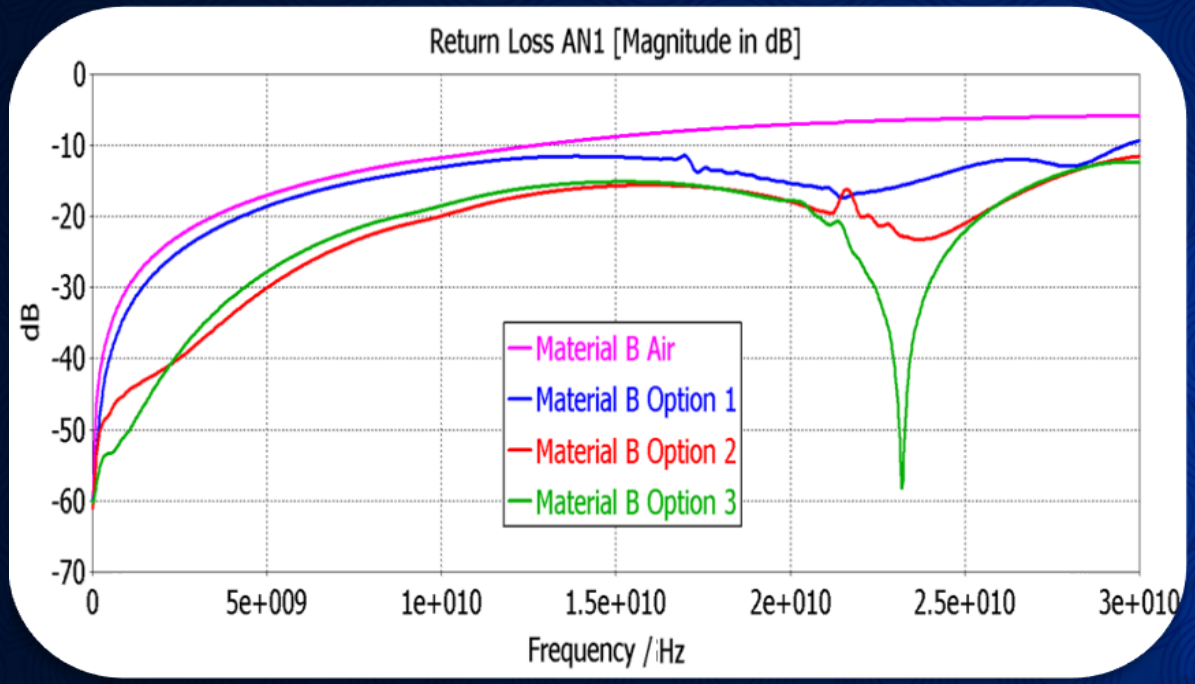
Insertion Loss Simulation Results

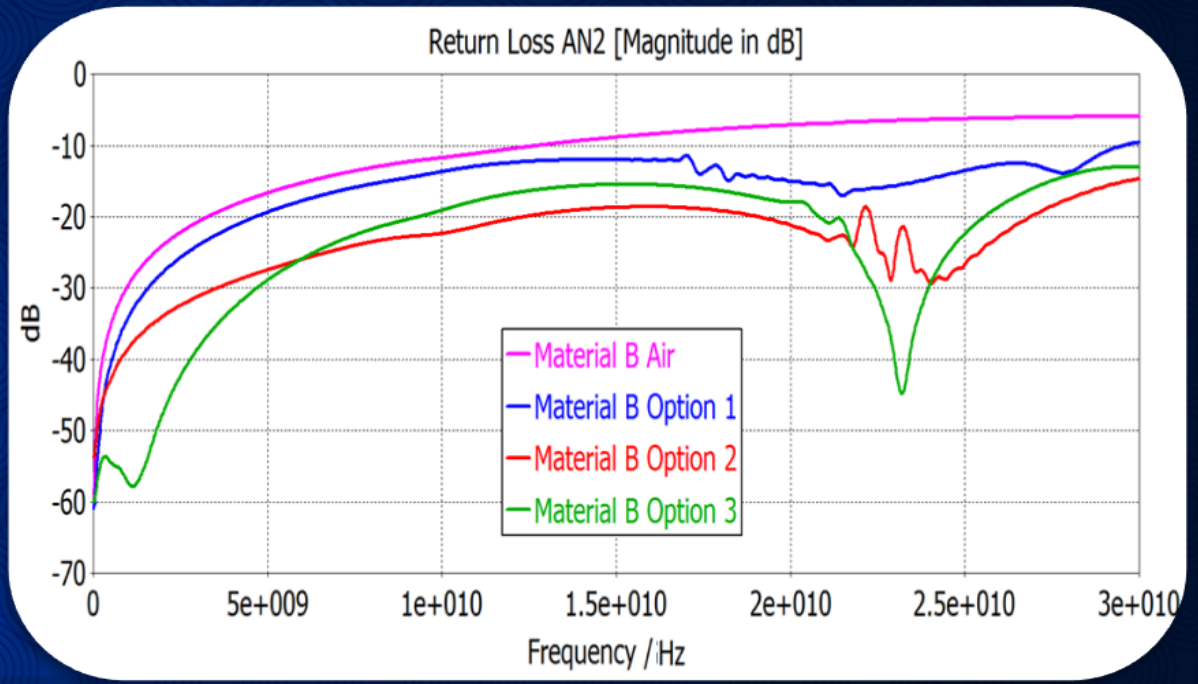




- Insertion loss can be compensated by the ATE system as long at it is measurable, stable and repeatable
- Note that the simulation only include a small length microstrip trace. A real probe card PCB would have a much longer PCB trace

Return Loss Simulation Results

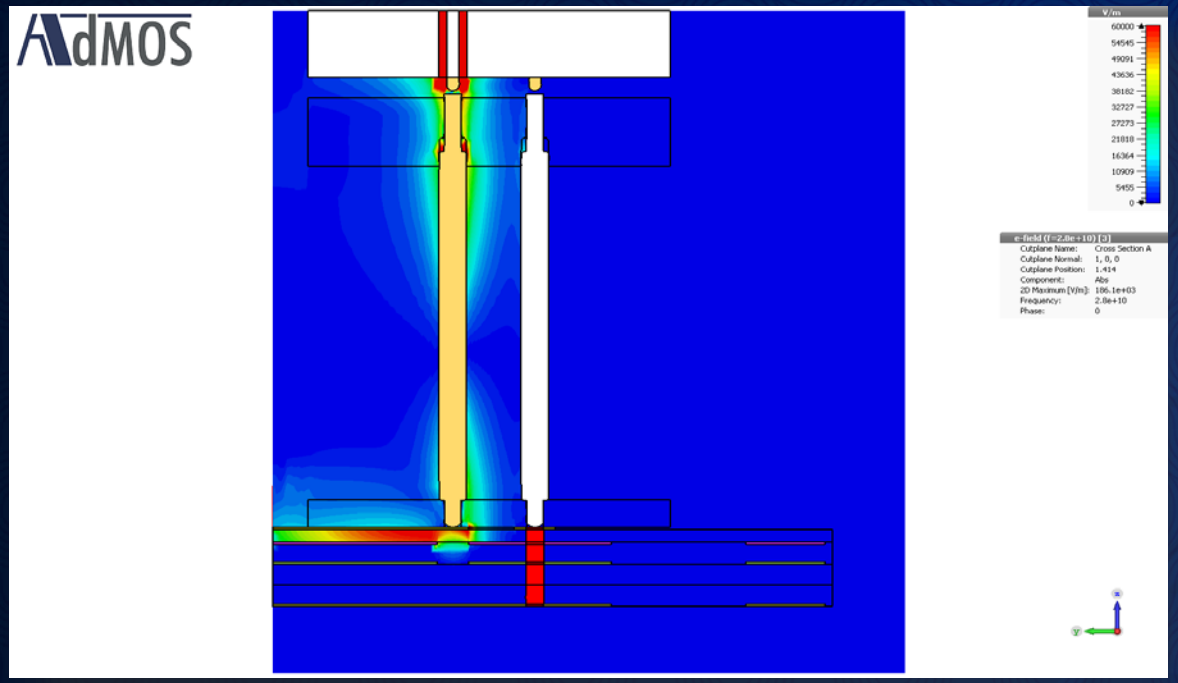




- Results for different probe head holder materials
- Air shows the worst results
- Return loss cannot be compensated by ATE system so it is critical to be minimized

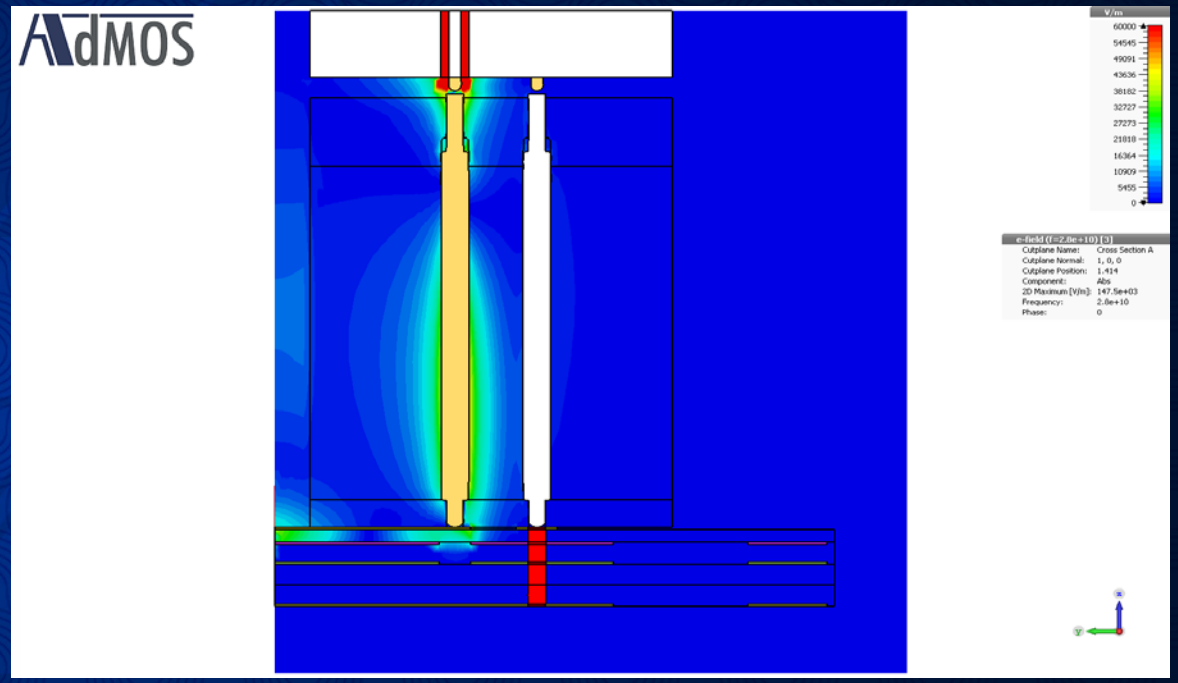
Animation of EM Field Intensity (28 GHz)

Air



- Max EM field intensity with air gap at 28GHz is 186k V/m

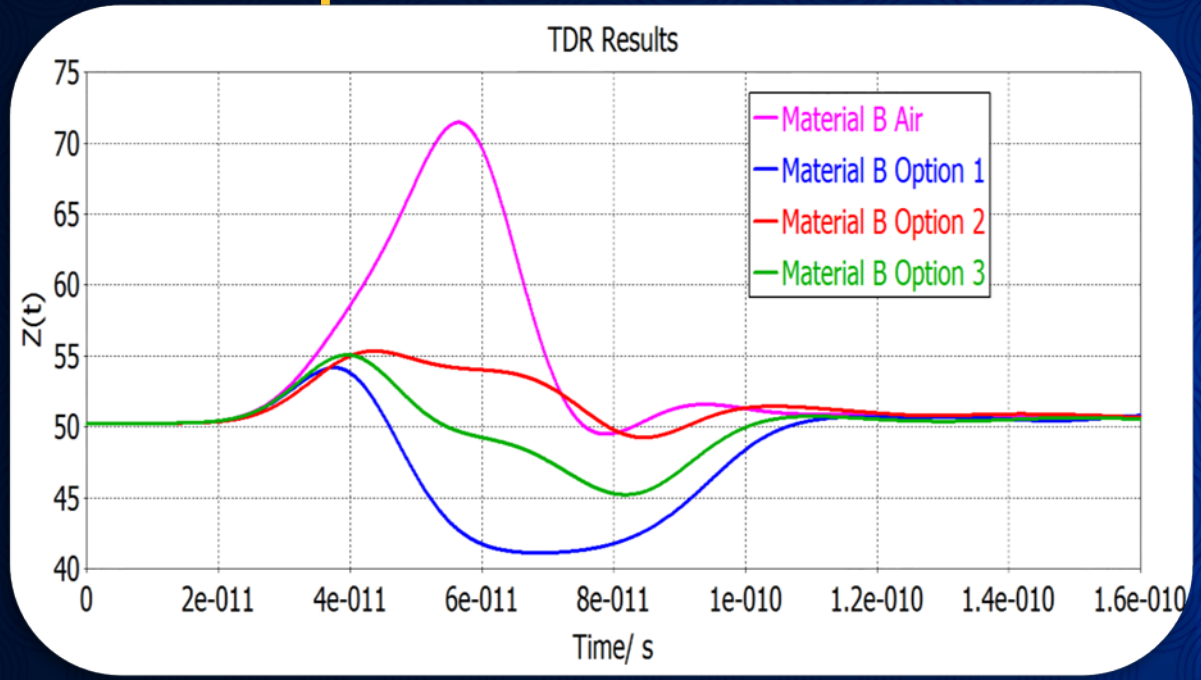
Material B Option 1



- Max EM field intensity with material B option 1 at 28GHz is 147k V/m

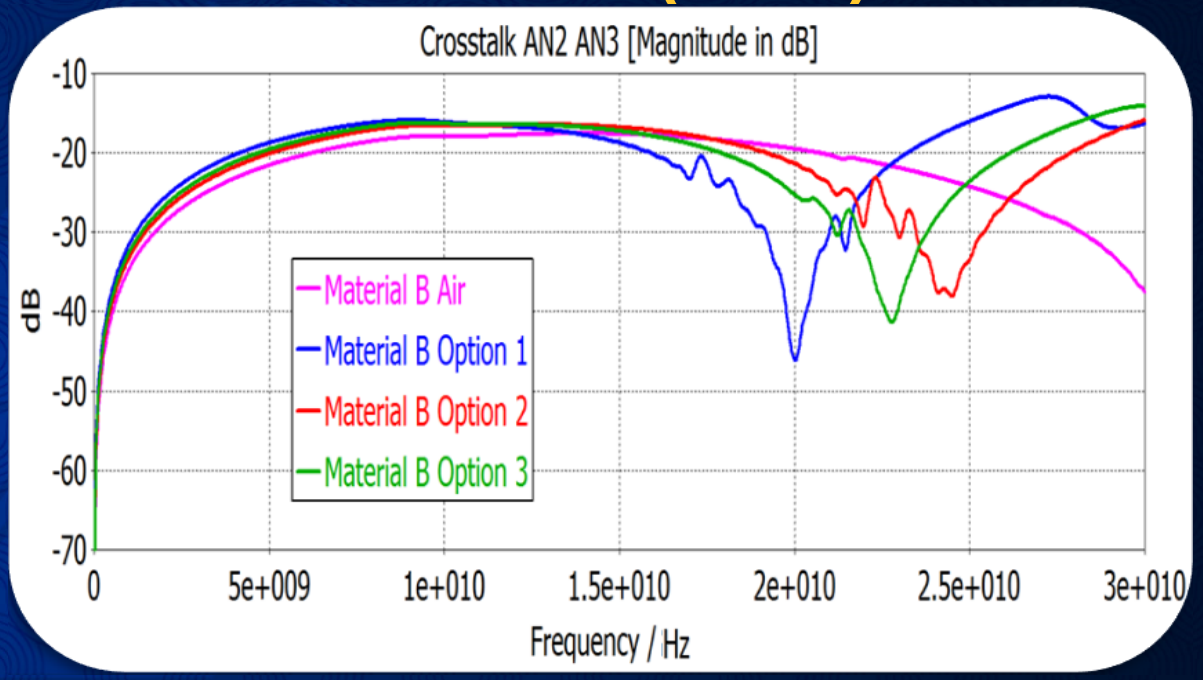
Simulation Results

TDR Impedance Results



- Impedance for different material options

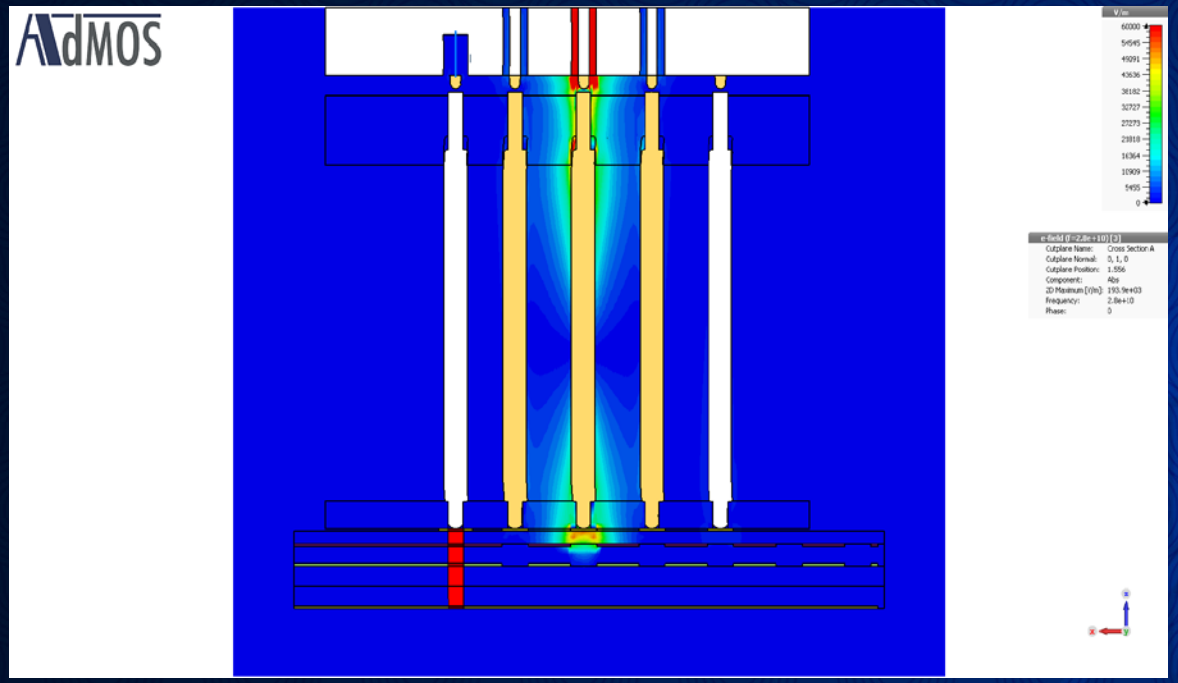
Crosstalk Results (NEXT)



- Crosstalk is high for 28 GHz for non-air probe heads
- High crosstalk is expected for a non-coaxial spring pin solution. This drawback can be addressed by testing one antenna at each time with the corresponding hit on test time

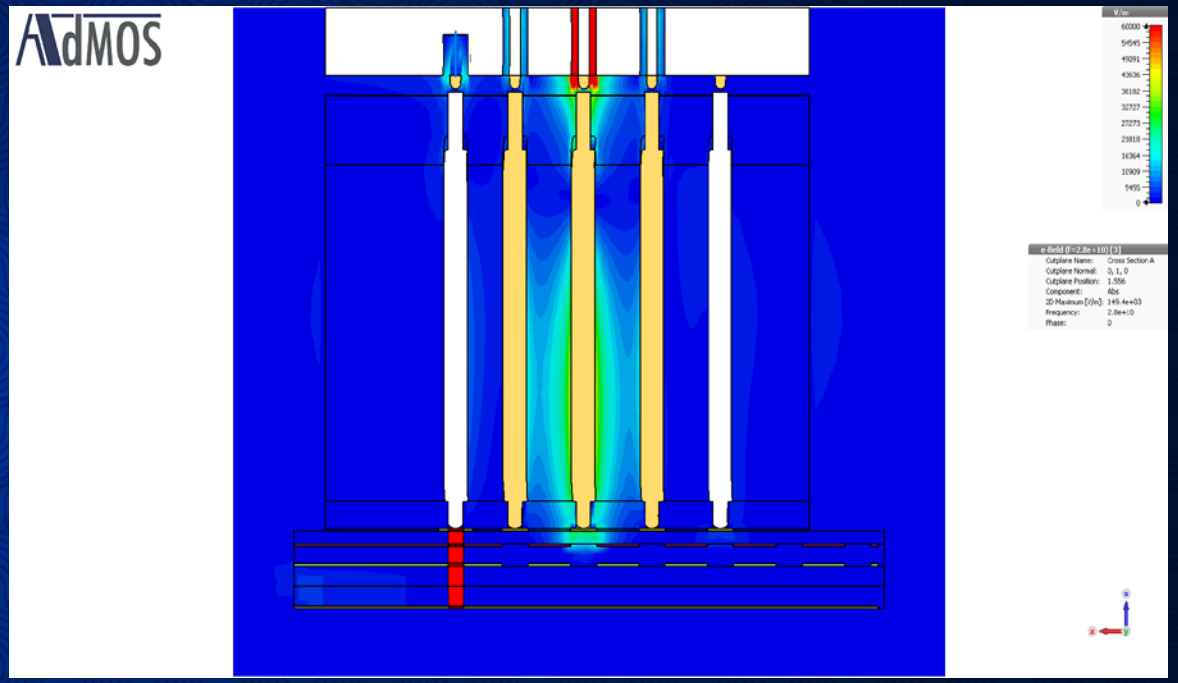
Crosstalk Field Animation at 28 GHz

Air



- Crosstalk max field intensity with air gap at 28GHz is 193k V/m

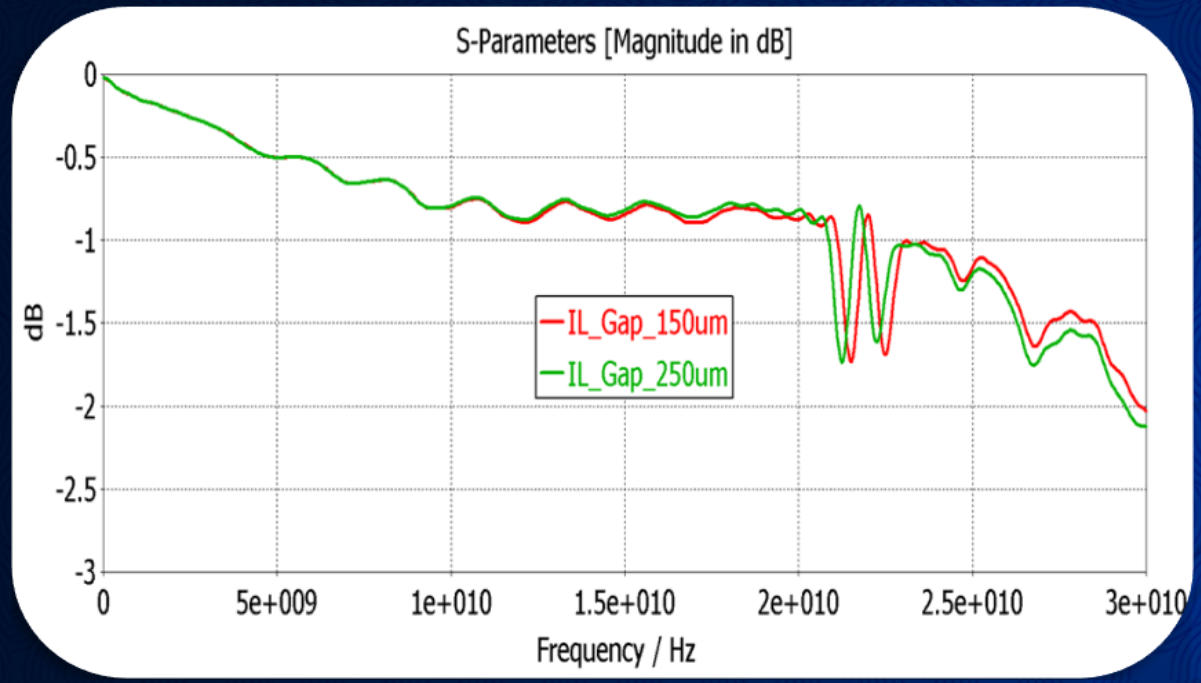
Material B Option 1



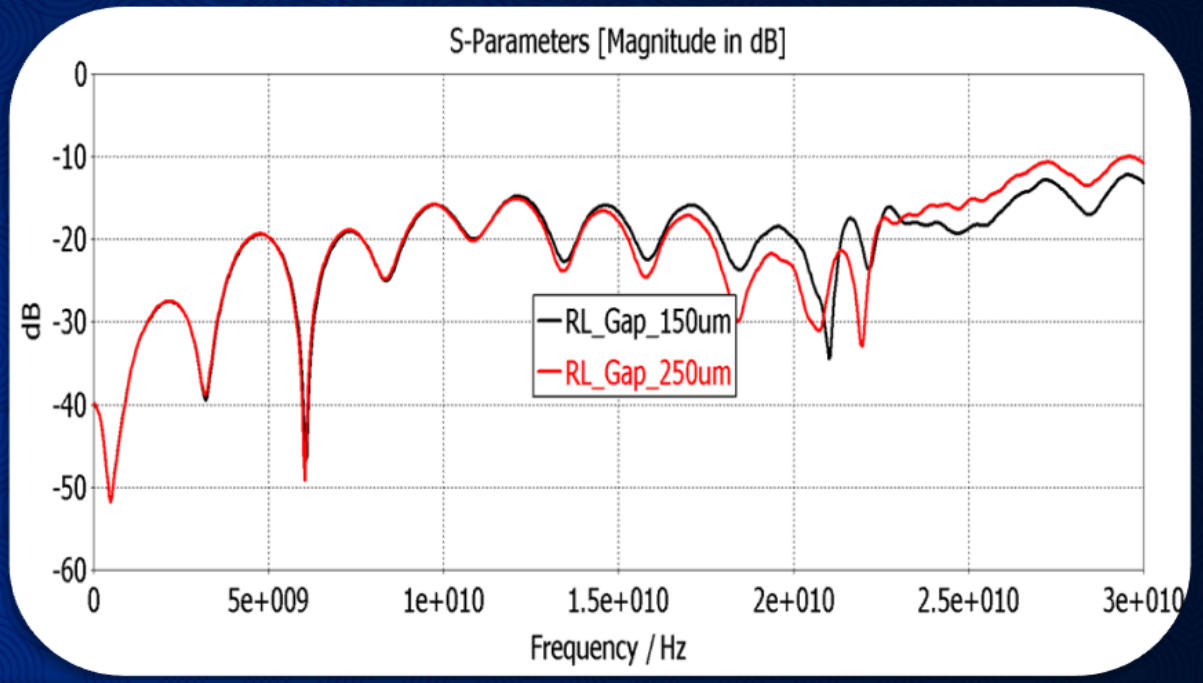
- Crosstalk max field intensity with material B option 1 at 28GHz is 149k V/m

Probe Head Air Gap Optimization

Insertion Loss



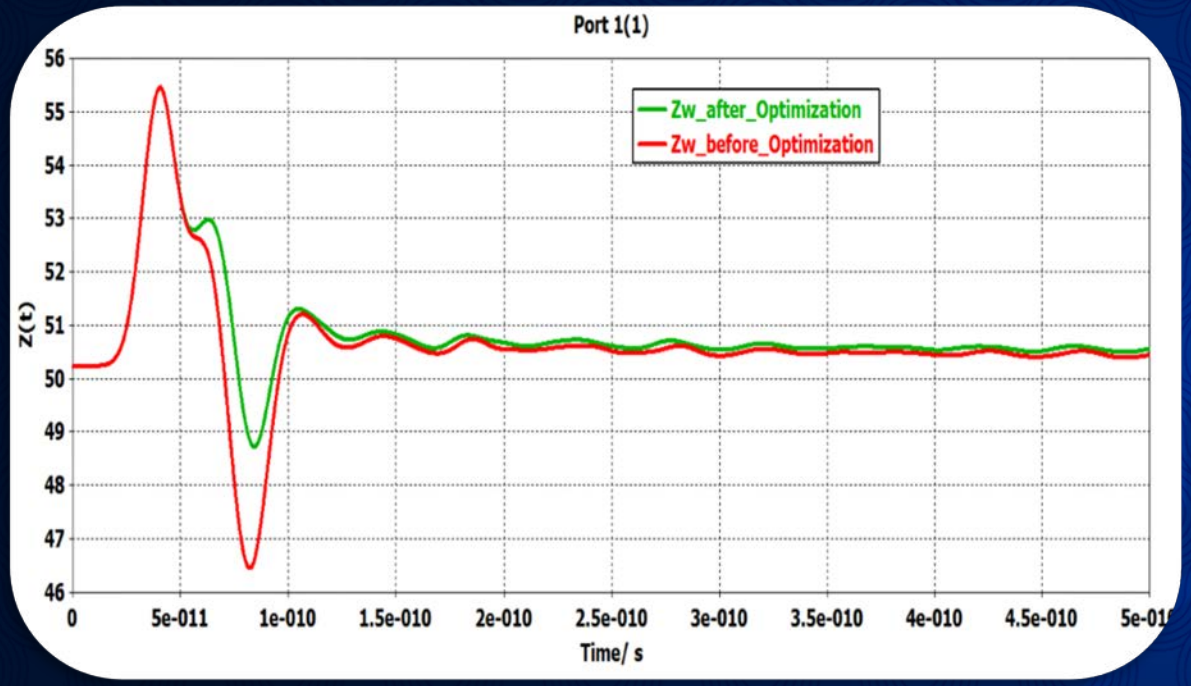
Return Loss



- Reduced air gap between probe head and wafer (probe extension) improves IL and RL at high frequency

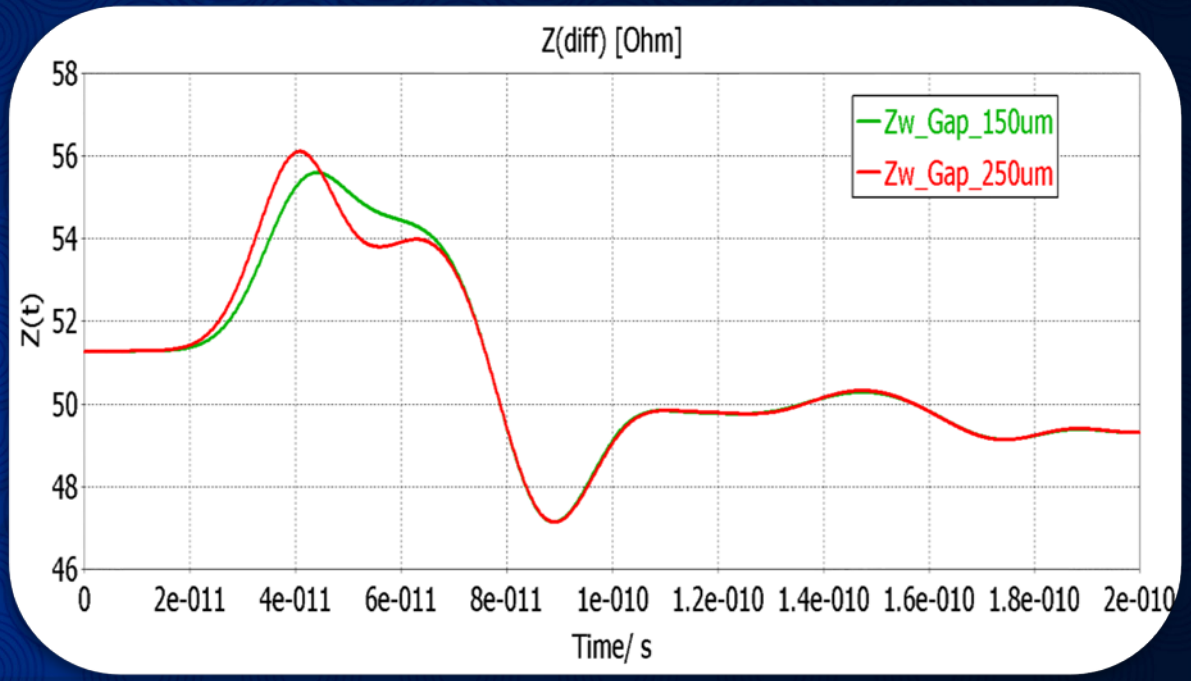
Probe Head Air Gap Optimization

Impedance before and after



- Because of the air gap between the wafer and the probe head body, a non-symmetrical guiding plate construction provides performance improvements as shown in this example

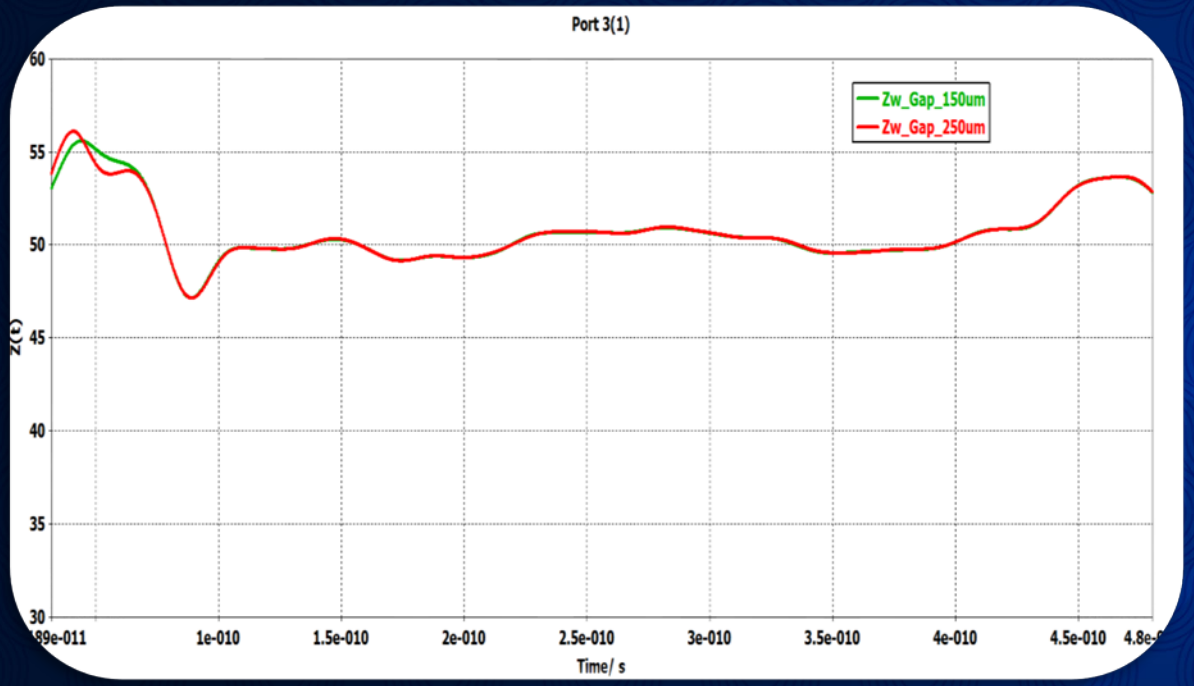
Impedance with different air gaps



- The air gap between the wafer and the probe head filling material are critical for impedance

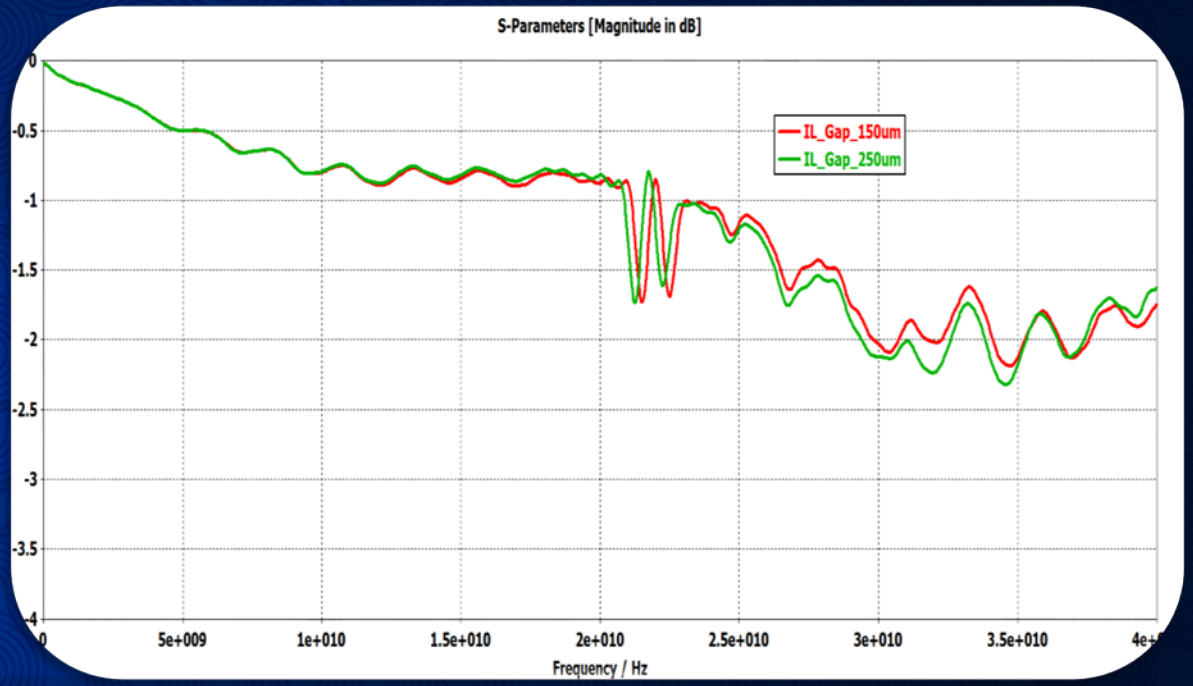
Probe Head Simulation up to 40GHz

Impedance



- TDR *Zw* with *Trise* 20ps
- The simulation was only performed for AN1, since the signal path corresponds to the worst case
- The optimization shows an improvement between 0.5-0.7Ω

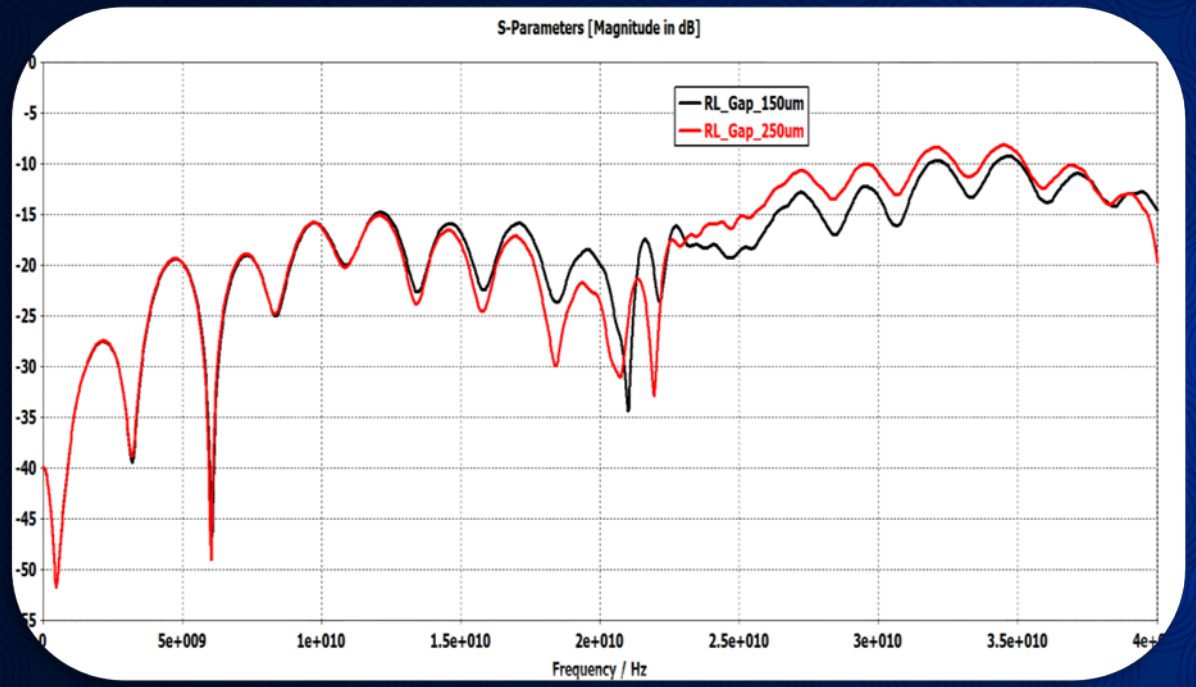
Insertion Loss for AN1



- ANT1 IL comparison for different air gaps between head and wafer

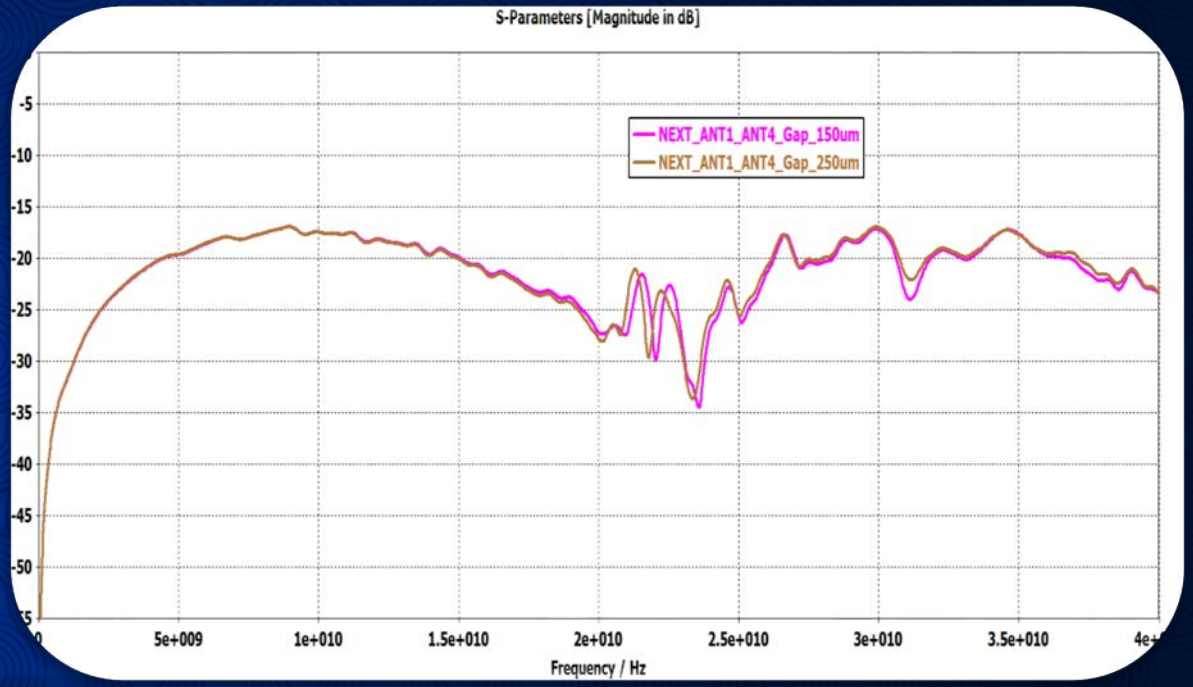
Probe Head Simulation up to 40GHz

Return Loss



- AN1 RL comparison for different air gap between head and wafer

Crosstalk NEXT AN1 and AN4



- AN1 & AN4 crosstalk comparison for different air gaps between head and wafer

Summary and Conclusion

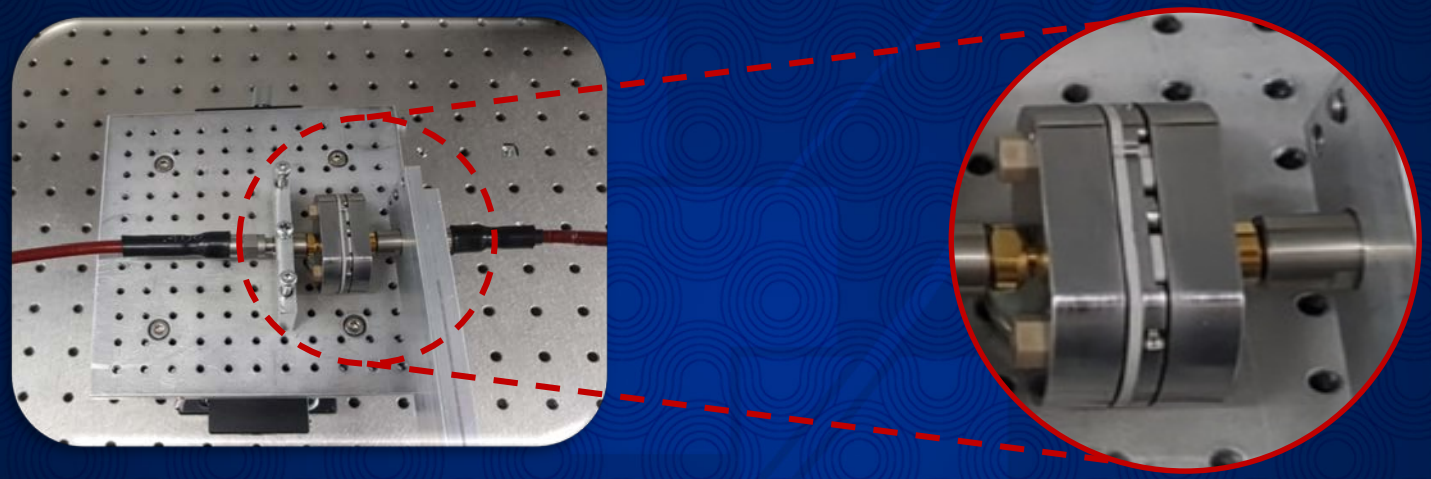
- The choice of the right probing solution for mmWave WLCSP applications like 5G depends on the performance objectives, volume, cost etc. There is no single right answer.
- The probe head only defines part of the test fixture performance, the probe card PCB signal trace and interconnect to ATE are also critical factors.
- Different optimization options of the probe head were presented and their impact analyzed. With a good model of the probe head it might also be possible to optimize the connecting micro-strip trace geometry to provide additional compensation
- The simulation results are showing a room for probe head design improvement especially to reduce the air gap which is crucial for impedance and signal integrity

Summary and Conclusion

- These simulation results provide a first indication of the feasibility of using a spring pin probe head for 5G WLCSP applications. The final proof is with the real DUT

Follow-On Work

- Verification study to confirm the simulation results



- Study of expected probe card PCB loss
- Testing of a FeinProbe® probe card at production environment

Thank You

LED Wafer Probe Test

Yoichi Funatoko
FormFactor

Taiwan, October 18-19, 2018

Overview

- Introduction
- Objectives / Goals
- Methods / Materials
- Results / Relevant Findings / Key Data
- Discussion of Results / Strengths / Weaknesses, etc.
- Summary / Conclusion
- Follow-On Work

LED Wafer Device Introduction

- **Focus on Small LED Die Size Probe Test**
  - Die Size < 50um
- **Small Bump Size**
  - Gold Bump Size < 10um
- **Tight Bump Pitch**
  - Bump Pitch < 40um
- **Wafer**
  - Warpage > 50um
  - Million Die per Wafer

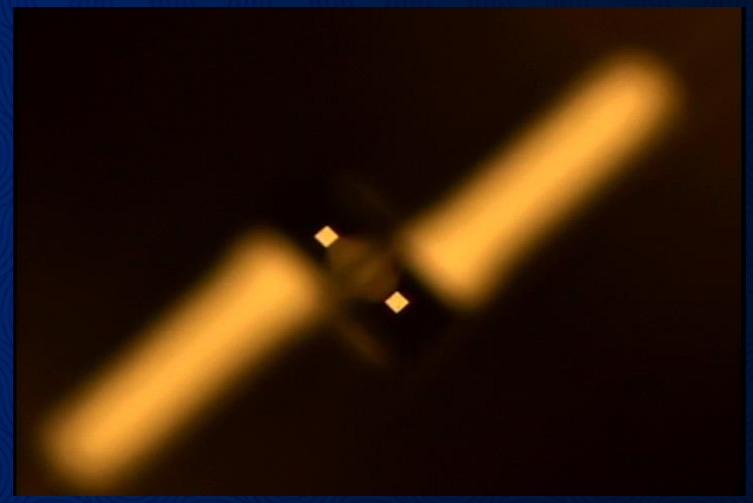
LED Wafer Probe Test Challenge

Item	LED Device Under Test	Probe Card	Prober
1	Gold Bump Pitch < 40um	Tight Pitch < 40um Probe	XY Chuck Stage Accuracy Probe to Tip Alignment Accuracy
2	Gold Bump Size < 10um	XY Tip Position Accuracy Low Scrub Ratio Contact Resistance	XY Chuck Stage Accuracy Probe to Tip Alignment Accuracy
3	Wafer Warpage > 50um	Over Drive Operating Margin Planarity	Contact Z Position Profile
4	Million Die per Wafer	Parallelism by Multi – DUT Probe Life Time	XYZ Contact Position Control Fast Indexing Speed
		Total Probing System XYZ Position Accuracy Probe to Pad Alignment Method	

Total Electrical Test Cost by Parallelism

Objectives

- **Develop Probing System for micro LED**
  - Probe Card Development and Evaluation
  - Total XY Position Accuracy +/- 4.5 um
    - Total = Probe Card and Prober
    - Probe Card and Prober Stage XY Accuracy
    - Probe to Pad Alignment Method
  - Actual Over Drive Control
    - Wafer Warpage > 50um
    - Actual OD Change by Temperature

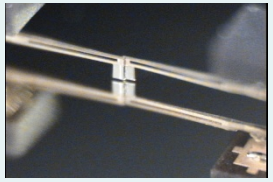
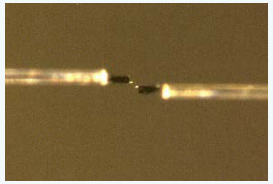
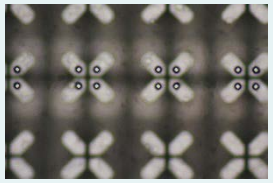
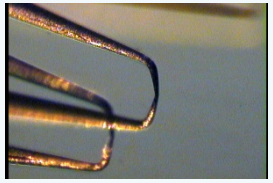


37um Pitch Probe

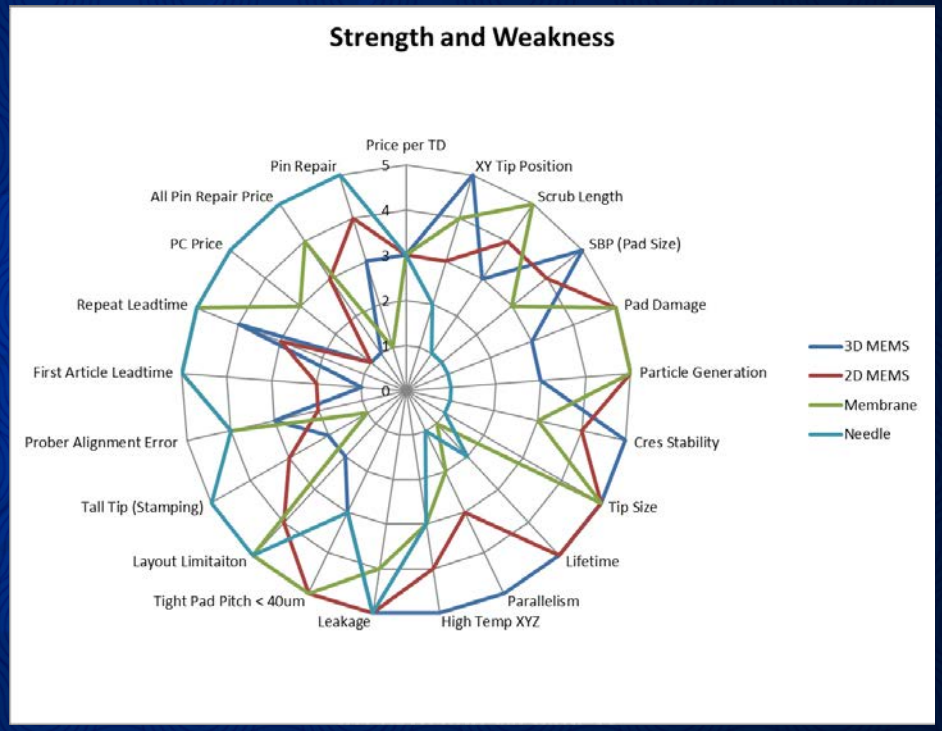
Total Probing System XYZ Position Accuracy Evaluation Methods / Materials

- **Probe Type**
  - 3D MEMS, 2D MEMS, Membrane, Needle
- **Probe Card**
  - 2DUT Intentionally Large Skip DUT Layout for Future Multi - DUT
- **Prober**
  - Probe to Pad Alignment Method
    - Probe to Pad Alignment Software Development
- **Wafer**
  - Customer Bump Pattern Wafer with Electrical Connection
    - Gold Bump Size < 3um for XY Position Accuracy Target +/- 4.5 um
- **Electrical Test**
  - Open / Short
  - 100,000 TD / Wafer

Probe Type Evaluation

Option		Probe Type
1		3D MEMS Cantilever
2		2D MEMS Cantilever
3		Membrane RBI
4		Needle

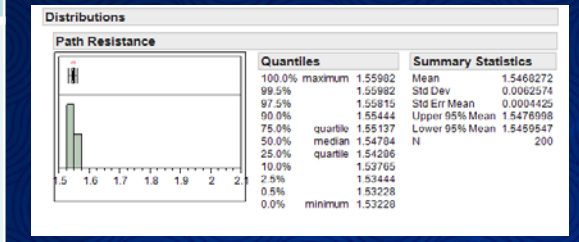
Advantage / Disadvantage

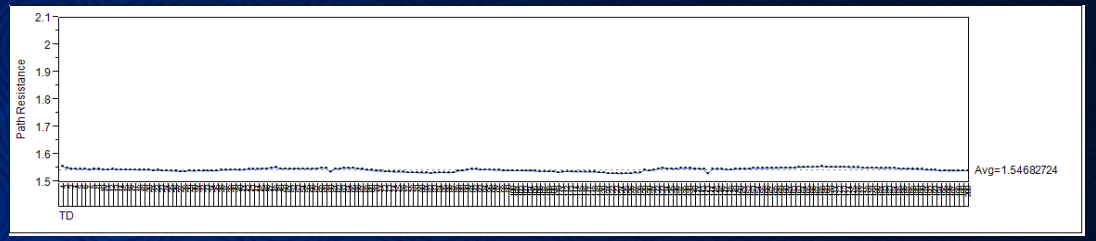


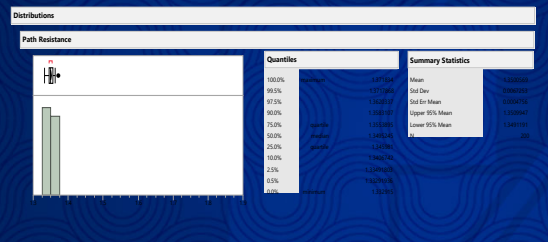
There is no perfect probe.

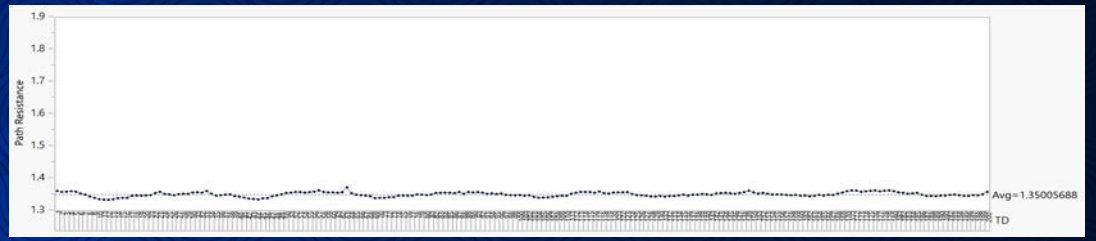
2Pin Path Resistance on Gold Wafer 200TD

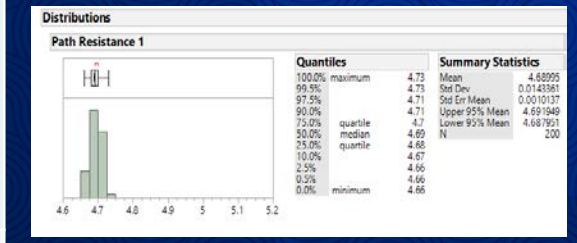
Option	Probe Type	Resistance Standard Deviation (Ohm)
1	3D MEMS Cantilever	0.006
2	2D MEMS Cantilever	0.007
3	Membrane RBI	0.014
4	Needle	0.064

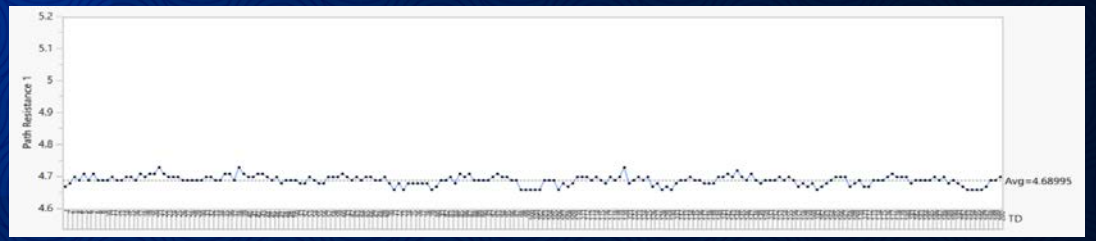


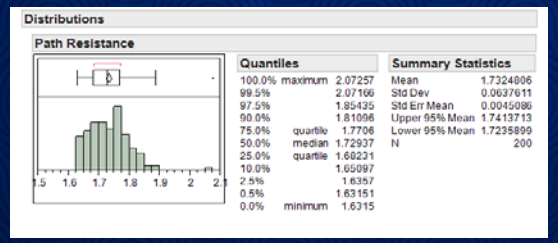


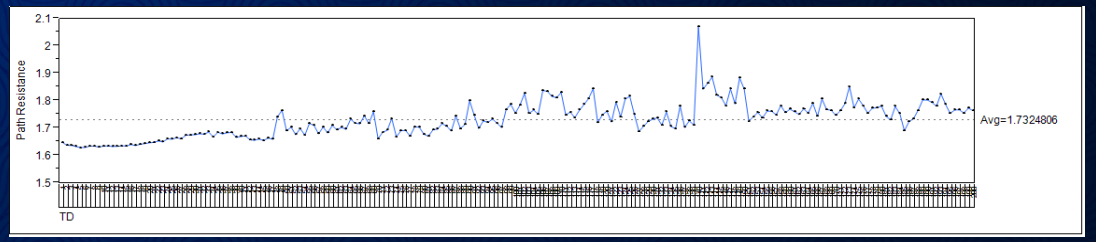




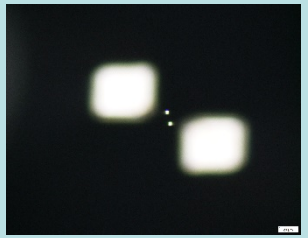
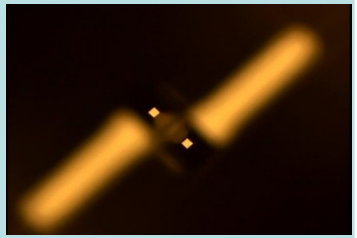




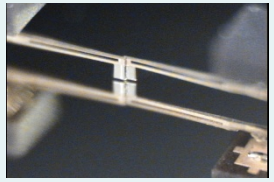
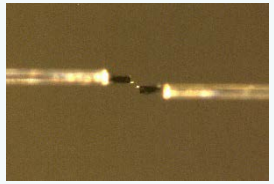
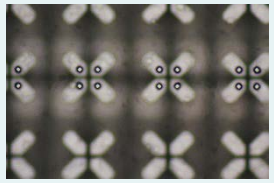
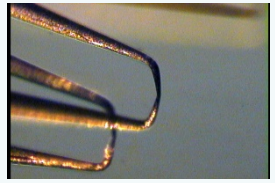




2D and 3D MEMS Cantilever Probe Card Tip Position

	2D MEMS Probe Card 	3D MEMS Probe Card 
Spring Fabrication Process	Lithography Lateral Direction Probe	Lithography Vertical Direction Probe
Tip Position	Spring and Ceramic Attach Process	Spring Fabrication Process
Typical XYZ Tip Position Accuracy 32DUT LED Probe Card	+/- 5um	+/- 1um
Card to Card XYZ Tip Position Error 32DUT LED Probe Card	+/- 5um	+/- 1um

Probe Type Evaluation

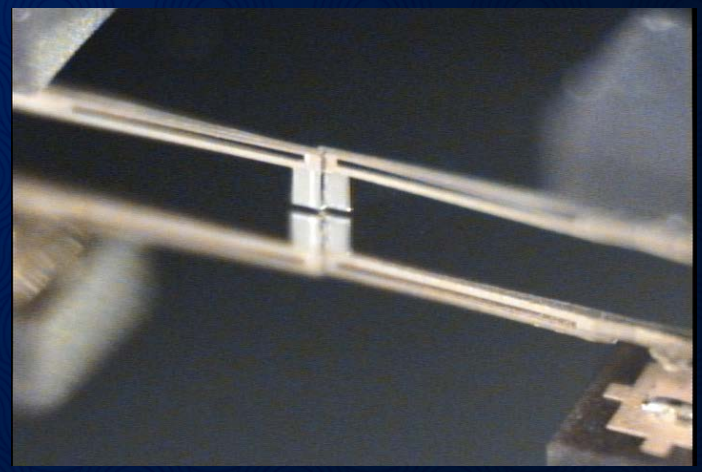
Option		Probe Type	Contact Resistance STD Deviation (Ohm)	XYZ Tip Position Accuracy	Card to Card XYZ Tip Position Error for Production	Probe Tip Alignment from Top Side
1		3D MEMS Cantilever	0.006	Typical +/-1um Excellent	Card #1 - #10 Same XY Tip Position	Need Development
2		2D MEMS Cantilever	0.007	Typical +/-5um	Different XY Tip Position for Card #1 - #10	Easy to Align
3		Membrane RBI	0.014	Typical +/-3um	Good XY Tip Position for Card #1 - #10	Difficult
4		Needle	0.064	Typical +/-5um	Large Variation	Easy to Align

3D MEMS Vertical Tip Probe to Pad Alignment

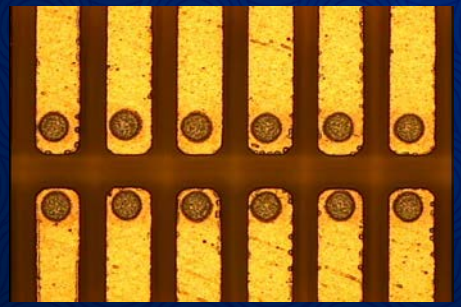
- **Prober**
  - No Upper Looking Chuck Camera
- **3D MEMS Cantilever Probe**
  - Tip Position at bottom of Beam
  - Beam Top Laser Mark XY Position Accuracy +/-5um
    - Not Acceptable for Total System XY Accuracy +/- 4.5um

Top View

Side View

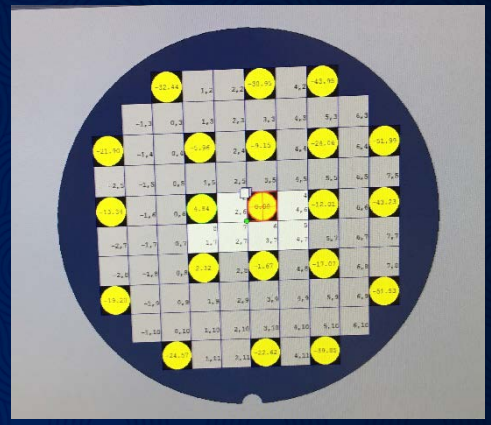


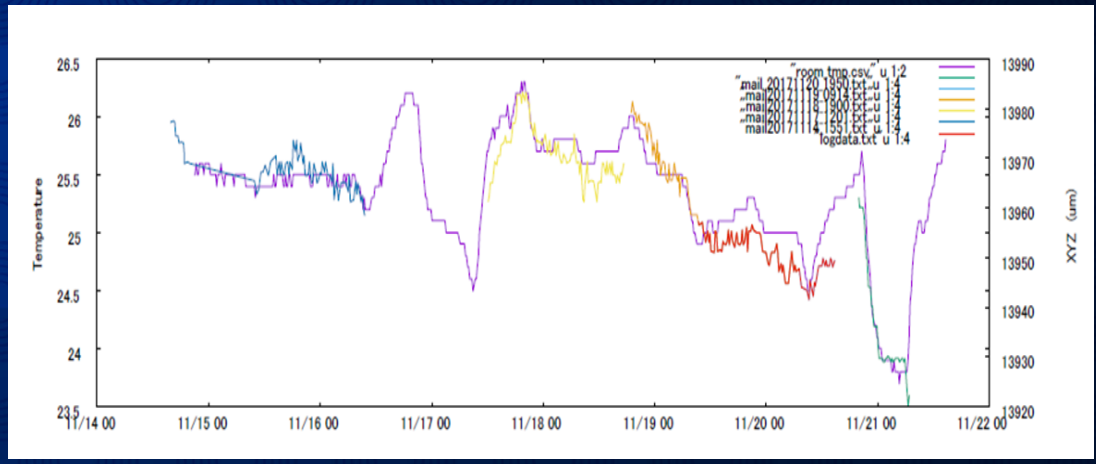
Laser Mark on Beam



Z Direction Probe to Pad Alignment Method 1

- **Optical Alignment**
  - Wafer Z Profile
    - > 21 Points Measurement for 50um Warp Wafer
    - 30 minutes!
  - Camera Position Move by Room Temperature Change
    - Aluminum (Camera Stage) : 23 ppm / deg C
    - FR4 (PCB) : 16 ppm / deg C
    - Ceramic (Probe Head) : 6 ppm / deg C



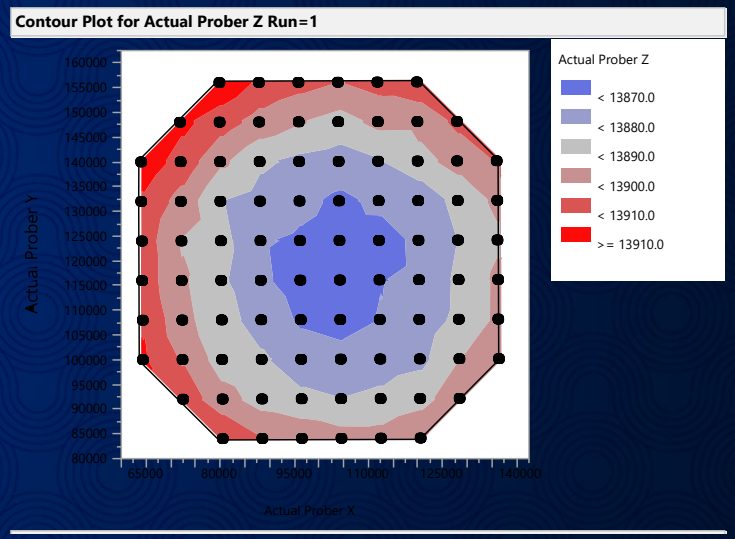


Temperature Changed 2 degree C in 7 days
Contact Z Position Changed 60um

Z Direction Probe to Pad Alignment Method 2

- **Electrical Alignment**
  - Accurate First Electrical Contact Z Position
    - Accurate Probe Tip Z and Wafer Z Position
  - 88 Location / Wafer
    - Do not require optical wafer Z profile
  - Need Electrical Tester
    - Need to control arcing

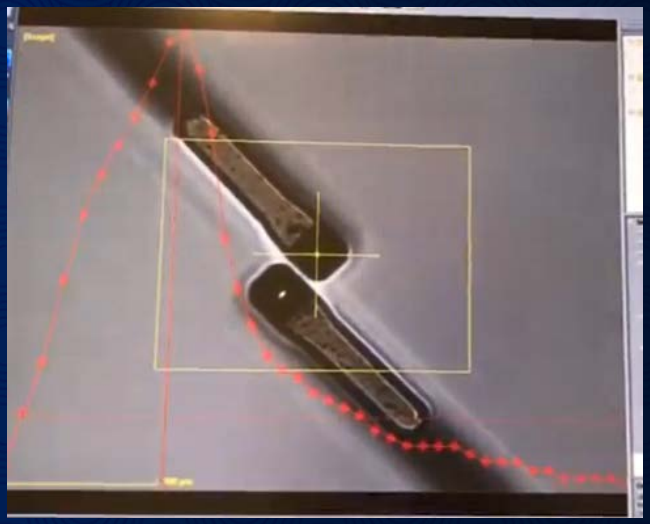
First Electrical Z Position Contour Plot



XY Direction Probe to Pad Alignment Method 1

- **Optical Alignment**
  - Use Chuck Mirror to Align 3D MEMS Probe
  - Alignment Accuracy Depends on Tip Condition
    - Tip Size
    - Clean / Dirty Tip by Particle
    - Smooth / Rough Tip Surface
  - Fast Alignment Time (Need to Focus Z)

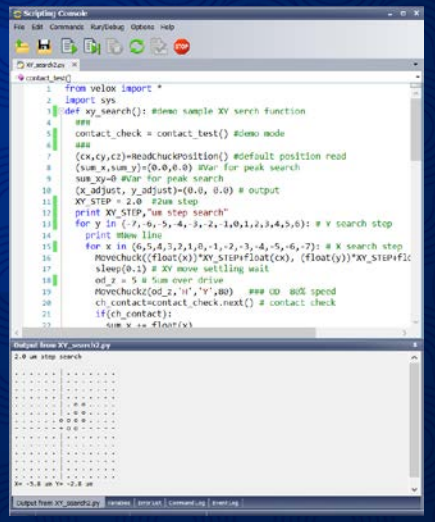
Top Side Microscope View using Chuck Mirror



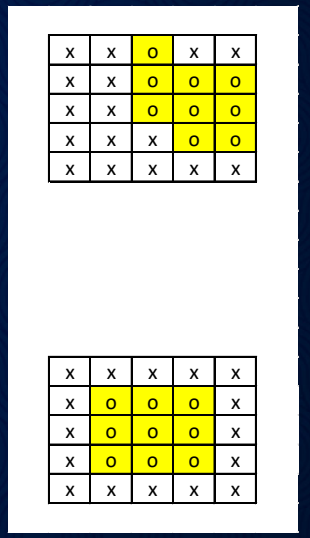
XY Direction Probe to Pad Alignment Method 2

- **Electrical Alignment**
  - 2 or 3um Stepping Electrical Contact
    - Python Script Development to Control Stage and SMU
  - Accurate XY Position Alignment

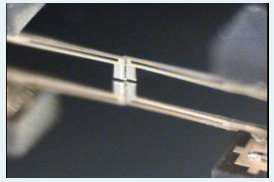
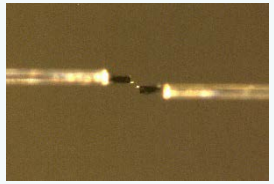
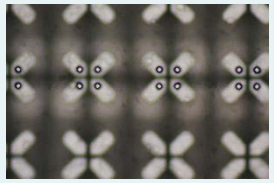
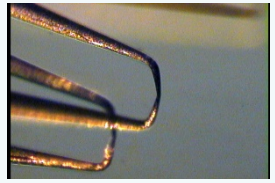
Python Script



3um Step Electrical Contact Position

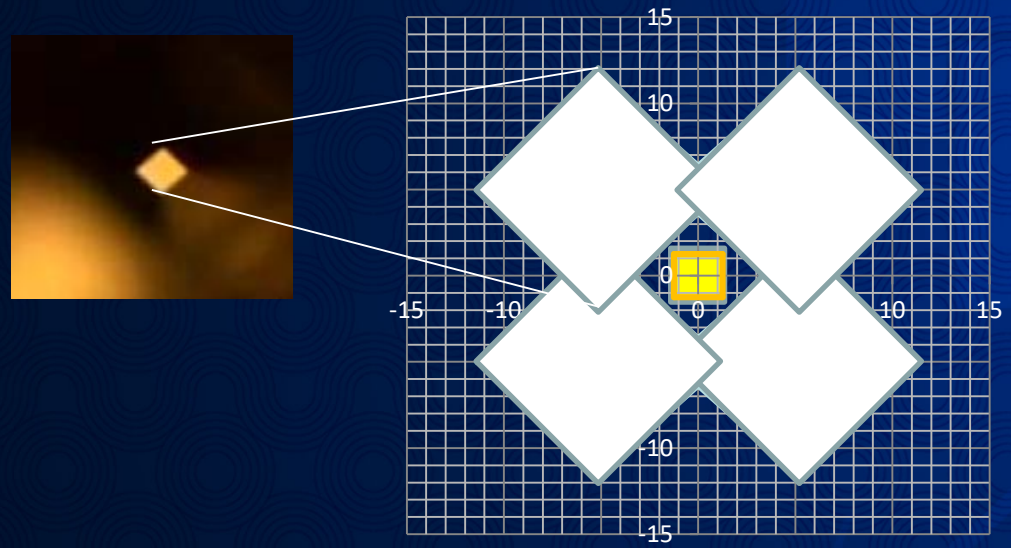


Probe Type Evaluation

Option		Probe Type	Contact Resistance STD Deviation (Ohm)	XYZ Tip Position Accuracy	Card to Card XYZ Tip Position Error for Production	Probe Tip Alignment from Top Side
1		3D MEMS Cantilever	0.006	Typical +/-1um Excellent	Card #1 - #10 Same XY Tip Position	Developed XYZ Electrical Alignment
2		2D MEMS Cantilever	0.007	Typical +/-5um	Different XY Tip Position for Card #1 - #10	Easy to Align
3		Membrane RBI	0.014	Typical +/-3um	Good XY Tip Position for Card #1 - #10	Difficult
4		Needle	0.064	Typical +/-5um	Large Variation	Easy to Align

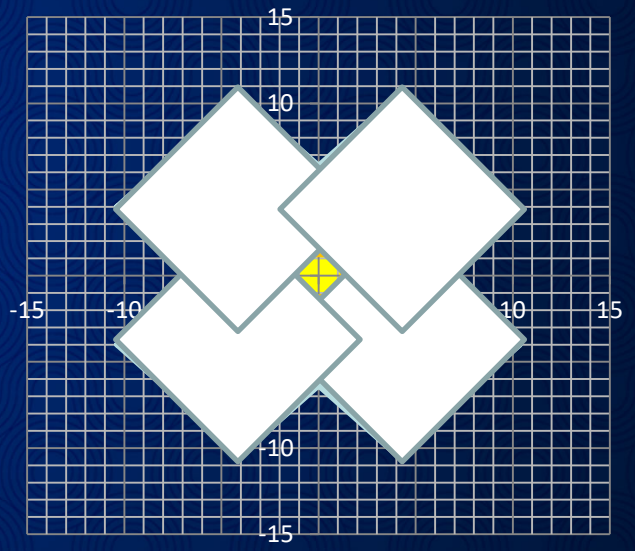
XY Tip Position Error and Contact Test Wafer Bump Size

- **XY Error +/- 5um : Open**



Gold Bump Size < 3um

XY Error +/- 4um : Short



XYZ Probe to Pad Alignment and 100,000TD Contact Test Result

Method	Z Probe to Pad Alignment	Actual OD Control Result	XY Probe to Pad Alignment	XY Probe to Pad Alignment Result
1	Optical Z Profile 18 Location / Wafer	Open Failure Contact Z Point Changed by Temperature	Optical	Alignment Error by Tip Condition
2	Electrical First Z Contact 88 Location / Wafer	Pass 100,000 TD	Electrical 3um Step Search	Pass 100,000 TD

Findings : Alignment Error and Cleaning

- **Optical Alignment**
  - Probe Tip Location Error by Particle and Tip Condition
  - Need Cleaning to Avoid Alignment Error

- **Electrical Alignment**
  - No XYZ Tip Position Error by Tip Condition
  - No Cleaning Required

Conclusion

- **Successfully Developed Total Probing System for Micro LED Wafer Test.**
- **Developed New 3D MEMS Cantilever Probe to Pad Alignment Method. Electrical XYZ Alignment Method Pass 100,000TD Contact Test on <3um Gold Bump.**
- **Engineering Prober is very Flexible to Develop New Alignment Algorithm.**

Follow on Work

- **Increase Probe Card Parallelism to > 32DUT and Release for Production**
- **Develop < 20um Pitch Probe Card**

Acknowledgements

- **FormFactor Team Member**
  - Masahiro Sameshima
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  - Shinpei Yoshida
  - Kazuyuki Kaname
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  - Nobuhiro Kawamata

Improve the Accuracy of High Speed Simulation to Meet 56G/112G Testing Requirement on PCB

Jackie Luo

ZENFOCUS
上海泽丰半导体科技有限公司

Taiwan, October 18-19, 2018

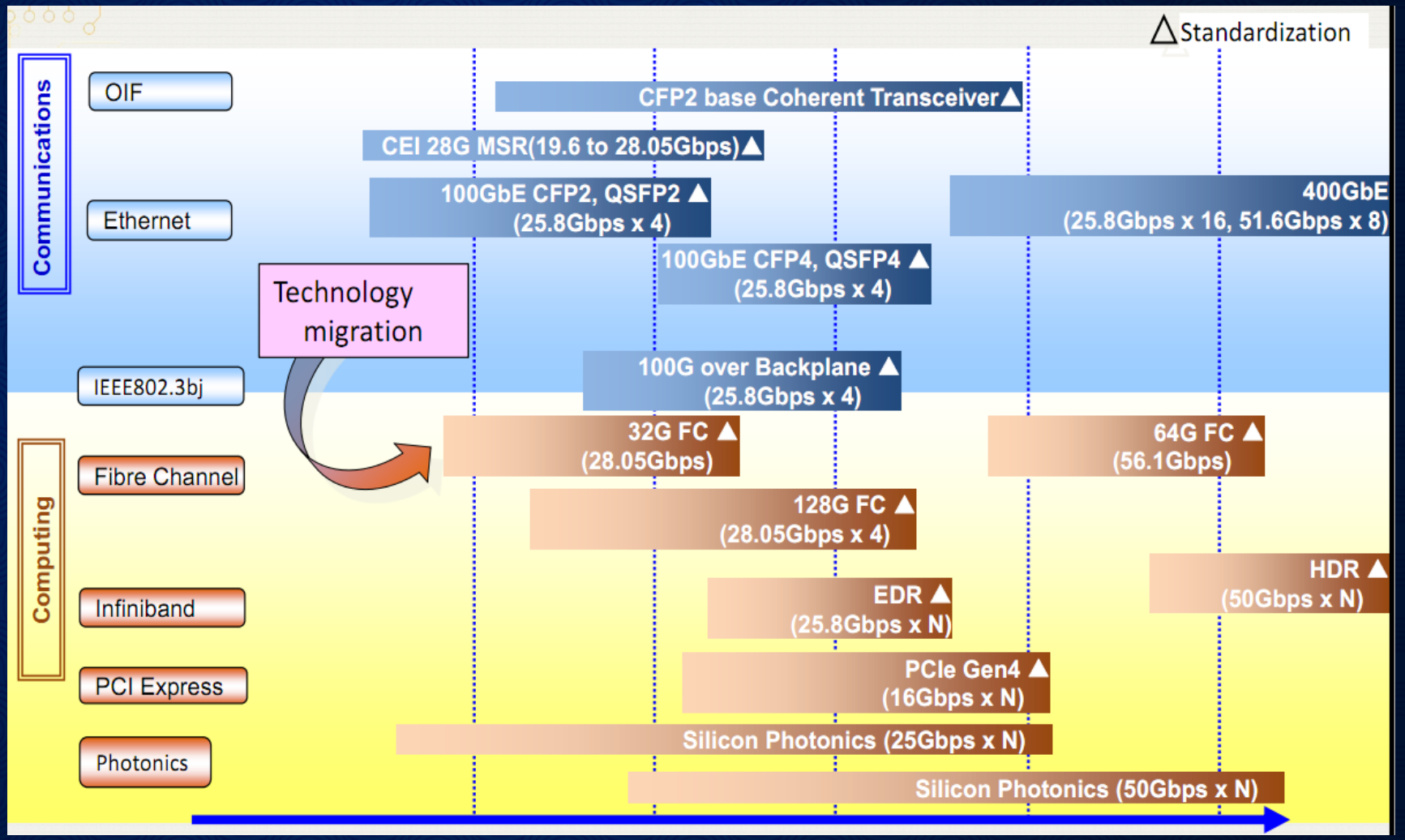
Overview

- Development of High Speed Interface
- PAM4 and NRZ
- Accurate factor in simulation
- Research board introduction
- Case Study
- Summary & Future work

Development of High Speed Interface

Released recently

- **IEEE802.3bs**
- **OIF-CEI-04.0**



PAM4 and NRZ

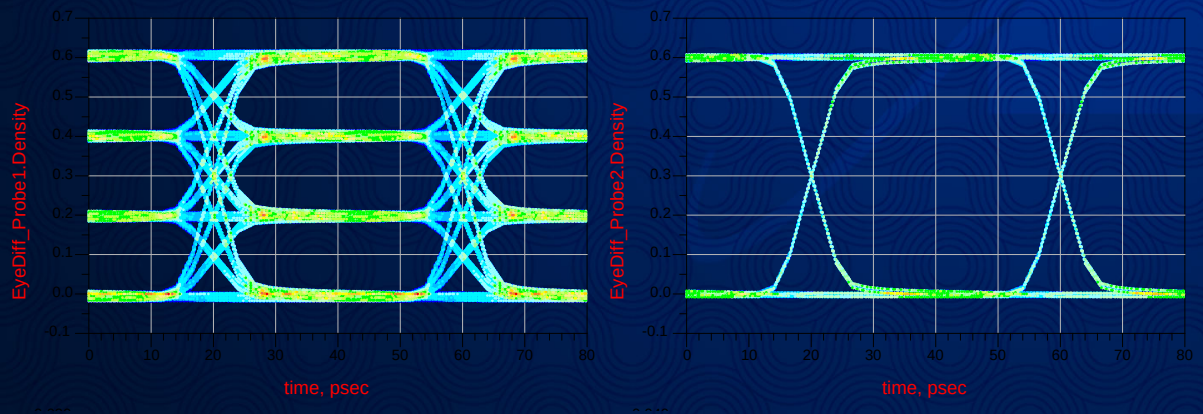
NRZ and PAM-4 are compared on the following points

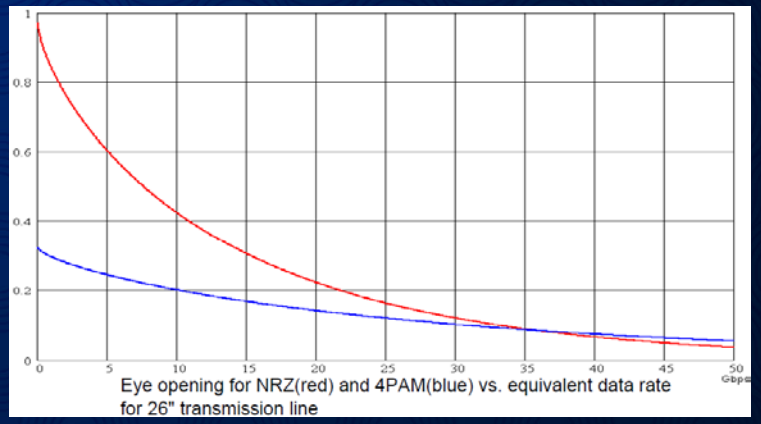
- **Vertical Eye Opening (Differential Amplitude)**
- **Horizontal Eye Closure (Unit Interval minus Jitter)**
- **Crosstalk Budget (Difference between amplitude of Noise Aggressor and Signal of Noise Victim)**

PAM4 and NRZ

NRZ and PAM4 are compared on the following points

- **Vertical Eye Opening**
  - Channel loss rises with frequency: Lower baud rate of PAM-4 implies less loss in channel
  - PAM-4 launch amplitude per signal level is 33% of NRZ for equivalent driver technology and supply voltage
  - At lower frequencies: Higher launch for NRZ provides greater vertical eye opening.
  - At higher frequencies: Lower loss for PAM-4 (because baud rate is 1/2 that of NRZ) compensates for lower launch voltage and results in greater vertical eye opening.





PAM4 and NRZ

	NRZ	PAM-4
Total Cycle (11.1 Gbps)	90 ps	180 ps
Total Jitter	(0.30 UI) 27 ps	(0.27 UI) 48 ps
Loss in Eye Width for PAM-4	0 ps	(0.33 UI) 60 ps
Eye Opening at Tx	(0.70 UI) 63 ps	(0.40 UI) 72 ps

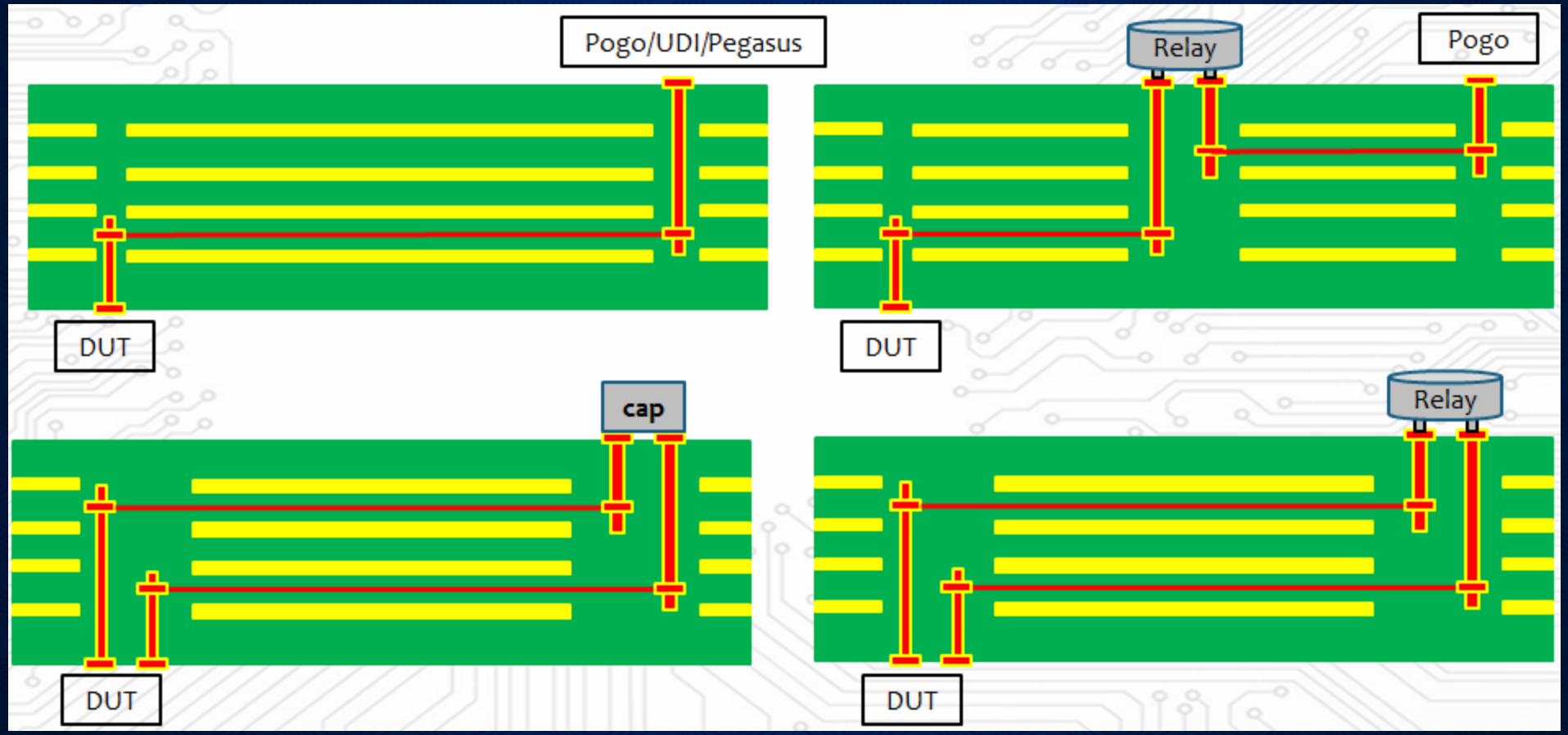
- **Horizontal Eye Closure**
  - Lower baud rate means more eye width due to base cycle.
  - DJ/RJ at the transmitter are related to spectrum of the transmitted signal and tend to scale with baud rate.
    - Implies that absolute value of DJ/RJ for half baud rate design would be 2x that of full baud rate design.
    - With careful design should be able to achieve DJ/RJ for half baud rate design of 1.8x that of full baud rate design.
  - PAM-4 results in additional loss in 33% of eye width due to switching between adjacent and non-adjacent levels.
  - Combination of effects will result in larger horizontal eye opening for a PAM-4 solution at transmitter output. *But eye opening for PAM-4 is not twice as large as NRZ as would be implied from baud rate difference.*
  - Spectrum of this jitter component is near the frequency of the baud rate, substantially above the bandwidth of the channel.
  - *Transmit jitter with this spectrum is particularly susceptible to phase noise amplification by the channel.*

PAM4 and NRZ

- **Crosstalk Budget**
  - Crosstalk is a substantial contributor to jitter at the receiver.
  - PAM-4 maximum signal swing is similar to NRZ and therefore the noise level from the aggressor signal is the same for both PAM-4 and NRZ.
  - PAM-4 vertical eye opening is 33% of NRZ and therefore the victim signal's tolerance for crosstalk is less.
  - Crosstalk budget for PAM-4 therefore starts out 9 dB less than for NRZ.
  - Greater channel attenuation at higher frequencies reduces this advantage for NRZ to the 3-6 dB range (depending on channel design).

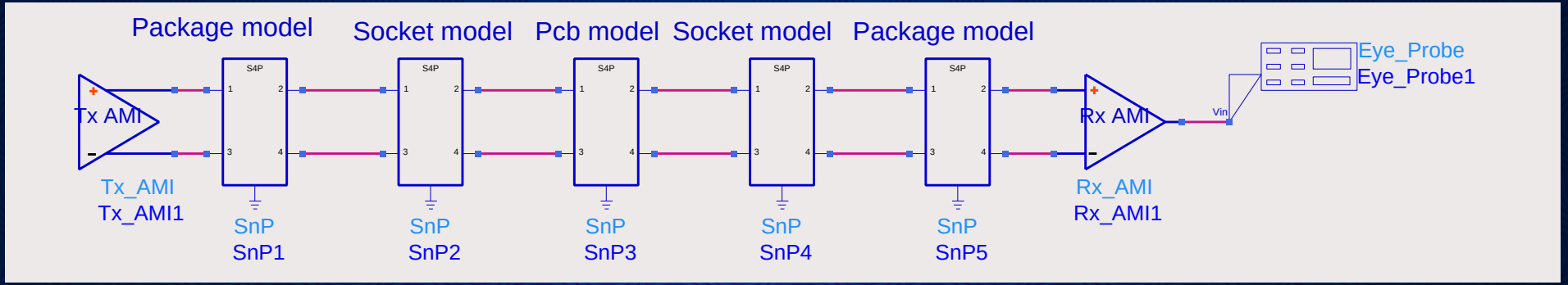
High speed signals in Test PCB

- **The signals shown in the below figures are all differential pairs.**

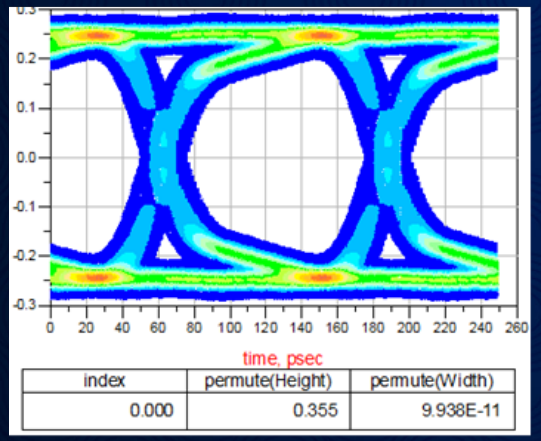


How the data rate affect the signal?

- **Date rate ↑ Eye width ↓ Eye high ↓ Eye Jitter ↑**

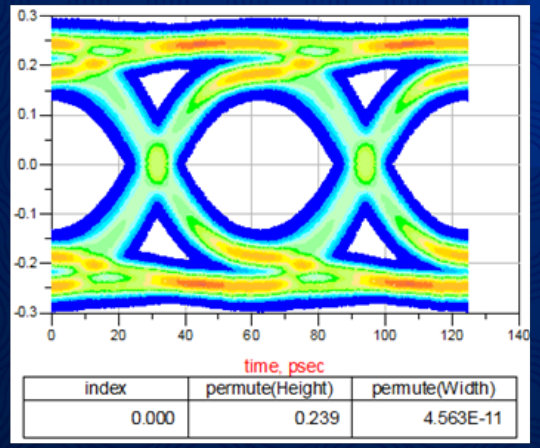


8Gbps



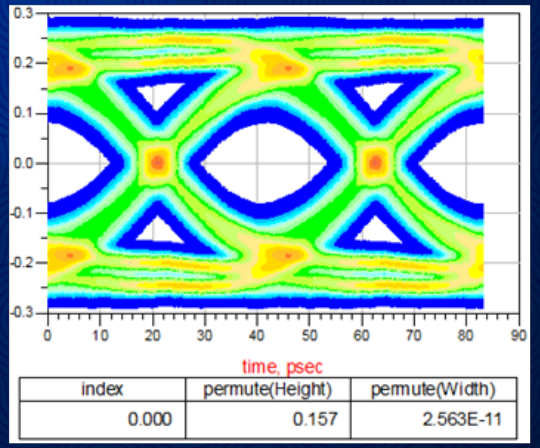
index	permute(Height)	permute(Width)
0.000	0.355	9.938E-11

16Gbps



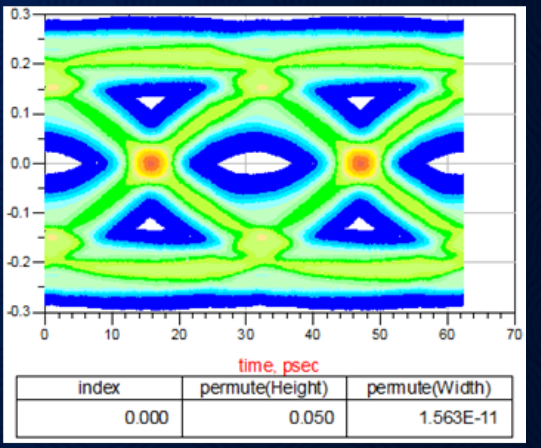
index	permute(Height)	permute(Width)
0.000	0.239	4.563E-11

24Gbps



index	permute(Height)	permute(Width)
0.000	0.157	2.563E-11

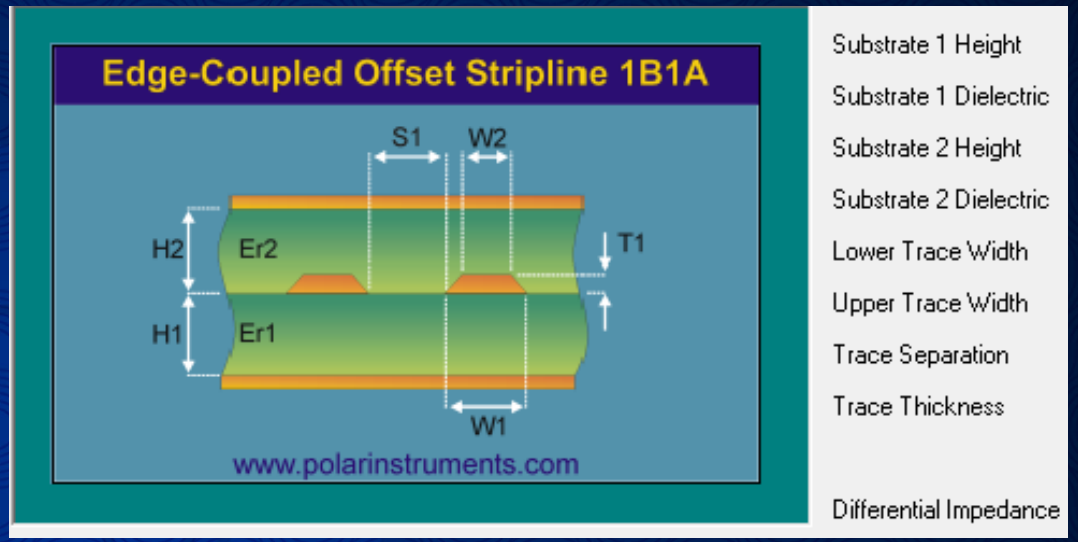
32Gbps

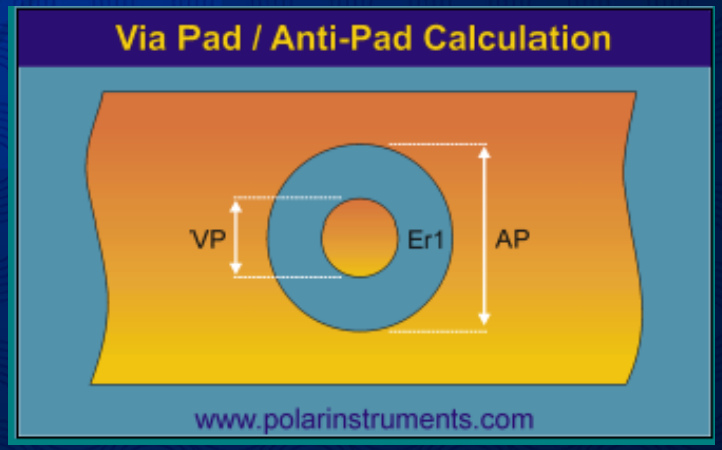


index	permute(Height)	permute(Width)
0.000	0.050	1.563E-11

Accurate factor in Simulation

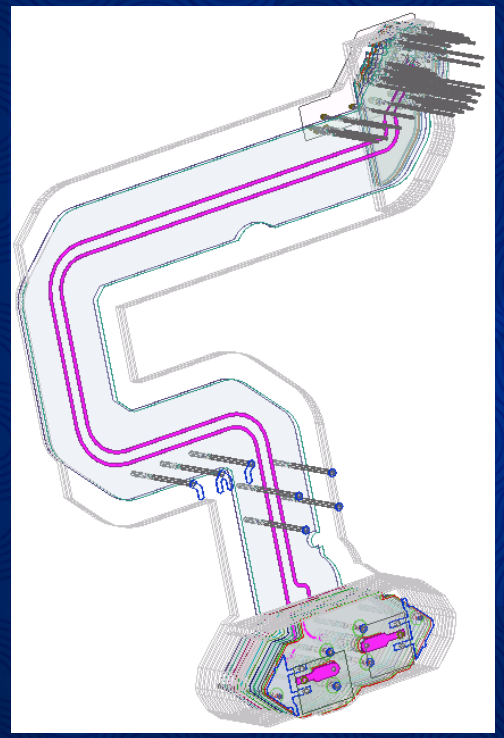
- **Garbage in garbage out**
- **Main factor**
  - Design parameters
    - Trace width
    - Trace separation
    - Trace thickness
    - Substrate Height
    - Substrate Dielectric
    - Surface Roughness
    - Loss Tangent
    - Conductivity
    - Via drill/pad/anti-pad/stub

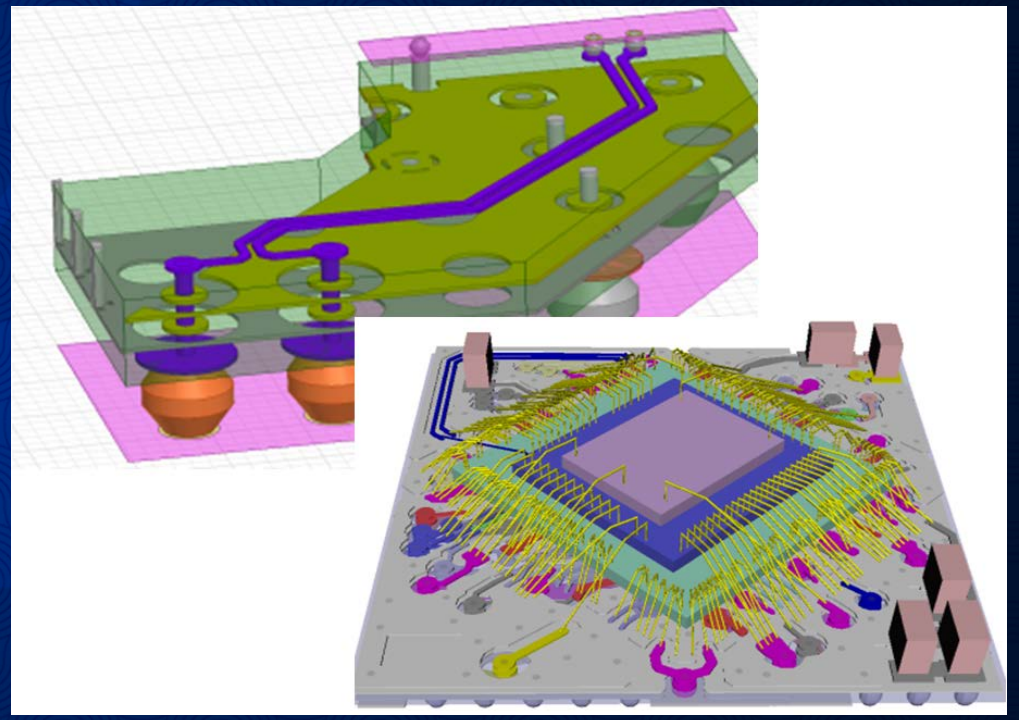




Accurate factor in Simulation

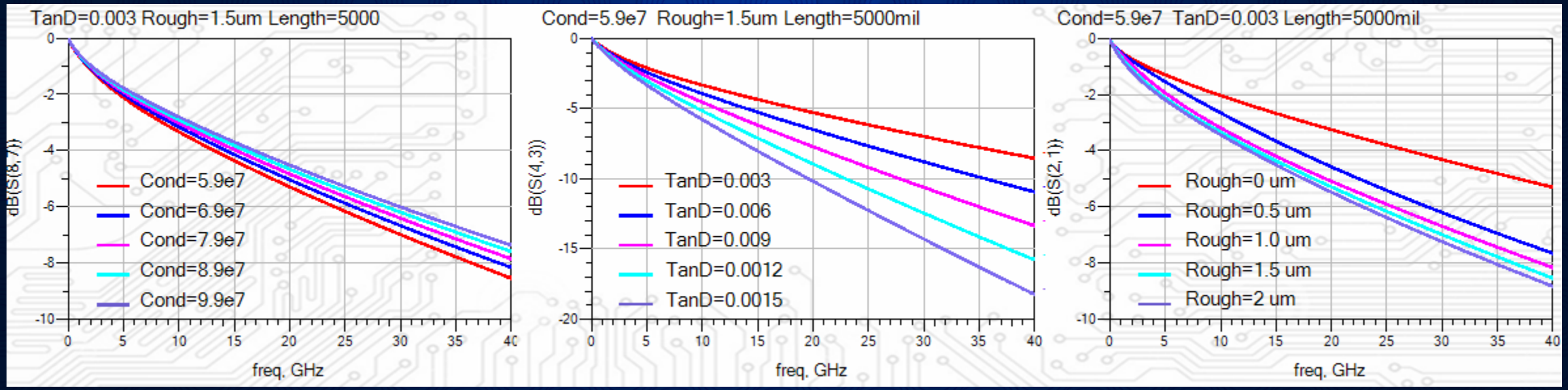
- **Garbage in garbage out**
- **Main factor**
  - Model and settings
    - Problem Analysis
    - Model Decomposition
    - Modeling
    - Parameters control
    - Settings control
    - others





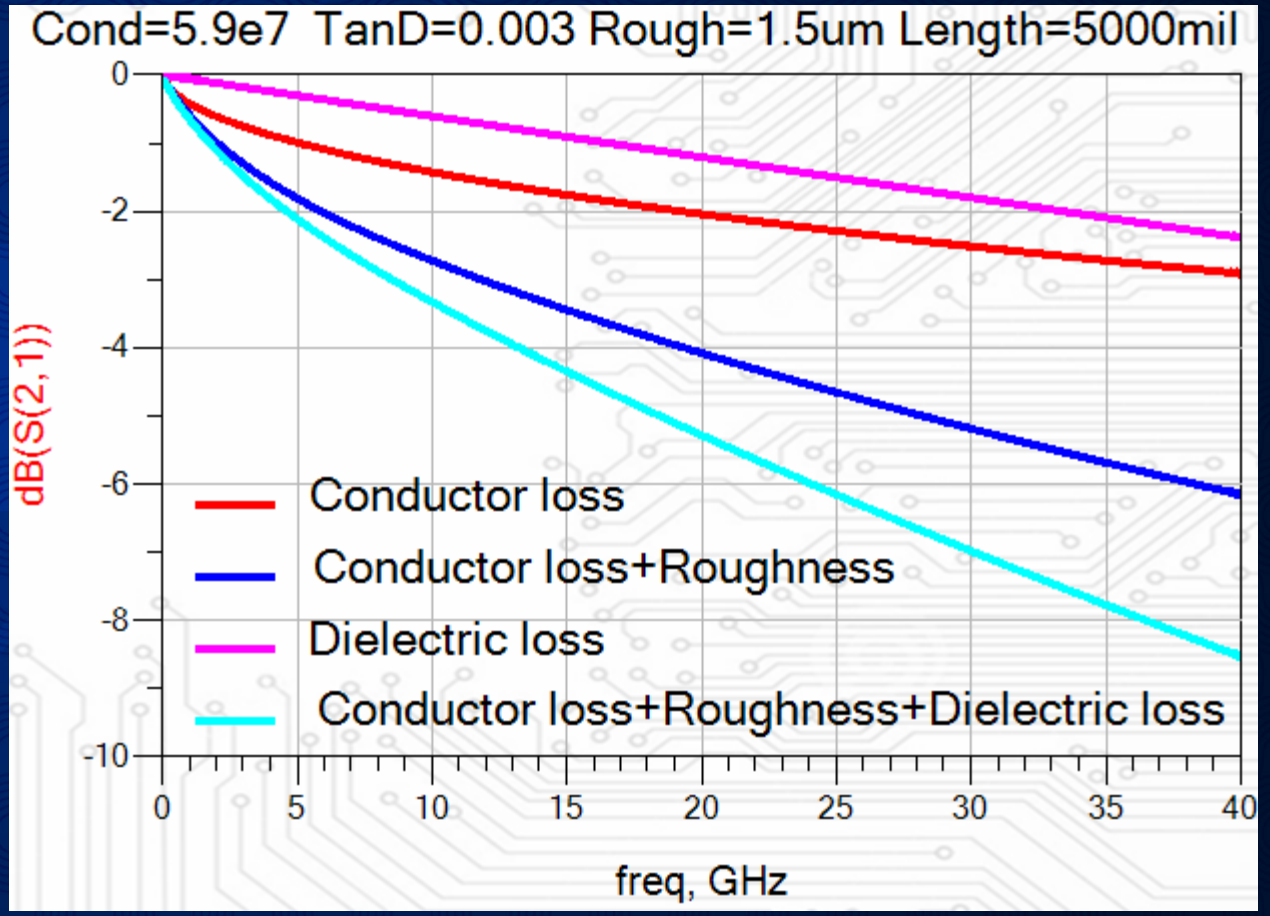
How the factor affect the loss?

- **Analysis One By One**
  - Conductivity
  - Loss tangent
  - Roughness
  - others



How the factor affect the loss?

- **Total Analysis**
  - High speed material with low loss are always used
  - The conductor loss is more than dielectric loss
  - The loss tangent is very low and its loss take no more than 25%
  - The roughness play a key role



What should we do next?

- **Research the accurate factor and consider them in simulation**
  - Material
    - Dk
    - Df
  - Conductor
    - Conductivity
    - Roughness
  - Fabrication
    - Trace width
    - Space
    - Thickness
    - etc.

Panasonic

MEGTRON7

Core Type	Actual Thickness		Cloth Style	ply	Typical Resin Content (%)	Typical Dk						
	mil	mm				1GHz	6GHz	12GHz	18GHz	23GHz	29GHz	34GHz
2	2.0	0.050	1035	1	65	3.37	3.36	3.35	3.35	3.35	3.34	3.34
2.6	2.6	0.065	1080	1	57	3.55	3.54	3.53	3.53	3.53	3.53	3.53
2.6	2.6	0.065	1078	1	57	3.55	3.54	3.53	3.53	3.53	3.53	3.53

Core Type	Actual Thickness		Cloth Style	ply	Typical Resin Content (%)	Typical Df						
	mil	mm				1GHz	6GHz	12GHz	18GHz	23GHz	29GHz	34GHz
2	2.0	0.050	1035	1	65	0.002	0.003	0.003	0.003	0.003	0.003	0.004
2.6	2.6	0.065	1080	1	57	0.002	0.003	0.003	0.003	0.004	0.004	0.004
2.6	2.6	0.065	1078	1	57	0.002	0.003	0.003	0.003	0.004	0.004	0.004

Research board Introduction

- **Design introduction**
  - Different trace impedance---50/90/100ohm
  - Different couple type of intra pair
  - Different trace length
  - Via structure
- **Nets in L3 for example**

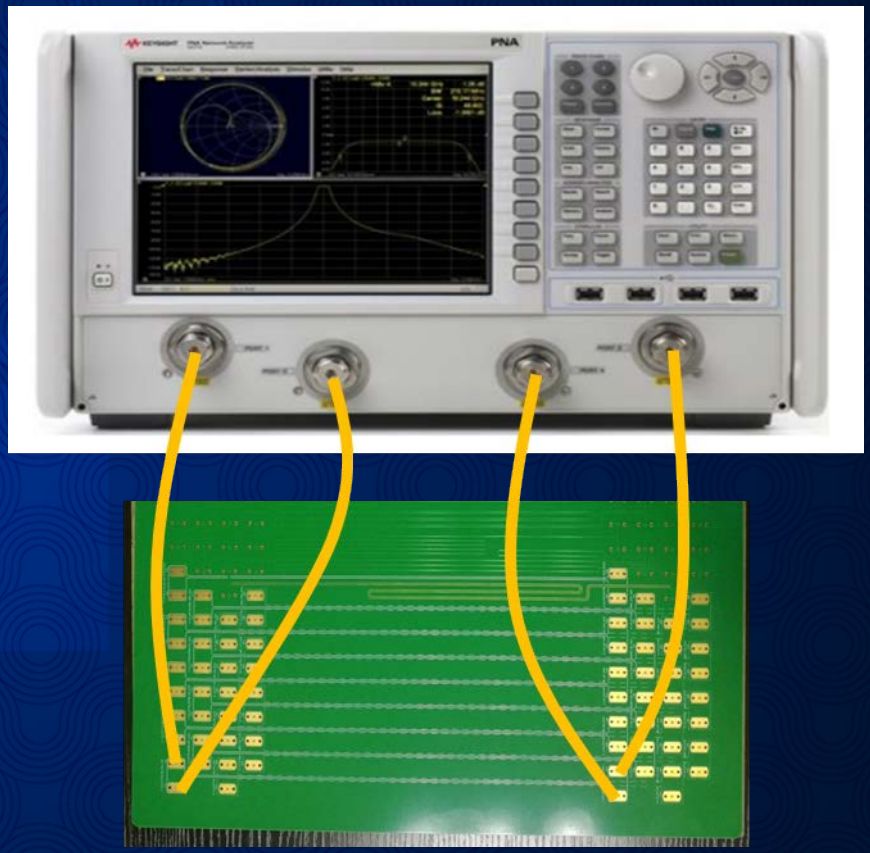
NO.	Net name
1	L3_DIFF100_W5_S8_30IN
2	L3_DIFF100_W5R3_S15_10IN
3	L3_DIFF100_W5R3_S15_20IN
4	L3_DIFF100_W5R3_S15_30IN
5	L3_DIFF90_W5R8_S6_30IN
6	L3_DIFF90_W6R5_S20_10IN

NO.	Net name
7	L3_DIFF90_W6R5_S20_20IN
8	L3_DIFF90_W6R5_S20_30IN
9	L3_SINGLE_W5R3_10IN
10	L3_SINGLE_W5R3_20IN
11	L3_SINGLE_W5R3_30IN

Layer	Info	Thickness
TOP	==========	0.5+Plating
	PP R-5670G 1035*2	4.487(mil)
L2	==========	1 Oz
	Core R-5775G 0.15	5.906(mil)
L3	==========	0.5 Oz
	PP R-5670G 1035*2	4.038(mil)
L4	==========	1 Oz
	Core R-5775G 0.15	5.906(mil)
L5	==========	0.5 Oz
	PP R-5670G 1035*2	4.038(mil)
L6	==========	1 Oz
	Core R-5775G 0.15	5.906(mil)
L7	==========	1 Oz
	PP R-5680NE 1035*2	3.962(mil)
L8	==========	0.5 Oz
	Core R-5785NE 0.146	5.700(mil)
L9	==========	0.5 Oz
	PP R-5680NE 1035*2	4.574(mil)
BOT	==========	0.5+Plating

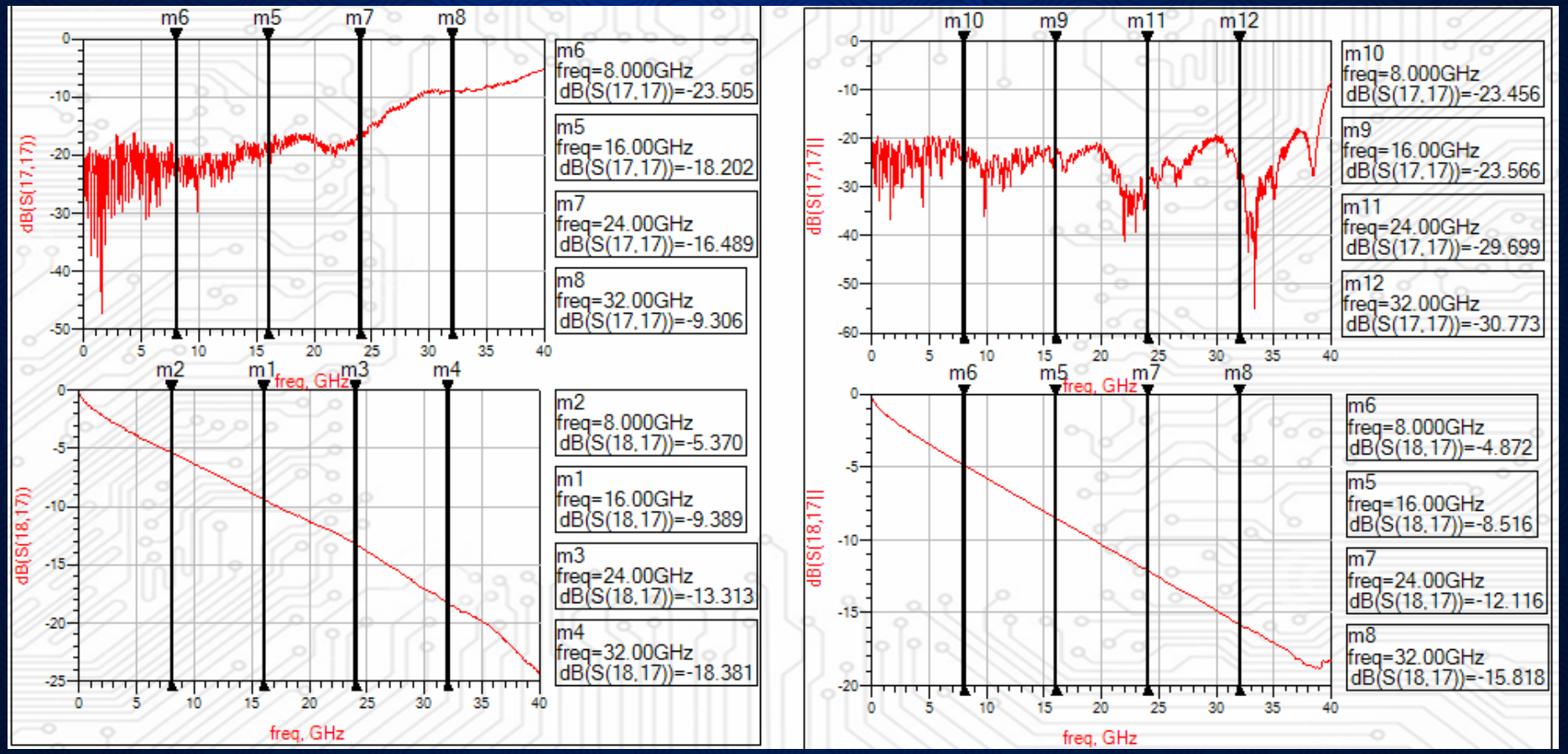
Lab Instrument and settings

- **Instrument: Keysight PNA N5227A**
- **Bandwidth: 10MHz-40GHz**
- **Step: 10MHz**
- **Calibration: E-CAL**



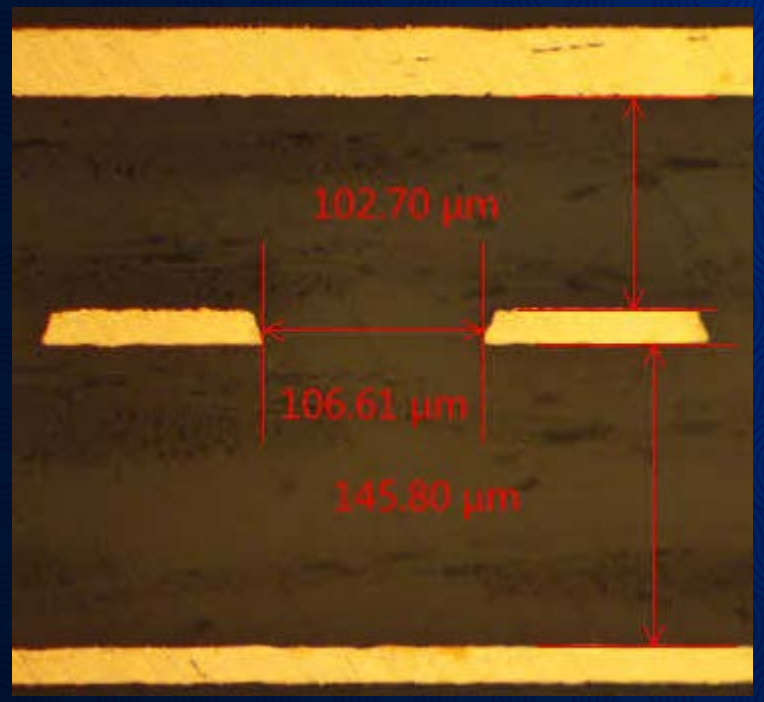
Data for example

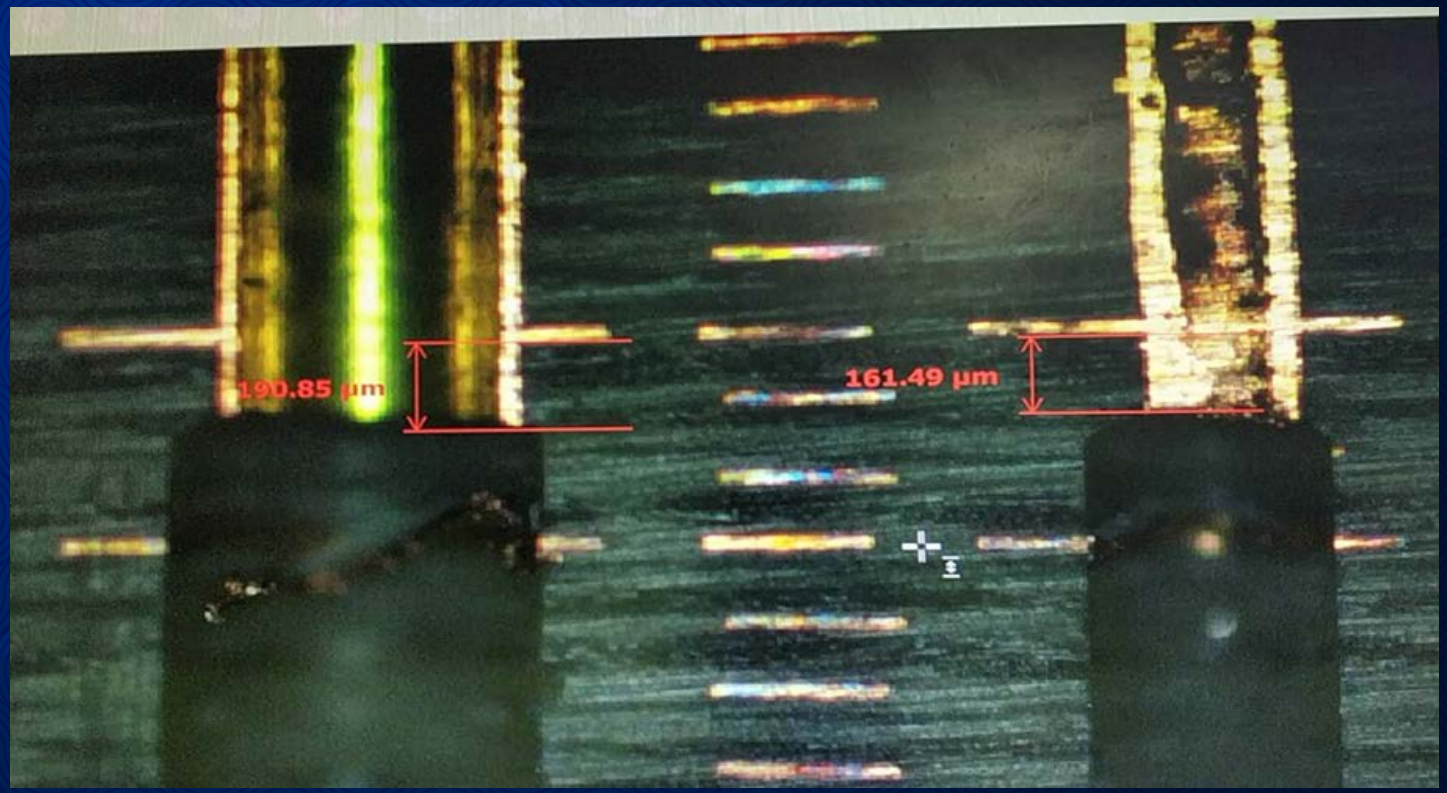
- Data without de-embedded
- Data with de-embedded



Data for example

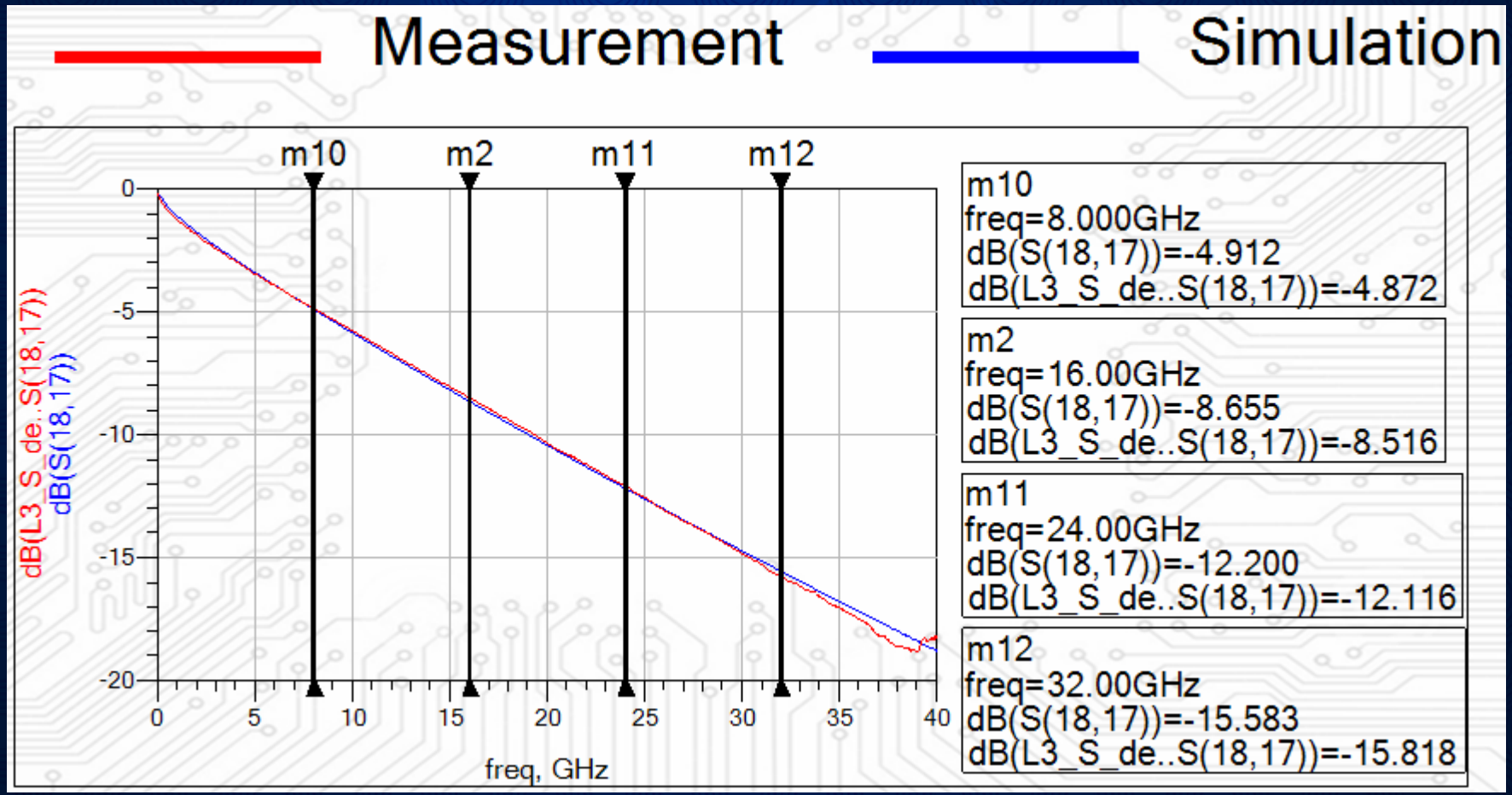
- **Slice of PCB**
- **Analysis of trace and via size**





Parameter adjustment and Loss fitting

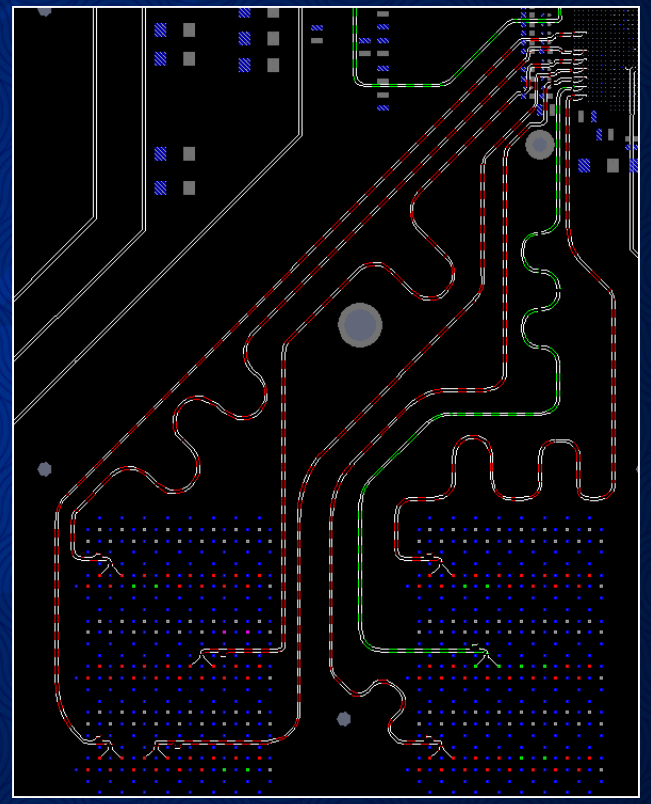
- **Loss fitting**
- **Parameters adjust and export**



Case Study

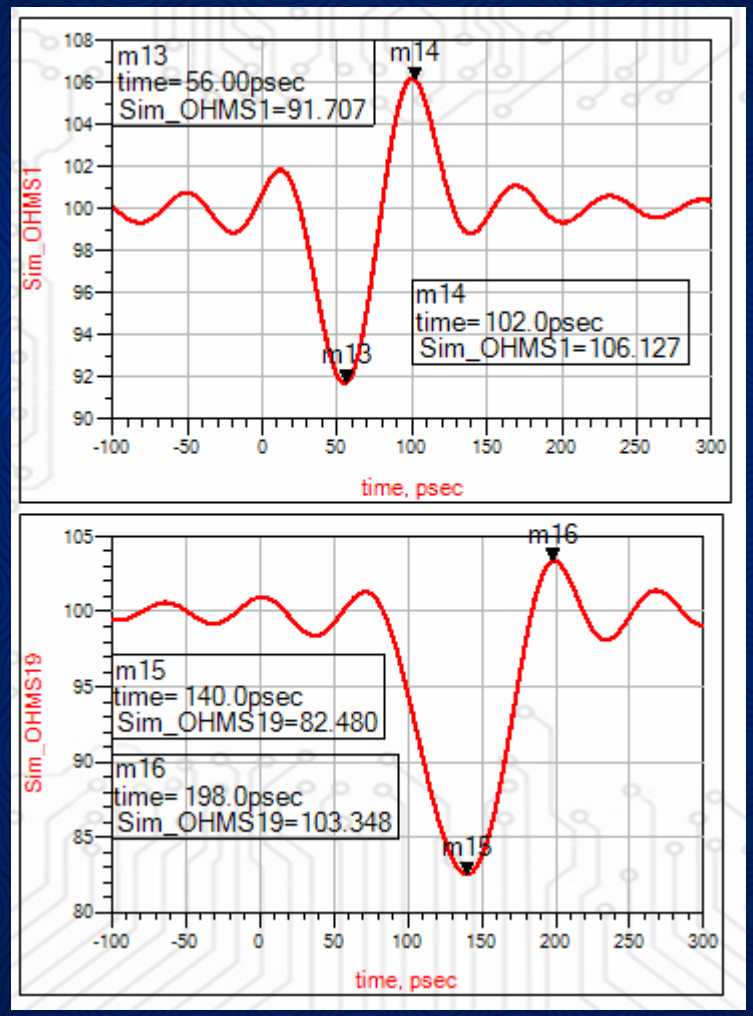
- One project with signals up to 16Gbps
- 6 lanes are included for analysis
- Bandwidth: 10MHz-16GHz
- Step: 10MHz

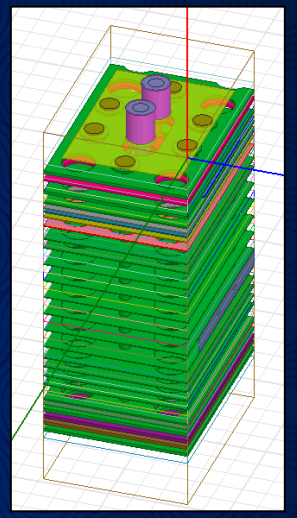
NO.	DUT	POGO	Layer
1	TX3	TX3	18
2	TX0	TX0	22
3	TX0	TX0	22
4	RX1	RX1	24
5	RX0	RX0	24
6	RX2	RX2	28

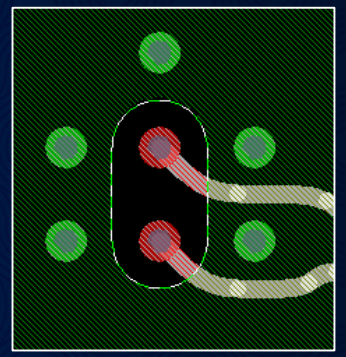


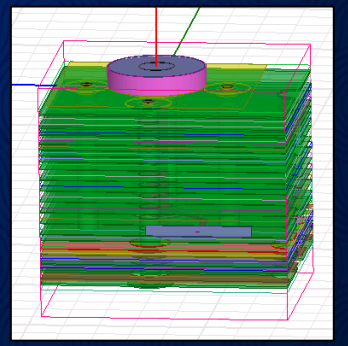
Case Study

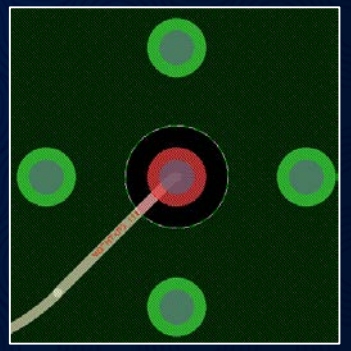
- **Optimization the via**
- **DUT Via**
  - Drill bit size 10mil
  - Anti-pad size 50mil
- **Pogo via**
  - Drill bit size 30 mil
  - Anti-pad size 100mil









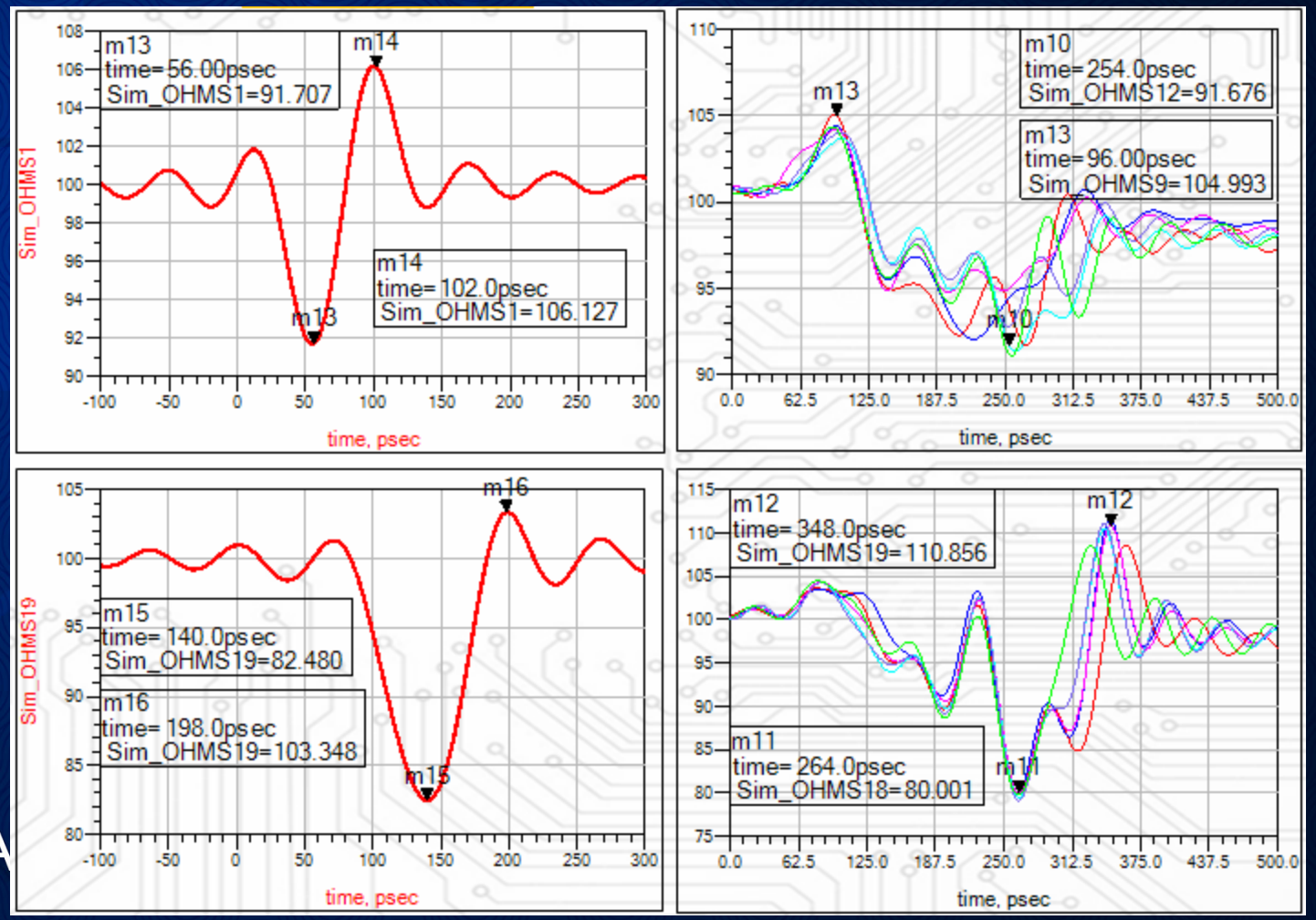


Case Study

- **Via Impedance correlation**
- **DUT Via**
  - Simulation 91.7-106.1ohm
  - Test 91.7-105ohm
- **Pogo via**
  - Simulation 82.5-103.3ohm
  - Test 80-110.8ohm

Simulation

Measurement



Case Study

- **Lane loss correlation**
- **Gap ~0.18db@8GHz**
- **Gap ~0.2db@16GHz**

Net	Simulation loss @8GHz/db	Test loss @8GHz/db	Error @8GHz/db	Simulation loss @16GHz/db	Test loss @16GHz/db	Error @16GHz/db
TX3	4.156	4.034	0.122	8.248	8.458	-0.21
TX0	4.267	4.156	0.111	8.923	9.073	-0.15
TX0	4.238	4.052	0.186	9.742	9.942	-0.2
RX1	4.596	4.546	0.05	9.859	9.969	-0.11
RX0	4.534	4.443	0.091	9.623	9.673	-0.05
RX2	4.773	4.804	-0.031	9.714	9.894	-0.18

Summary & Future work

- **Based on the research, the loss gap between simulation and test is no more than 0.18db@8GHz, 0.2db@16GHz**
- **More challenges in higher frequency loss control**
- **We will continue to decrease these gaps and try to get a very good correlation at high frequency**

Thanks for your Attention!

High Performance CIS Wafer Probing Using 2D MEMS Technology

Korea Instrument **Yunhwi PARK**, Kyoungsub KIM
Youngjin KIM, Sungjun KANG

Samsung Electronics Kyushik MIN
Changhoon HYUN

Taiwan, October 18-19, 2018

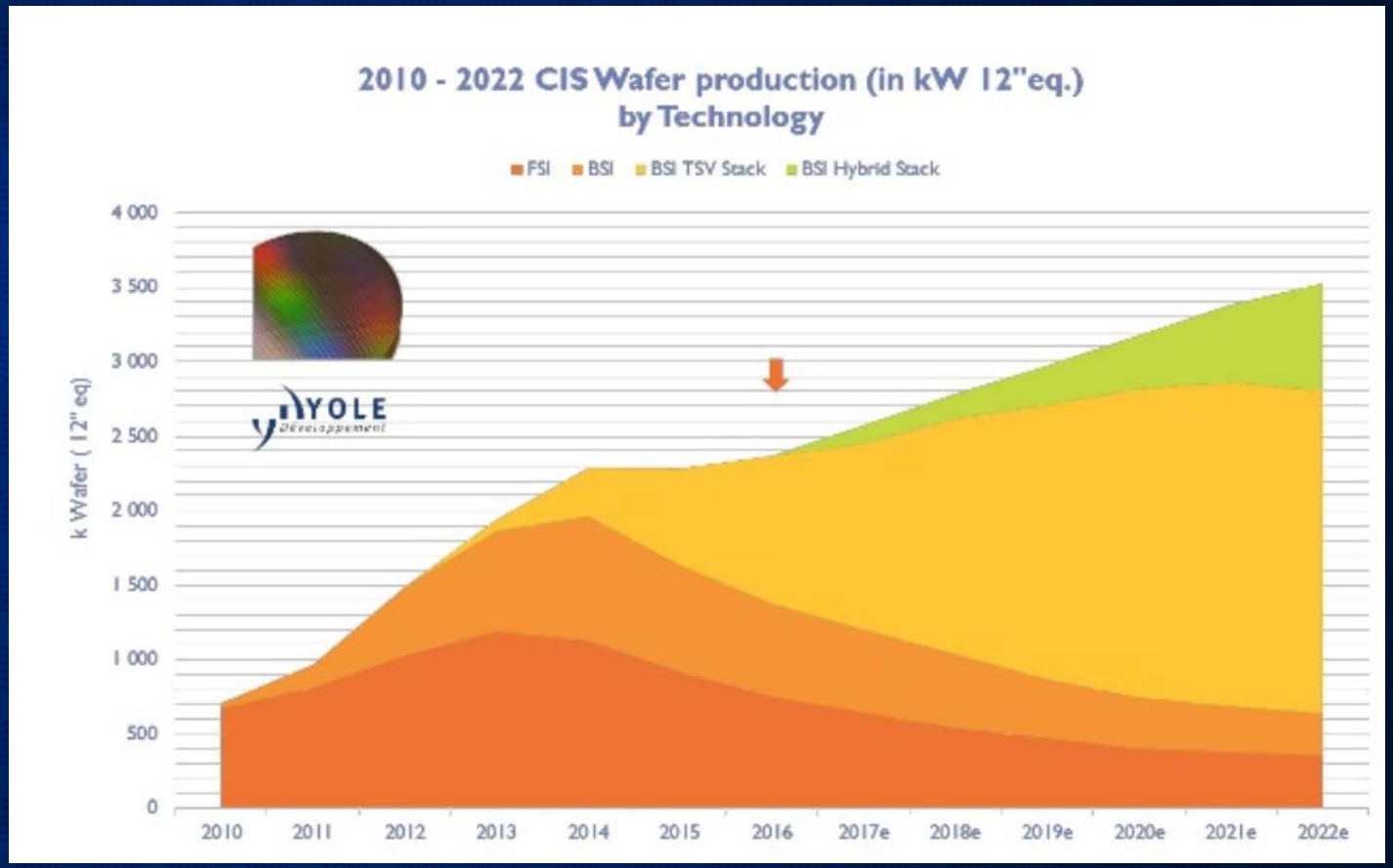
Contents

- Market
- Probing for CIS Test
- Probe Card Solutions
- 2D MEMS Probe Card for CIS Test
  - structure, probe, performance, reliability
- Future Work
- Summary

Market

Market Growth

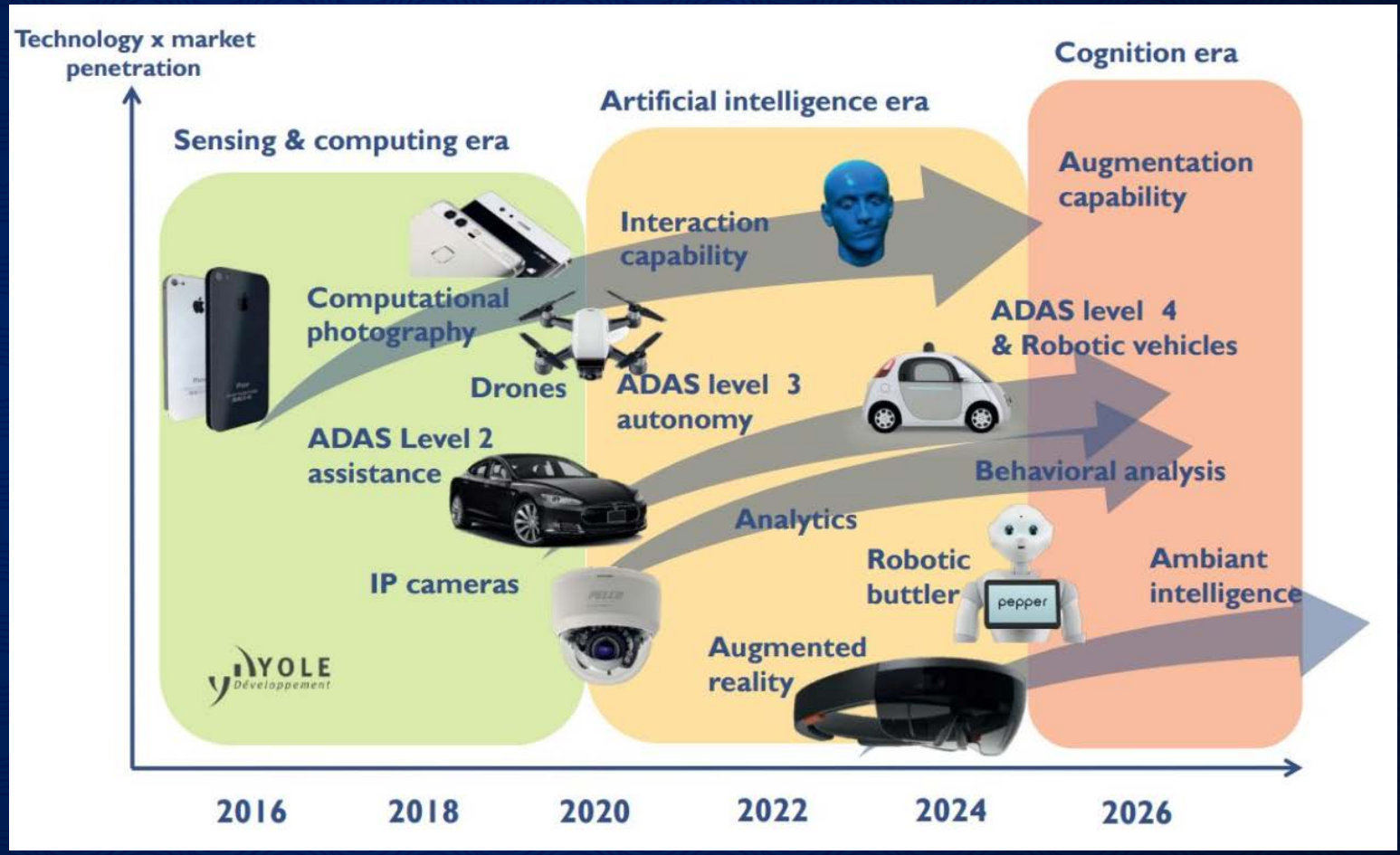
CMOS image sensor market is expected to grow over 10% per year(~2022)



Yole, 2017

Market Drivers

3D Sensing, Automotive, Security, Robotics, AR and AI drives CIS market growth!

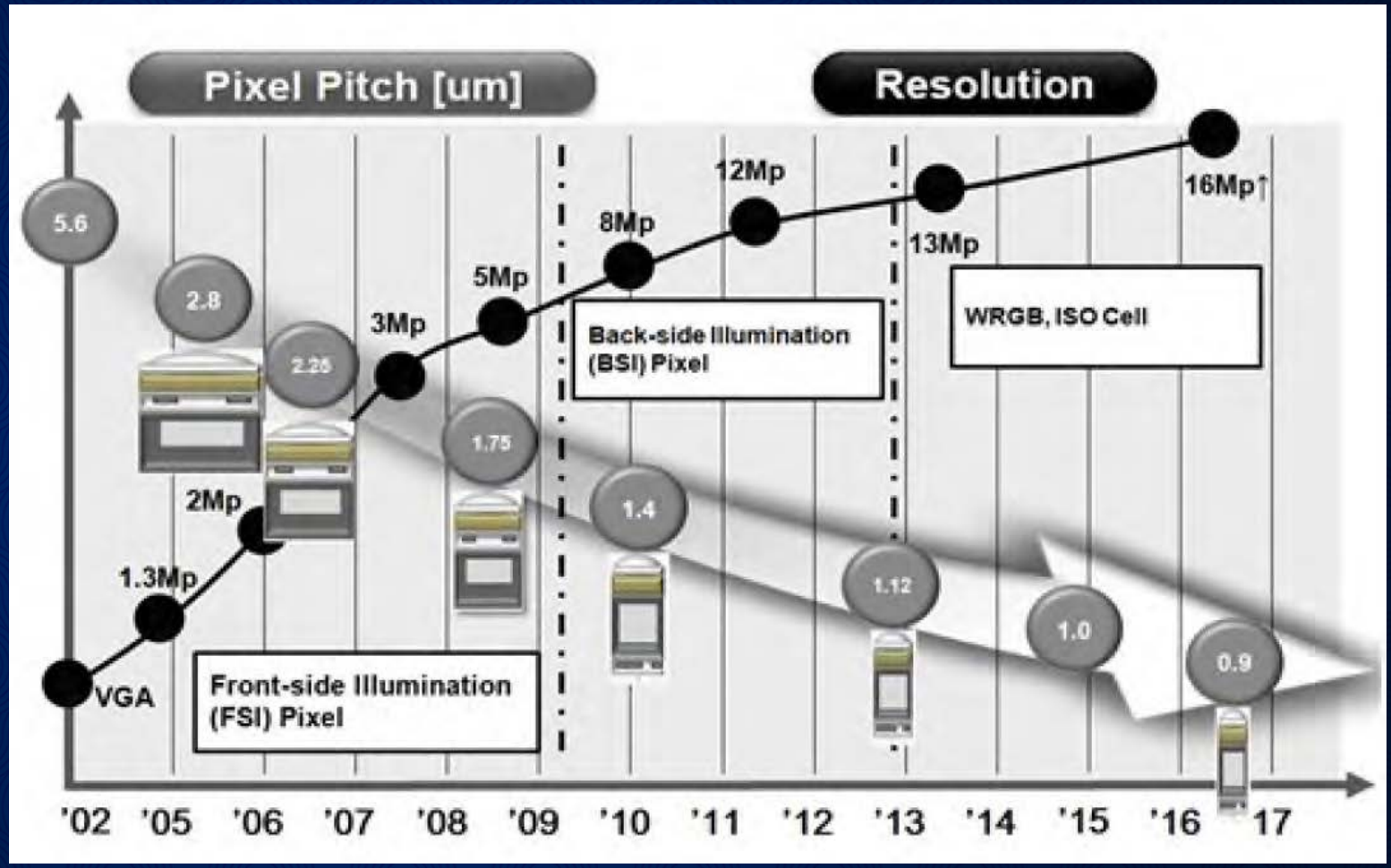


Yole, 2017

Pixel Pitch and Resolution

0.9um pixel size

> 20M pixel resolution



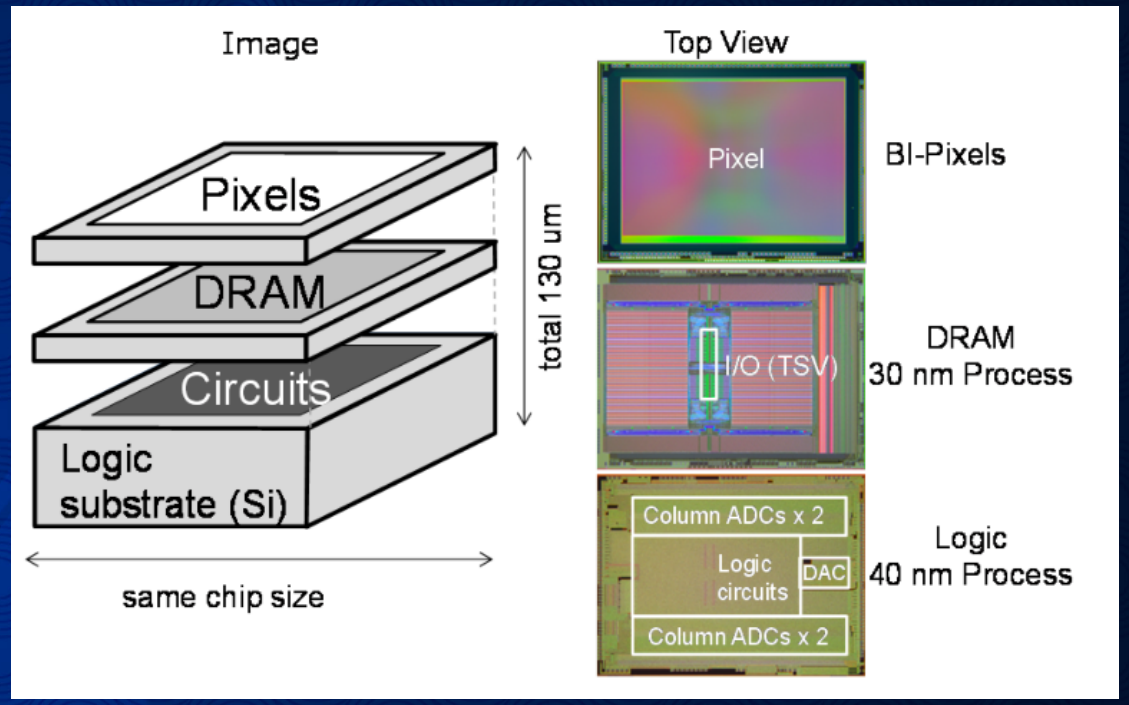
CIS Technology Trend

FSI

BSI

ISO CELL

Samsung



3-Die Stack

IEDM 2017, Sony

Sensitivity Improvement

Speed Improvement

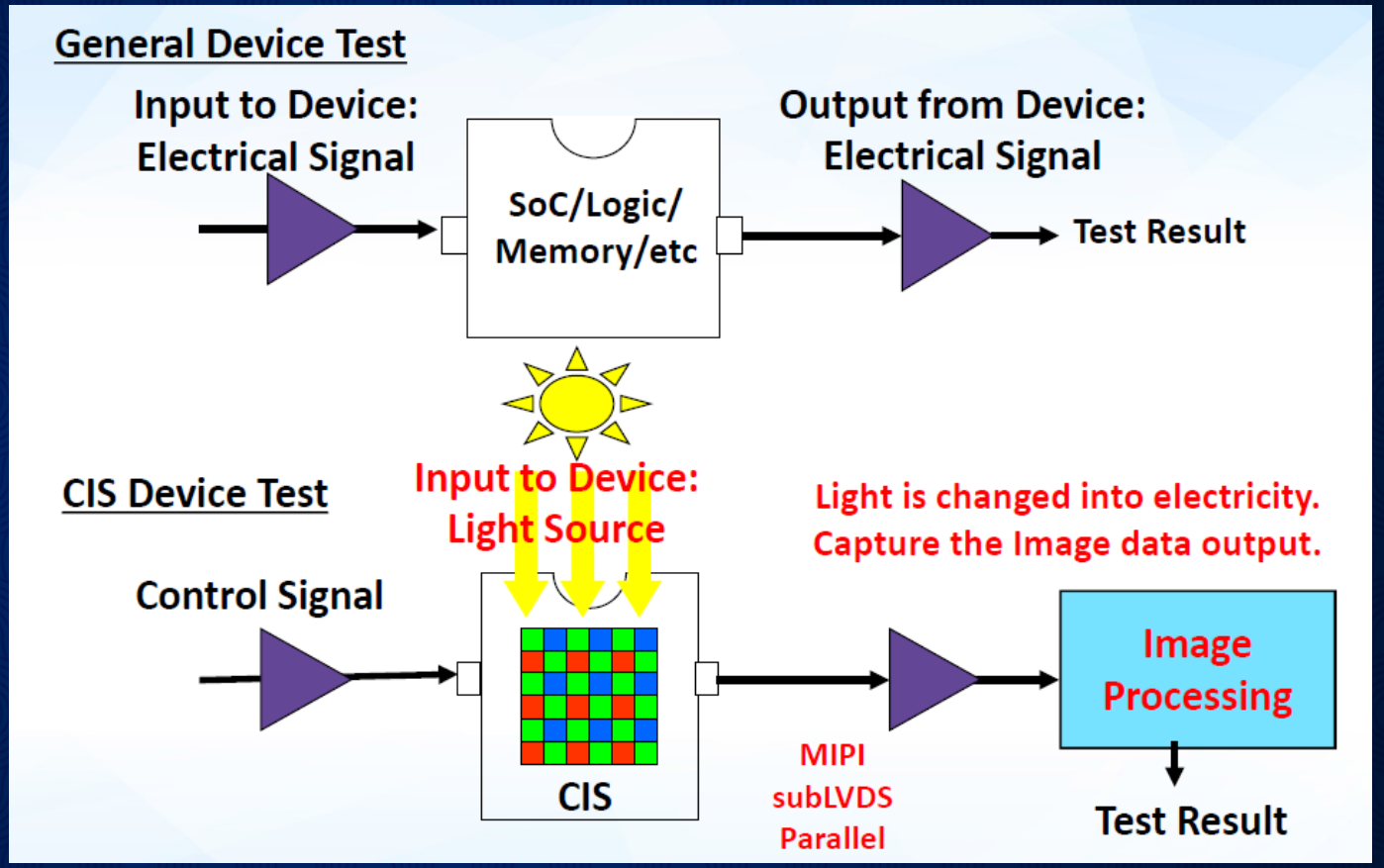
Probing for CIS Test

CIS Wafer Test

Light Sensor!

Input : Light

Output : Electric



Advantest, 2017, Koreatest Conf.

CIS Wafer Probing Issue

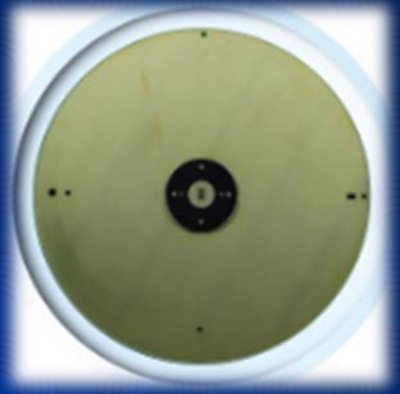
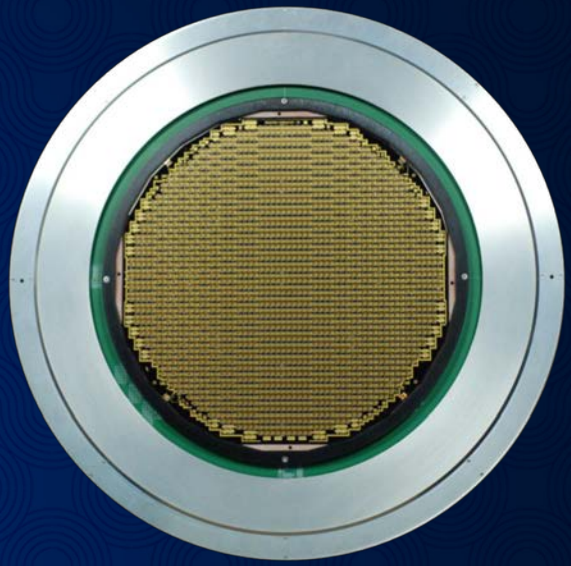
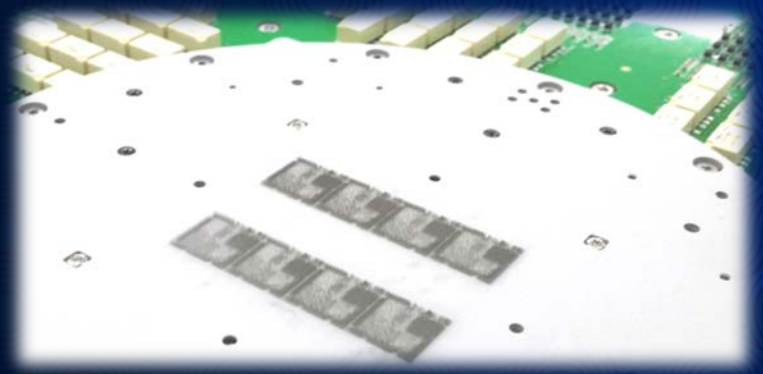
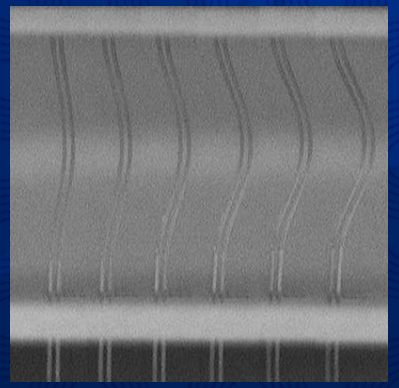
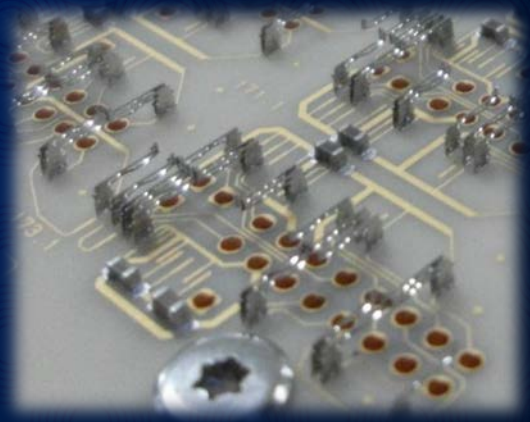
- Vision Test → Low Particle from probing
- High Frequency → Low Loss/Noise GHz SI/PI
- Multi-Touch Down → Low Cres, Long Tip Life Time

	Memory	CIS
Wafer	12"	12"
Touch Down	1~2	100~200
Vision	X	O
Frequency	30~100MHz	> 1.2 Gbps
Min. Die Skip	No Skip	1Die Skip

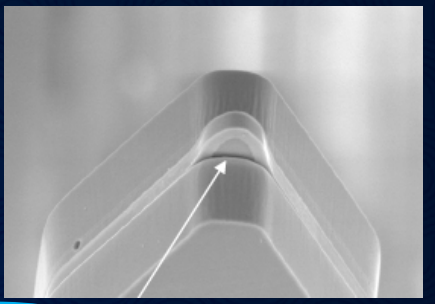
Probe Card Solutions

Various Type Probe Card

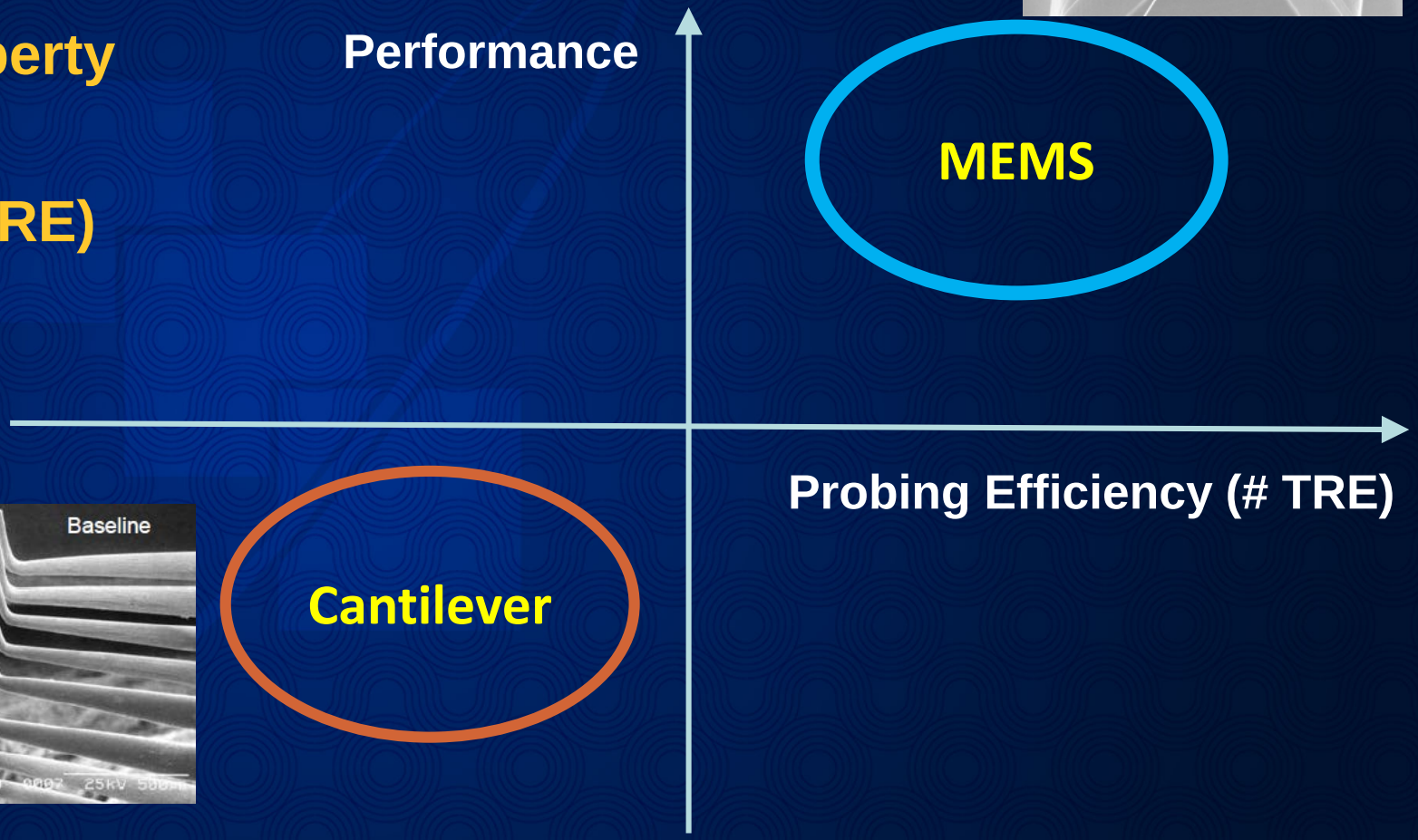


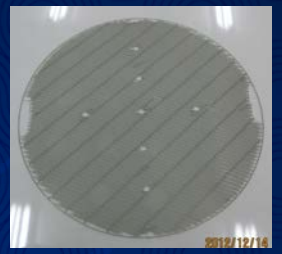
Why MEMS?



- Good & Uniform Probe Property
- Controlled Scrub Mark
- High count probing (multi-TRE)
- Good Elec. Characteristics



3D & 2D MEMS



- 2 types of MEMS Probe
- 3D MEMS

  - etching/plating 3D shape tip in sacrificial substrate(i.e. Si)

    → beam formation on that substrate

    → bonding on pre-fabricated bump on ceramic substrate(MLC)

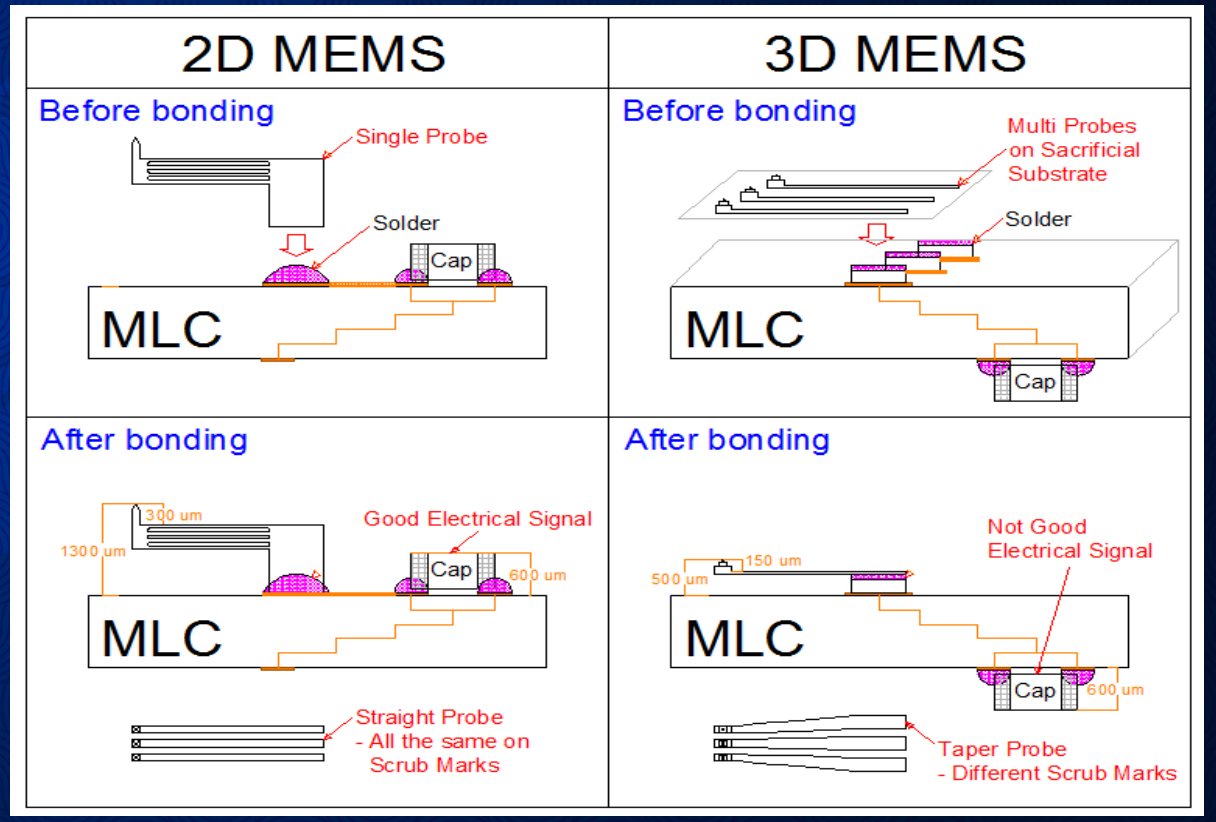
    → etch out sacrificial substrate

- 2D MEMS

  - additive 2D process whole probe on substrate

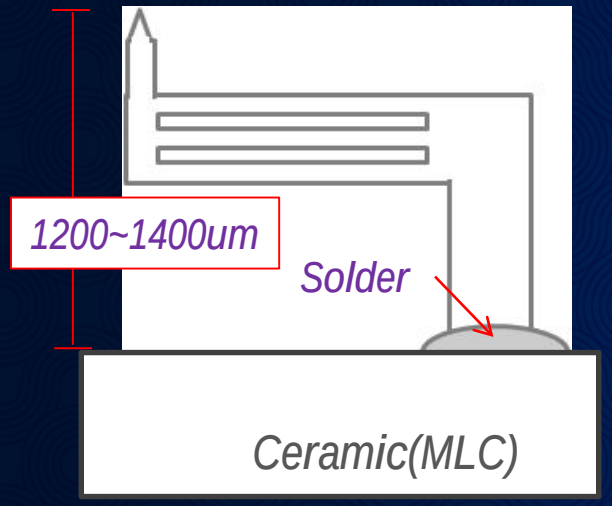
    → detach individual tip

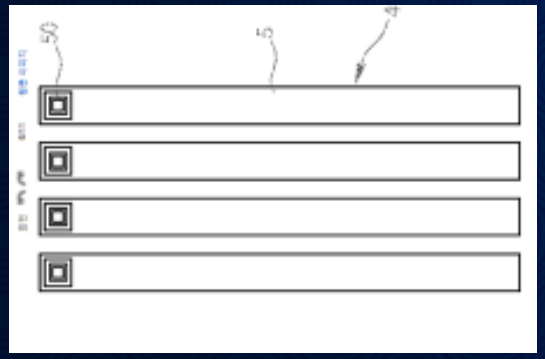
    → laser soldering on ceramic substrate

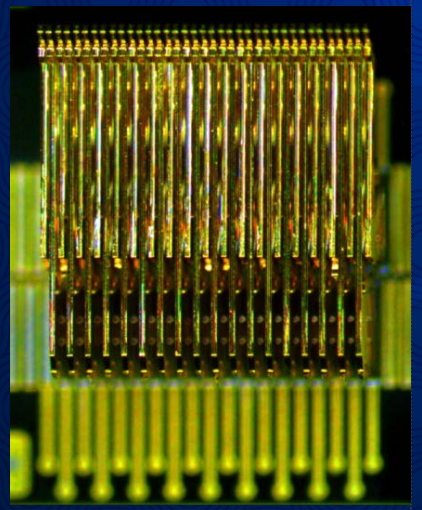


3D & 2D MEMS

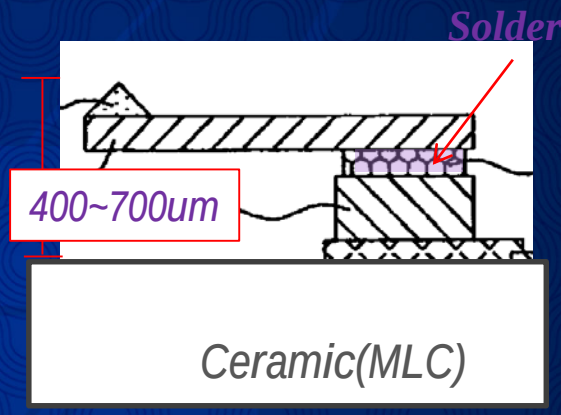
2D MEMS

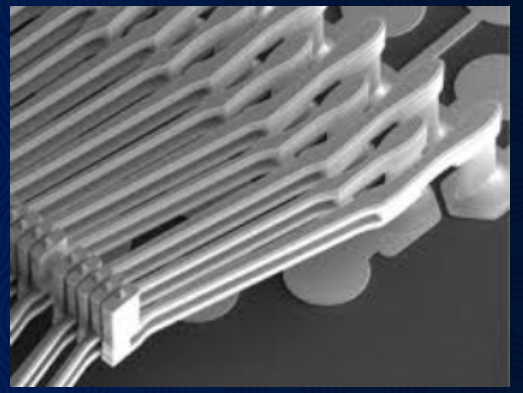


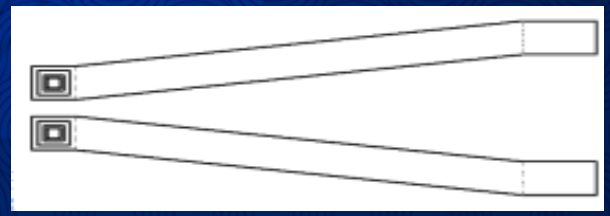


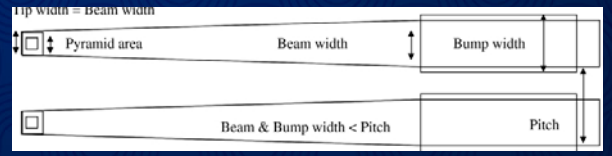


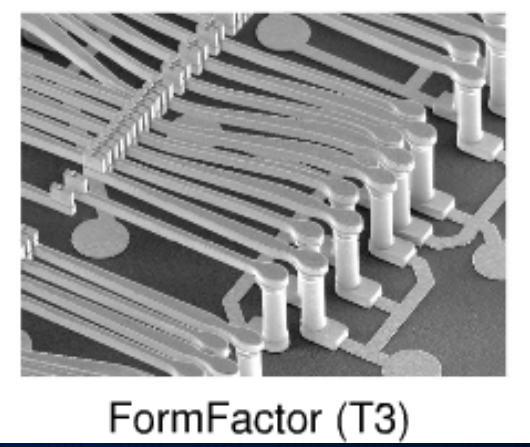
3D MEMS





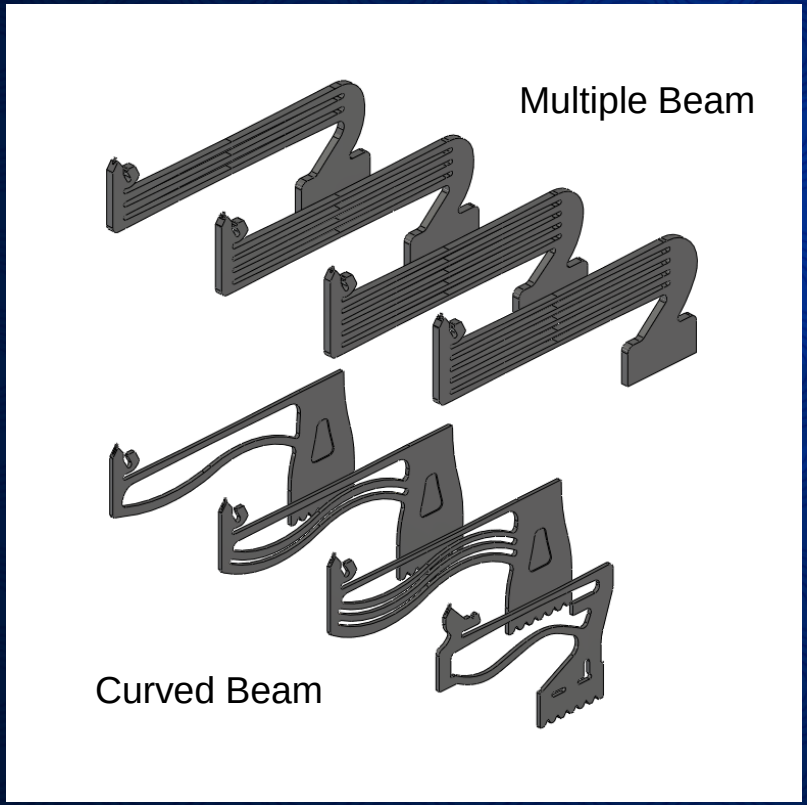






2D Probe Design Flexibility

- **Wide Beam Design Flexibility → Target Specific Probe Property is possible**



CCC, Force,
Scrub Movement

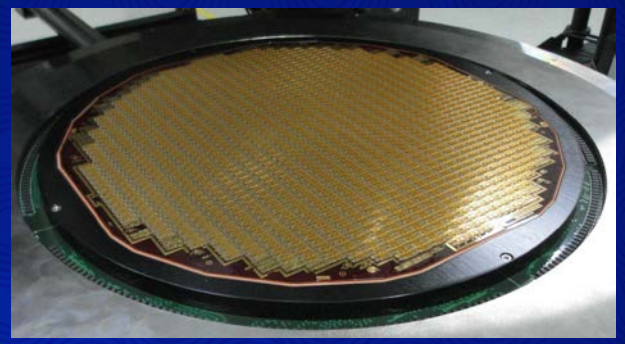
3D & 2D MEMS

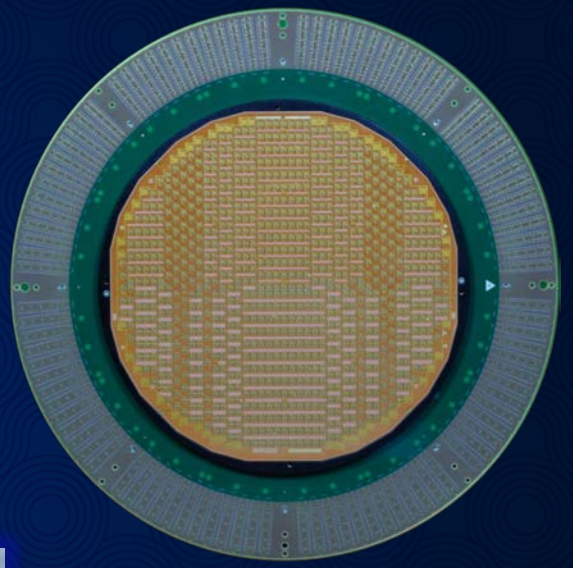
2D has several proper characteristics for CIS testing (high speed, particle, multiple TD, etc)

	3D	2D	Remark	Impact
Tip Height	Low	**High**	Capacitor Near Probe	Lower Impedance
Tip Shape	Pyramid	**Plate**	Constant Tip Area with Wearing	Low Al Particle
Multiple Beam	1~2	**> 4**	Small Scrub Movement Control	
Curved Beam	X	**O**		
Probe Shape	Different with Position	**All the Same**	Same Geometry Probes	Uniform Property

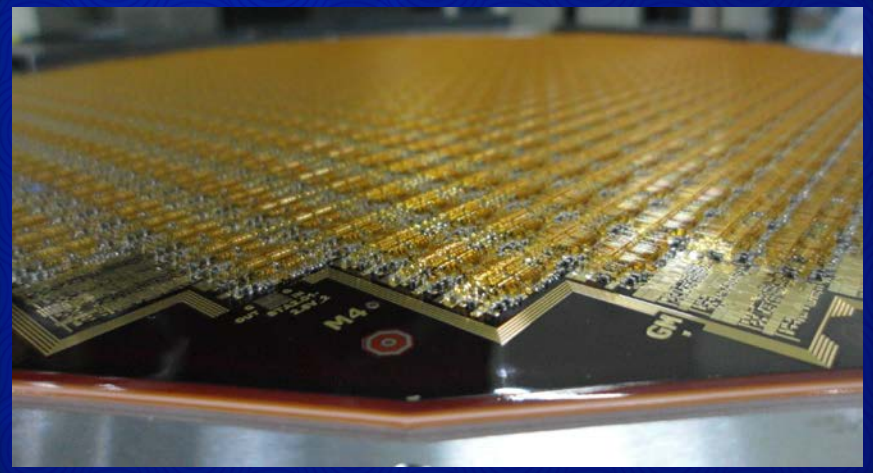
Application

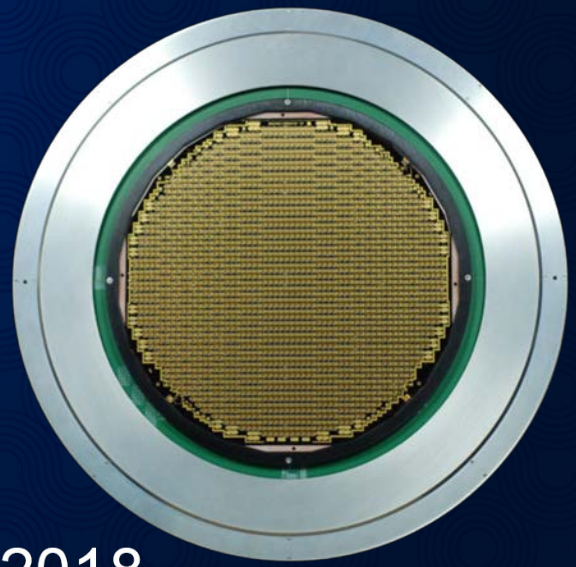
- **2D MEMS is being used for 12" one touch down testing of memory wafer**





- **# pin : 10K~150K**
- **pitch : down to 50um**
- **CCC : up to 1A**

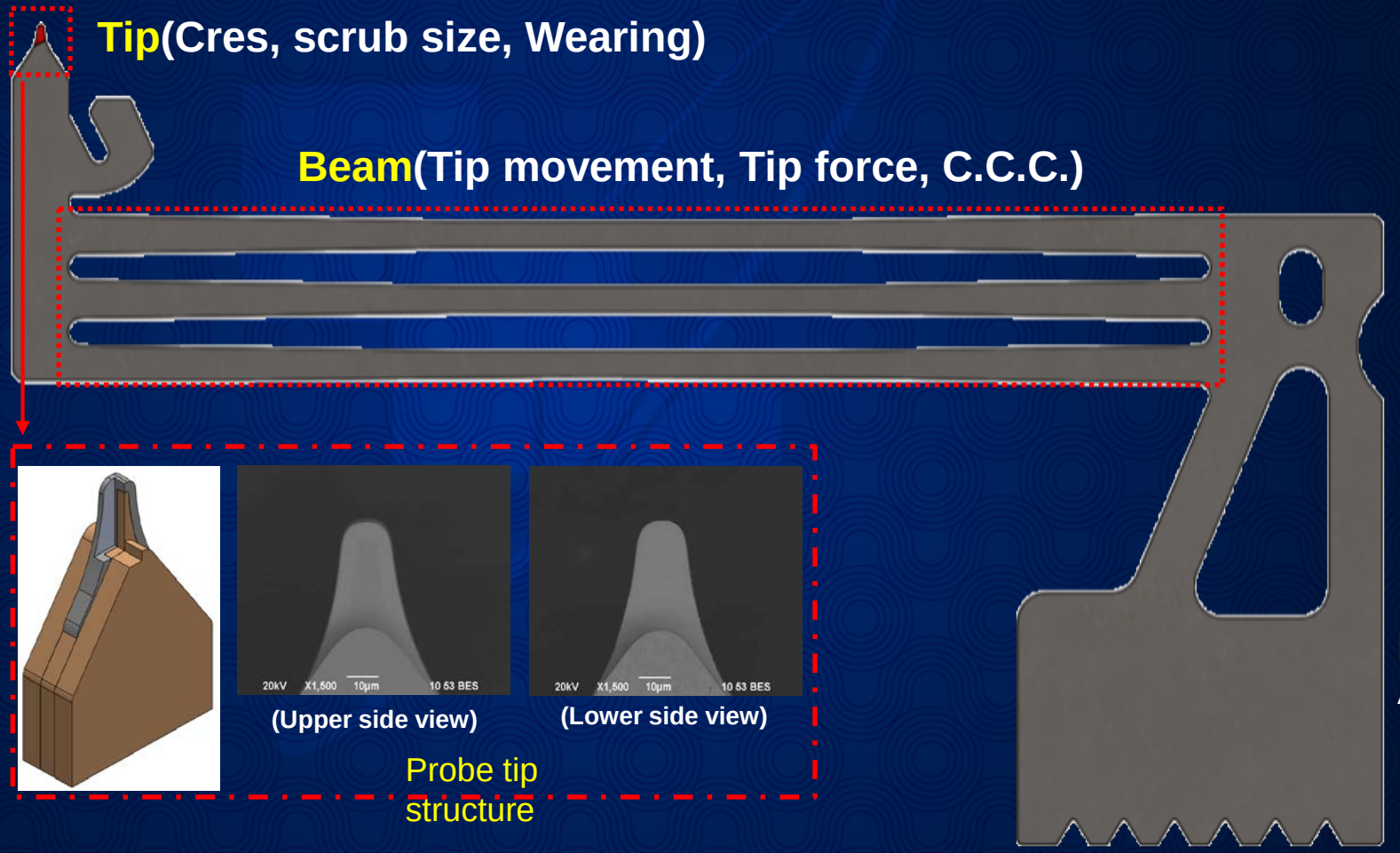




2D MEMS Probe Card for CIS

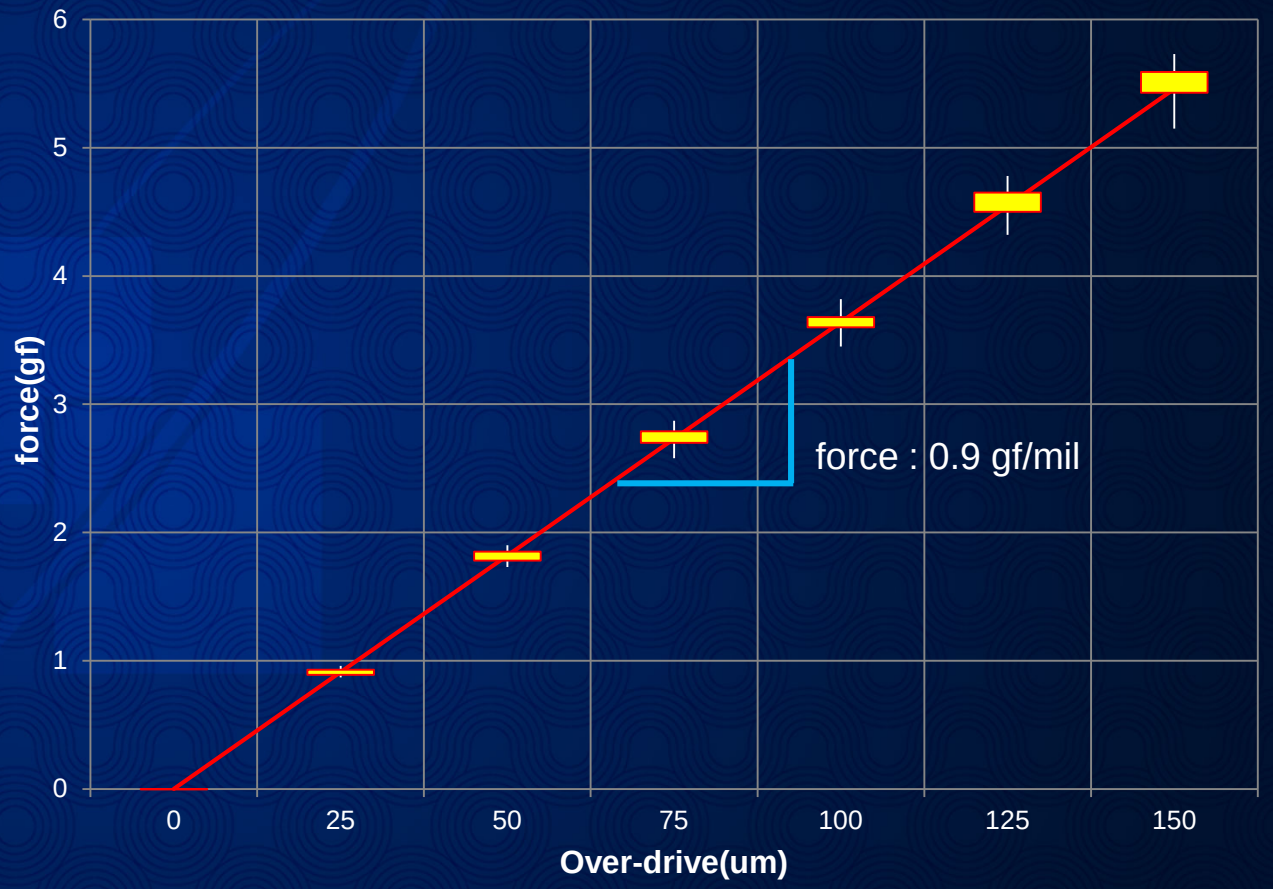
2D MEMS Probe

Ni-Alloy MEMS
Thickness : 35um
Tip Height : 1.2mm
Tip Length : 1.5 / 2.2mm



Probe Property : (1) Force

Probe force : 0.9gf/mil

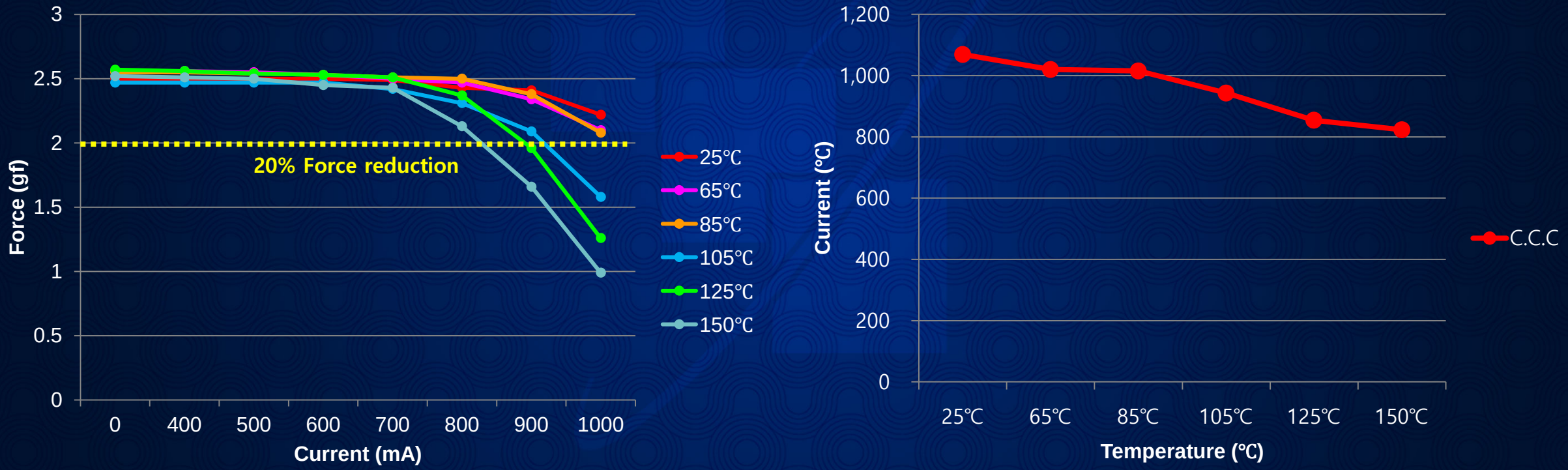


Test Condition

Temp.	Room temp.(23 ℃)
Prober	Tip test machine
Over Drive	0 um ~ 150 um (Step 25 um)
Contact time	10 sec (each step)
Fixed	Vacuum
T/D count	3 count(each test pin)

Probe Property : (2) C.C.C

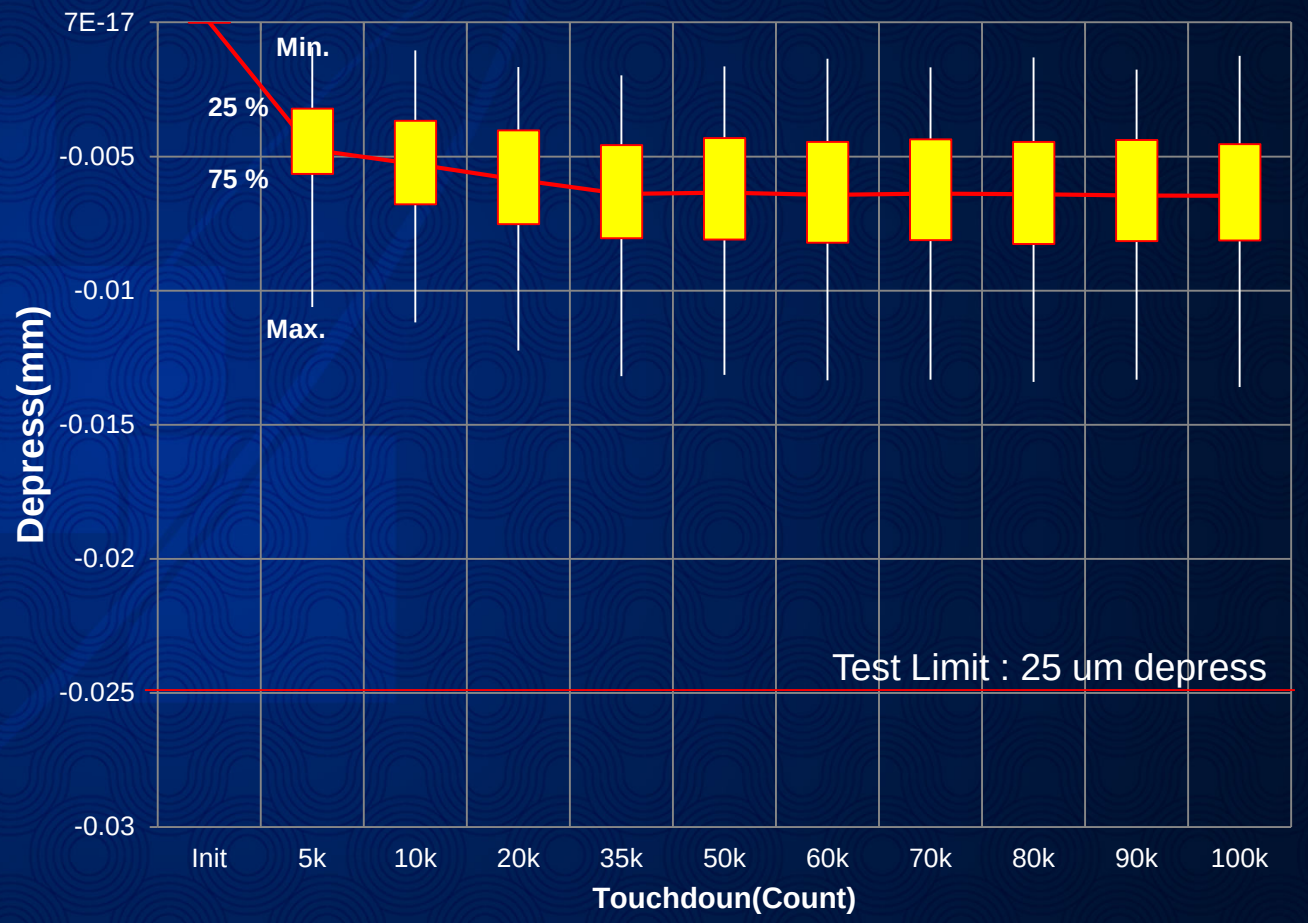
CCC is over 1A at room temperature, and decreases with temperature



· Test Overdrive: 100um
· Test Time: 2min/Current

Probe Property : (3) Depress

Probe depress increase with touch down, but saturated 5~10um over 100K TD



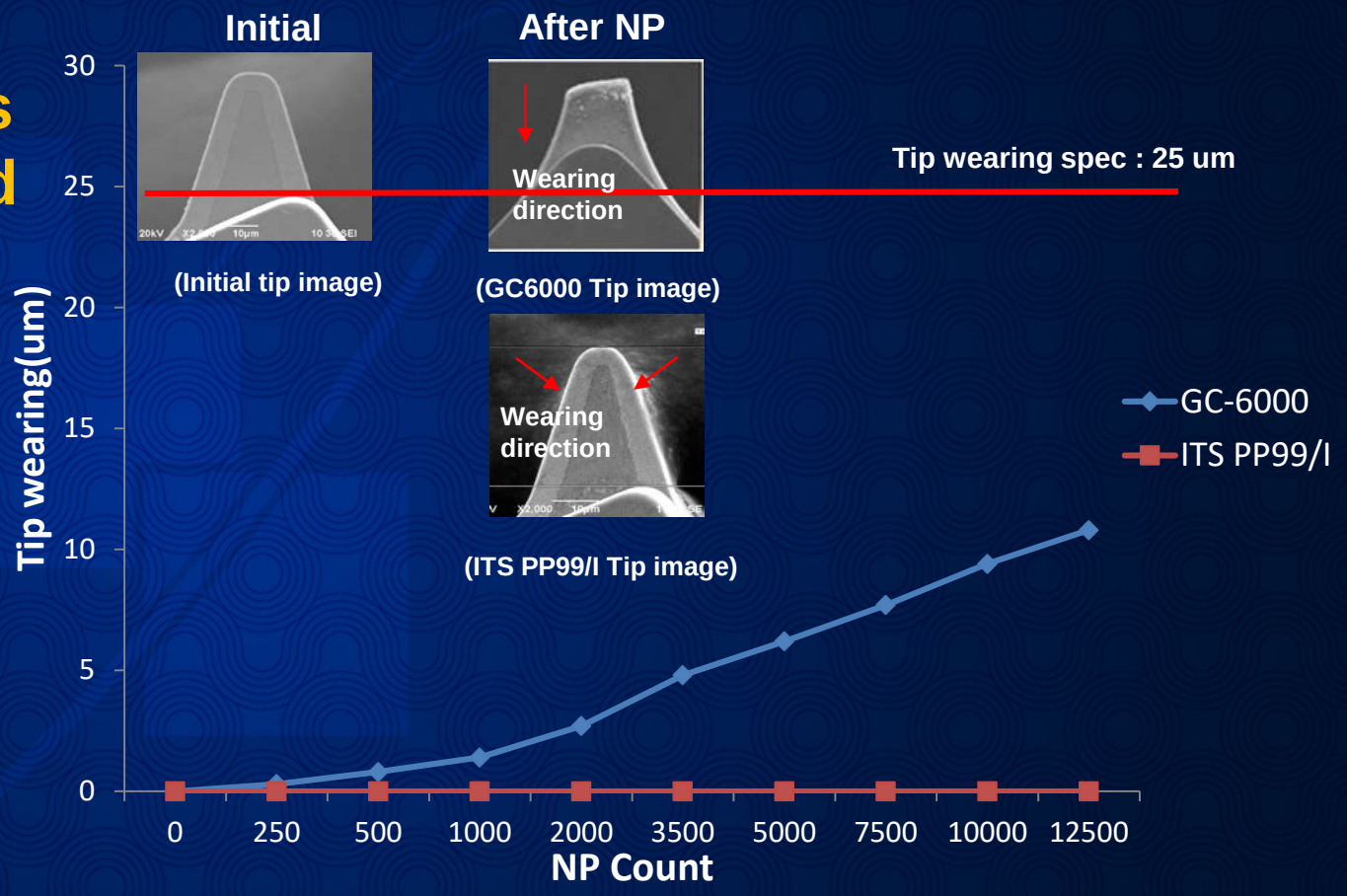
Test Condition

Temp.	Hot (90 ℃), Cold (-25 ℃)
Prober	SECRON IP-300H
Over Drive	100 um
Contact time	Total 12 sec (Contact 10 sec, Separate 2 sec)
Fixed	Bolting (1 Pound/ 8 Point)
T/D count	Hot 50 k, Cold 50 k

Probe Property : (4) Tip Wear

Tip wearing by needle polishing is under 10um for hard NP sheet, and under 2um for soft NP sheet

→ Over 1M touchdown is possible



Test Condition

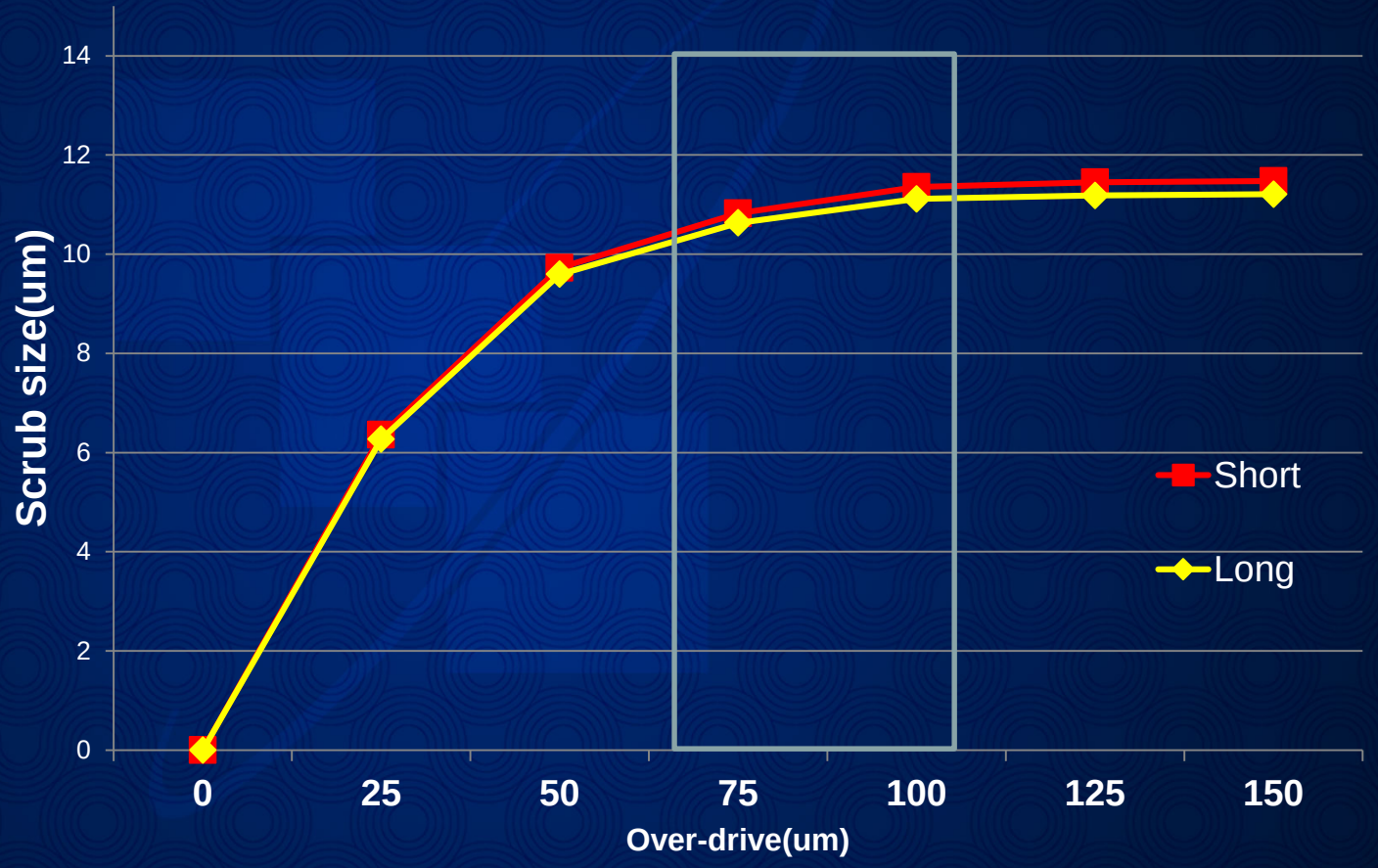
Temp.	85 ℃
NP sheet	GC-6000, ITS PP99/I
Over Drive	75 um

* NP : Needle Polishing

Probe Property : (5) Scrub movement

Scrub movement increase with overdrive up to 11um and saturates

← Beam structure design



Case Study

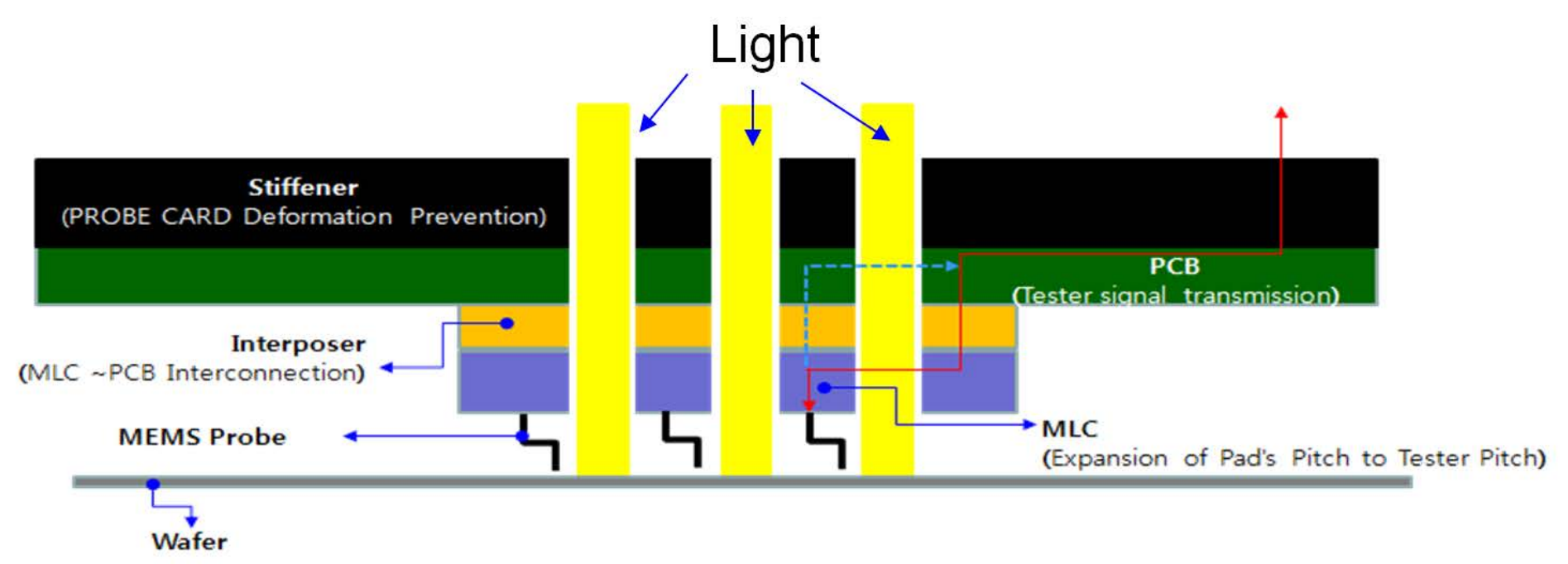
- **Mobile Image Sensor**

Device			
Model	ISOCELL Fast	Resolution	4032x3024 (12M)
Pixel Size	1.4um	Optical Format	1/2.6"
Pixel Type	ISOCELL	Frame Rate	30fps
Interface	MIPI 4 Lane RAW	Chroma	RGB
Auto Focus	Dual-PD	Product Status	Mass Production
Application	Mobile phone, Tablet		

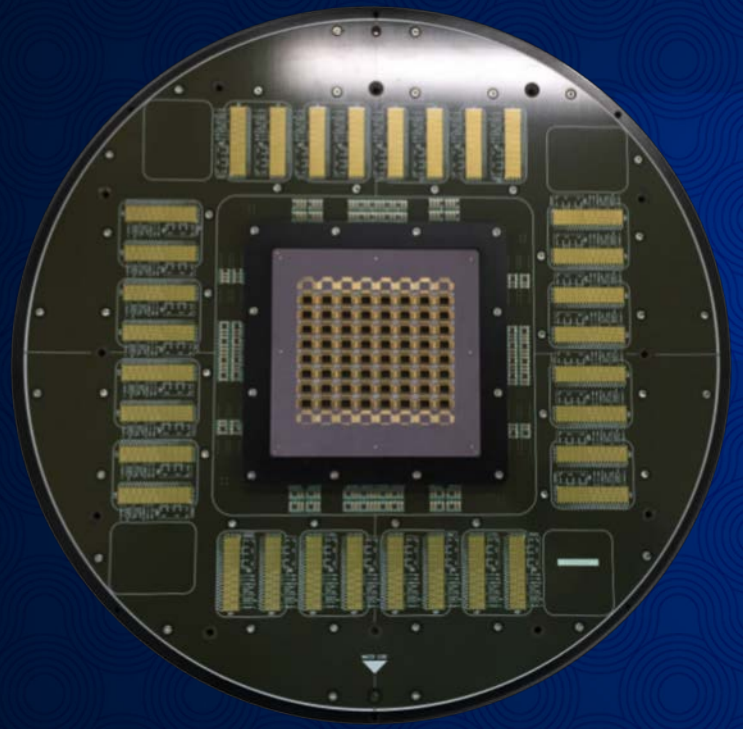
Probe Card Design Specifications			
DUT	63	DUT Array	7x9
PIN	< 15K	pitch	< 100um

CIS Probe Card

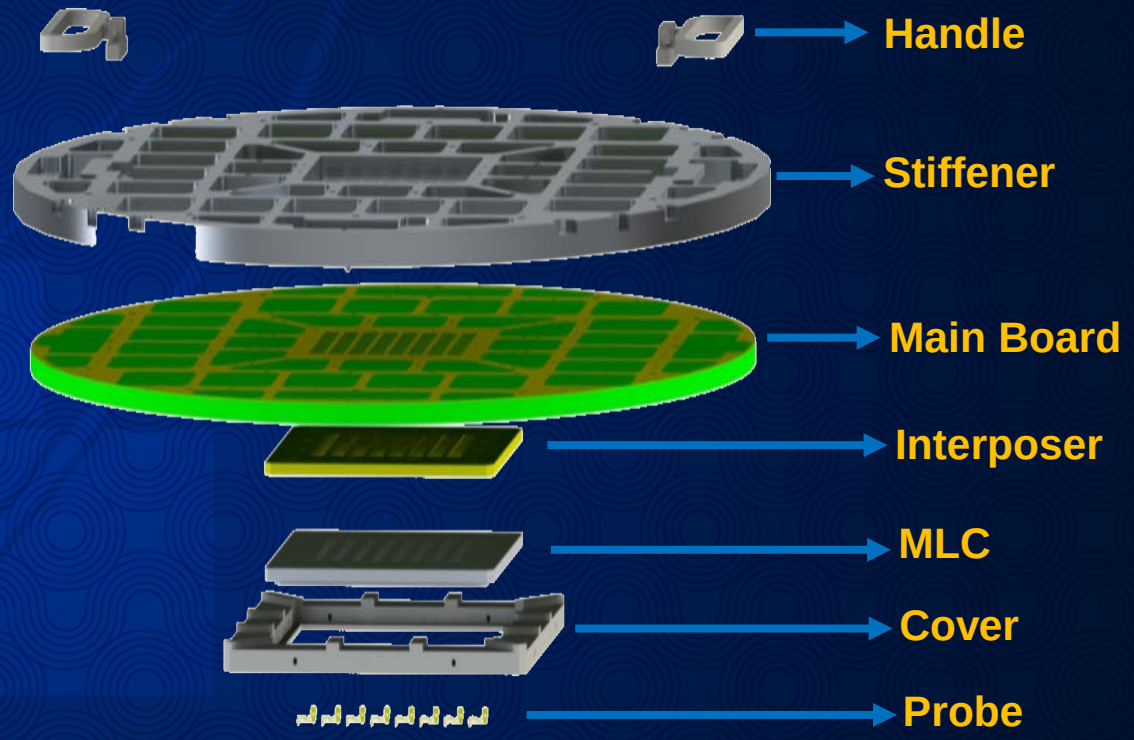
- **CIS probe card must have cavity to transmit light to wafer**
- **MEMS probes are positioned on top of MLC(multilayer ceramic)**



CIS P/C Structure



Wafer side view

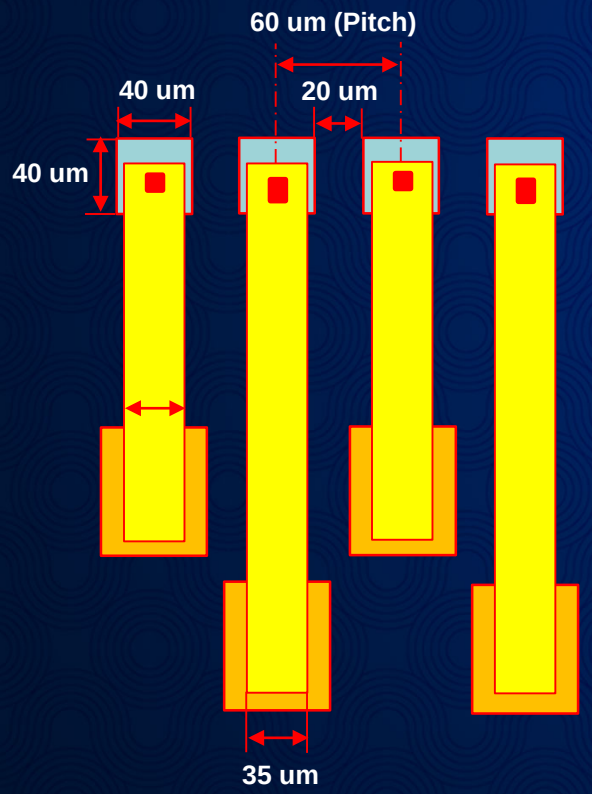


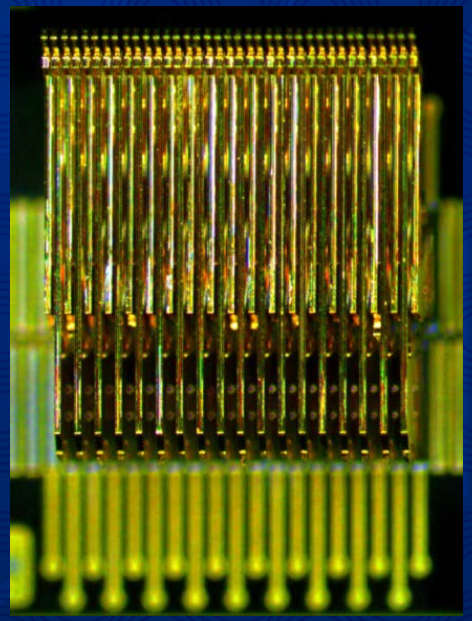
P/C Structure

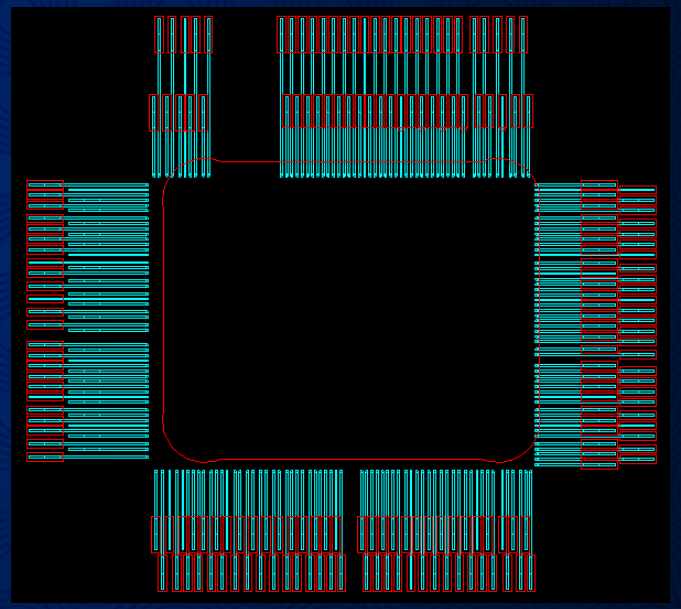
Probe Array

- **Staggered Array using 2 different length probe**
- **60um pitch possible (For this design, 100um pitch)**

Staggered Array

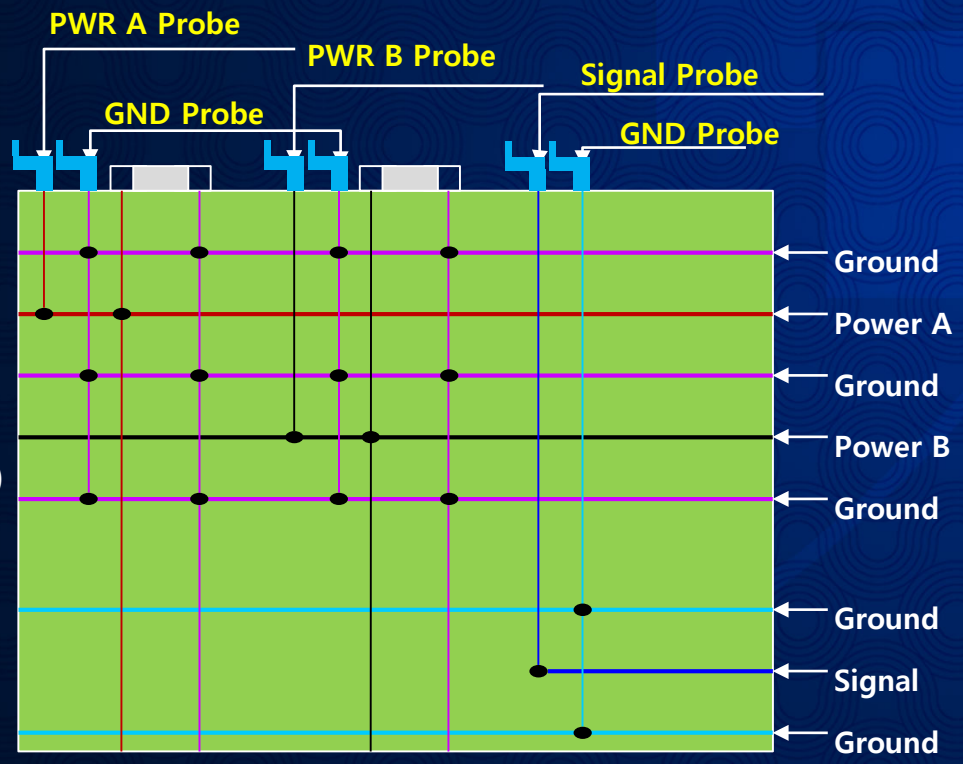


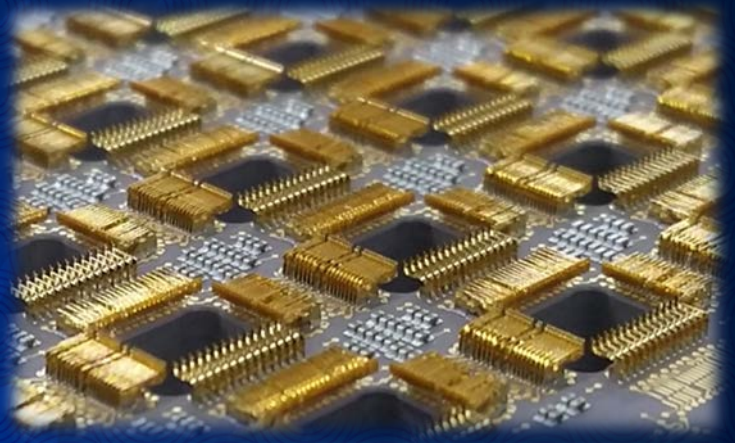


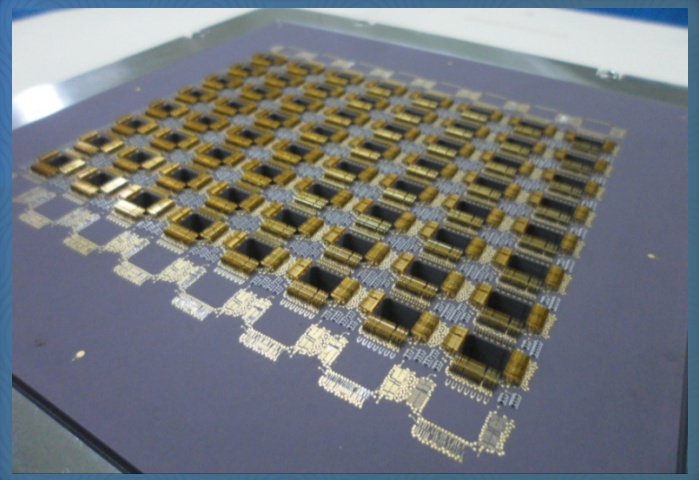


Probe Head

- **Probes and MLCC are bonded on 40+ layer MLC(multilayer ceramic)**



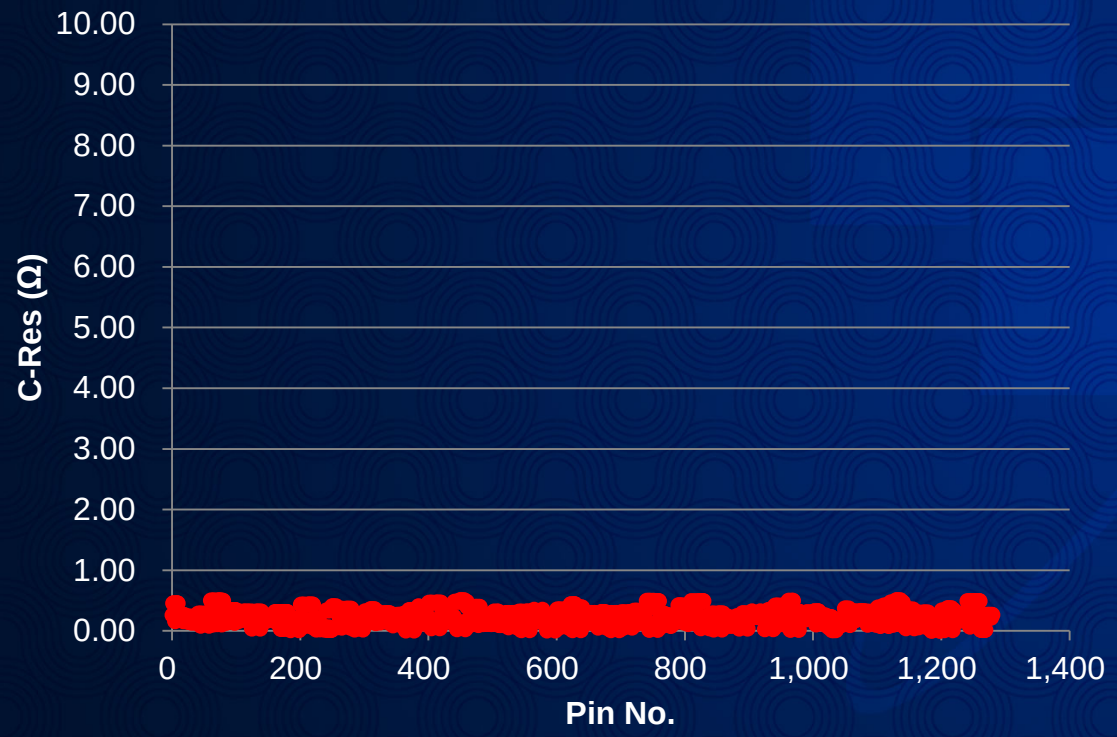


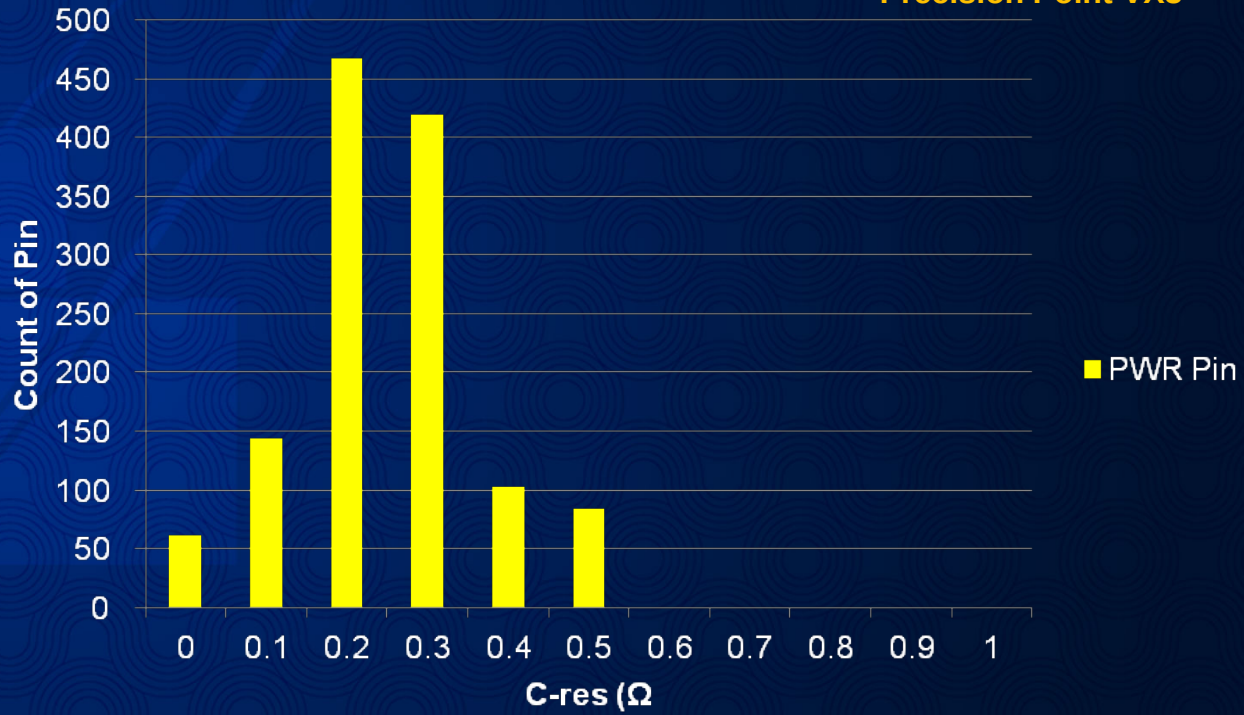


Cres

Precision Point VX3

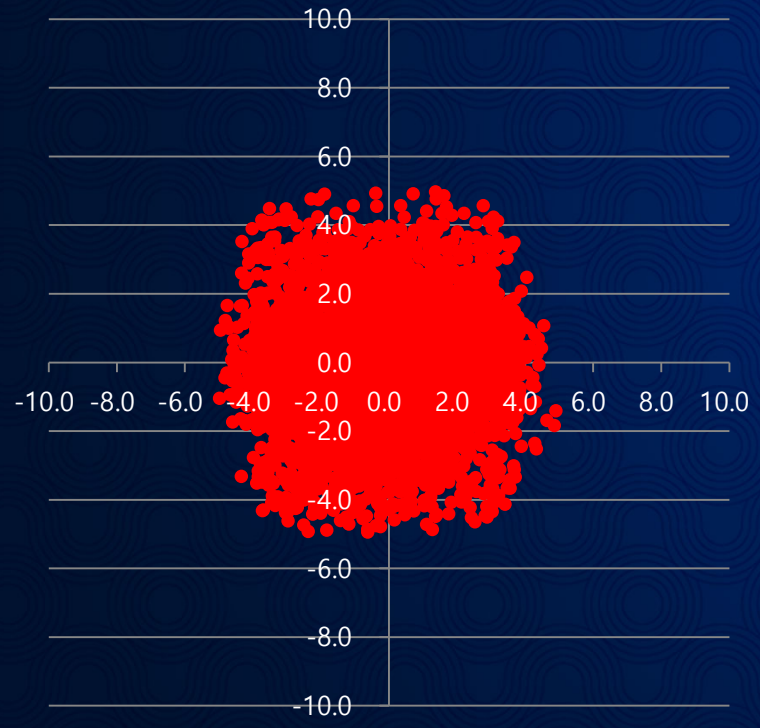
- **Power Pin Cres : < 0.5 ohm over 1,300 pin**
  - **Avg 0.25 ohm, Stdev 0.11 ohm**

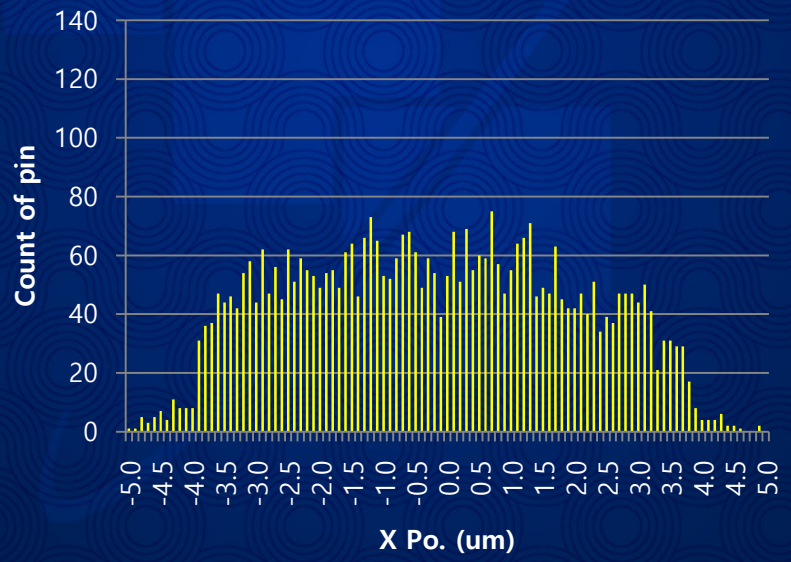


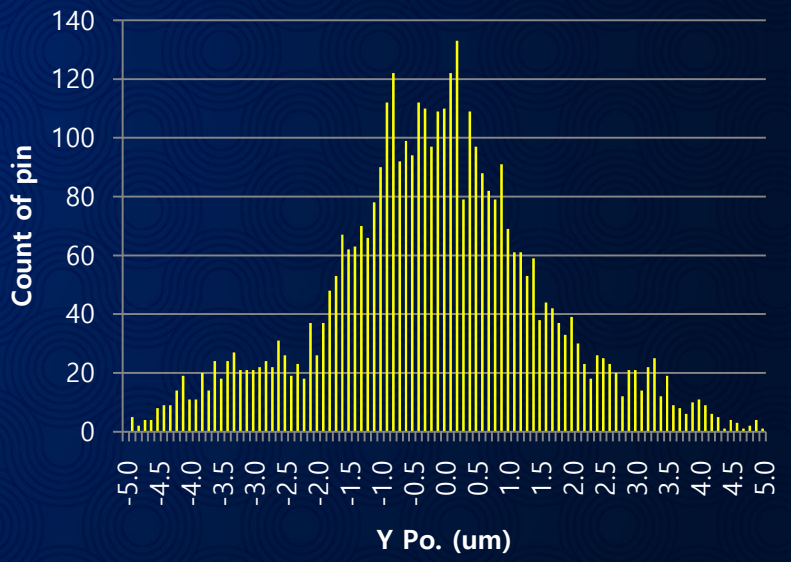


X/Y Position Accuracy

- **Probe's X/Y Position Accuracy : ±5.0um**

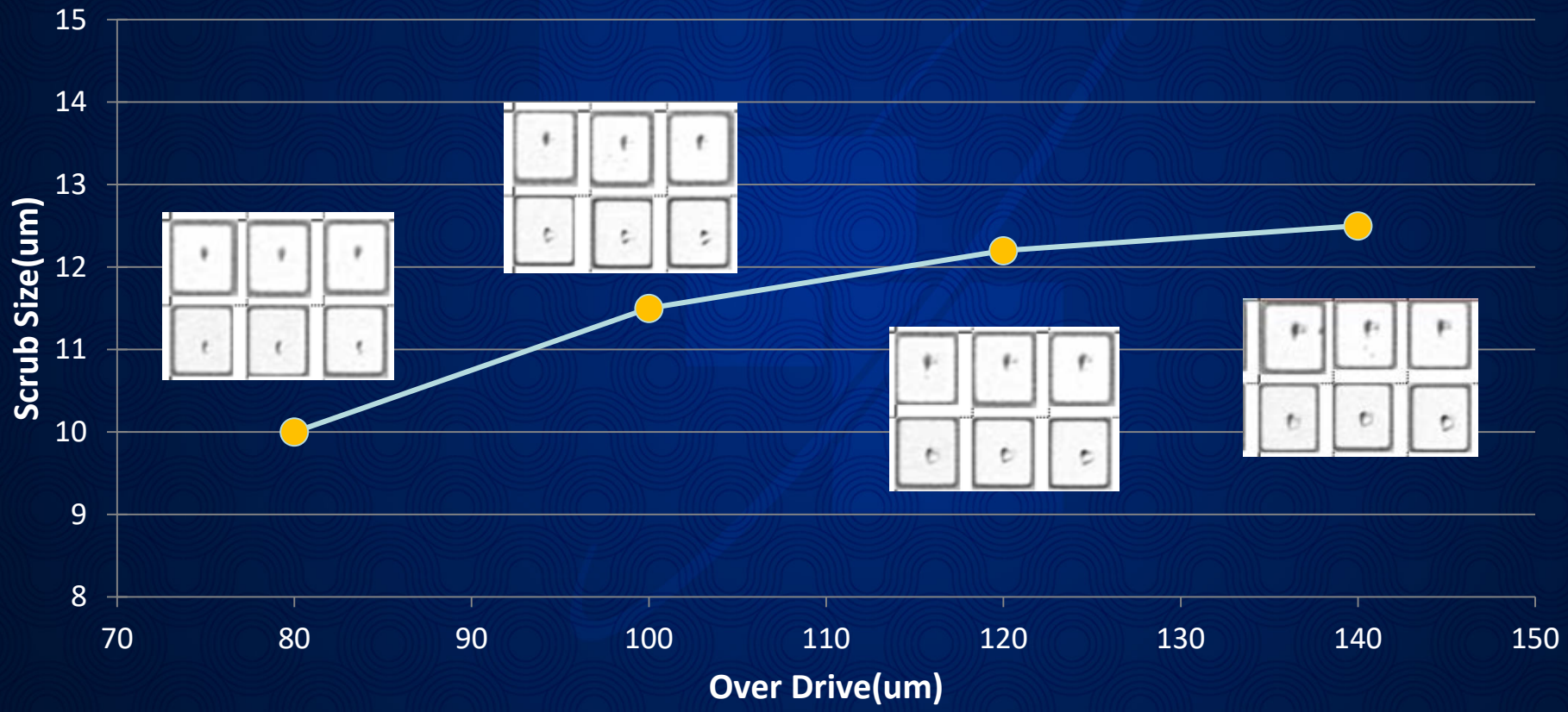






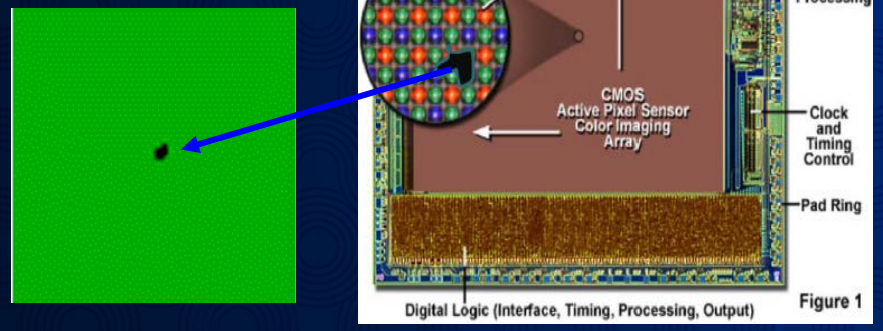
Scrub Mark

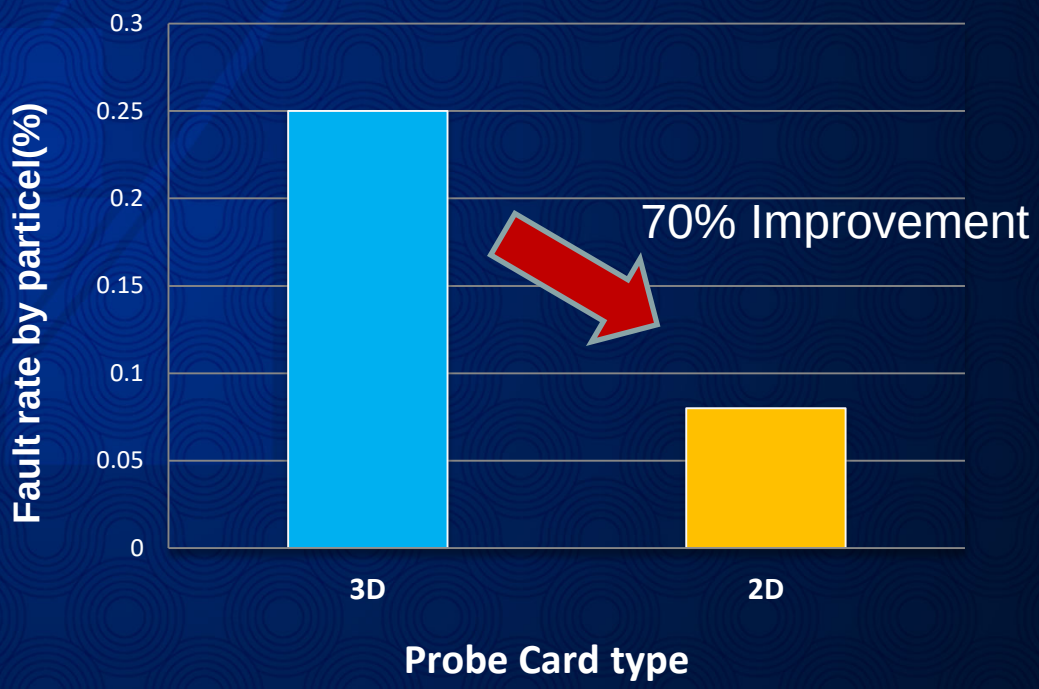
- **Scrub size are under < 12um for testing OD (70~100um)**



Aluminum Particle

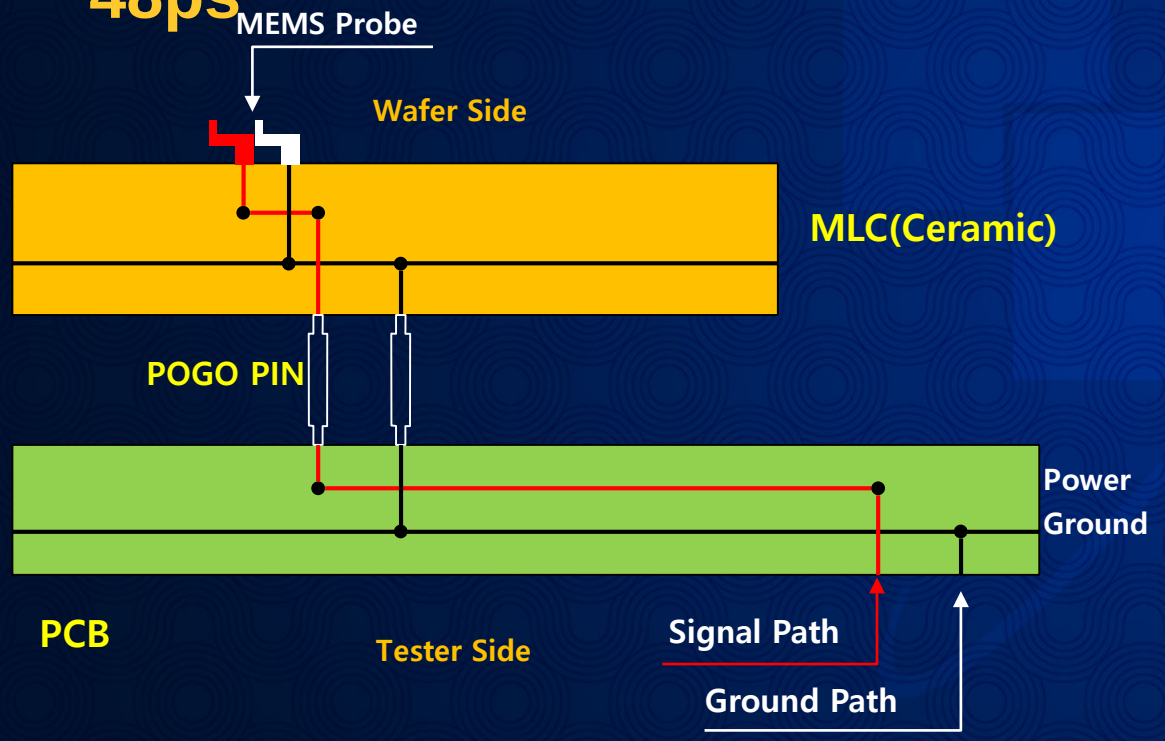
- **Aluminum particle/debris by probing decreases over 70% and increases related wafer yield**



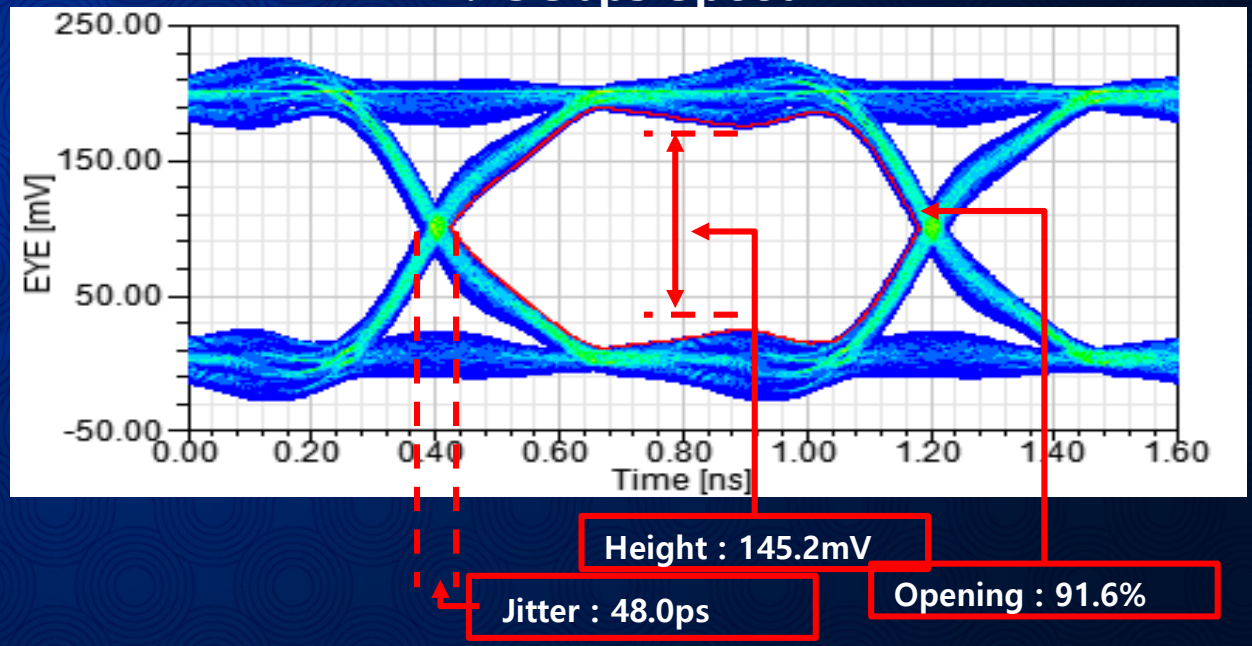


Electrical Characteristics : Signal Integrity

- Ceramic and PCB design to minimizing path length and discontinuity
- At 1.25Gbps, Eye opening > 90%, Height 145mV(200mV swing), Jitter 48ps



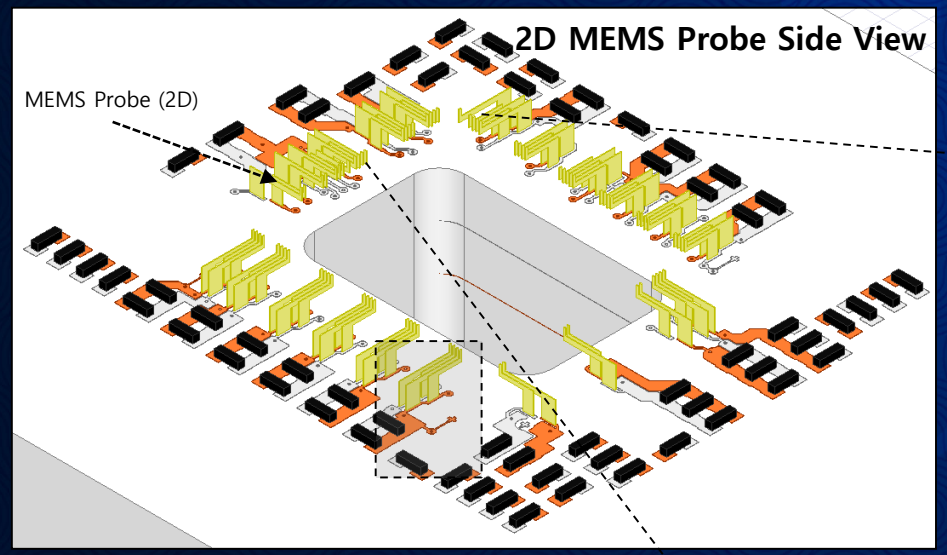
1.25Gbps Speed



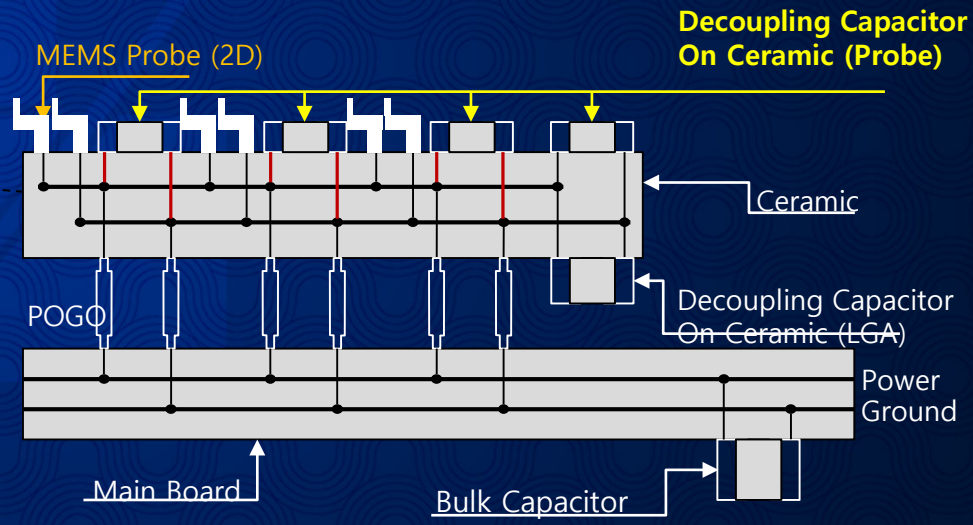
* VIN : 200mV
* Bit Pattern : PRBS
* Tr/f : 100ps (0~100%)
* Termination : 100Ω
* PRBS Length : 2^10-1

Electrical Characteristics : Power Integrity

- **Power and ground plane in MLC near probe**
  + Decoupling capacitor near probe
  → Low power net impedance is possible



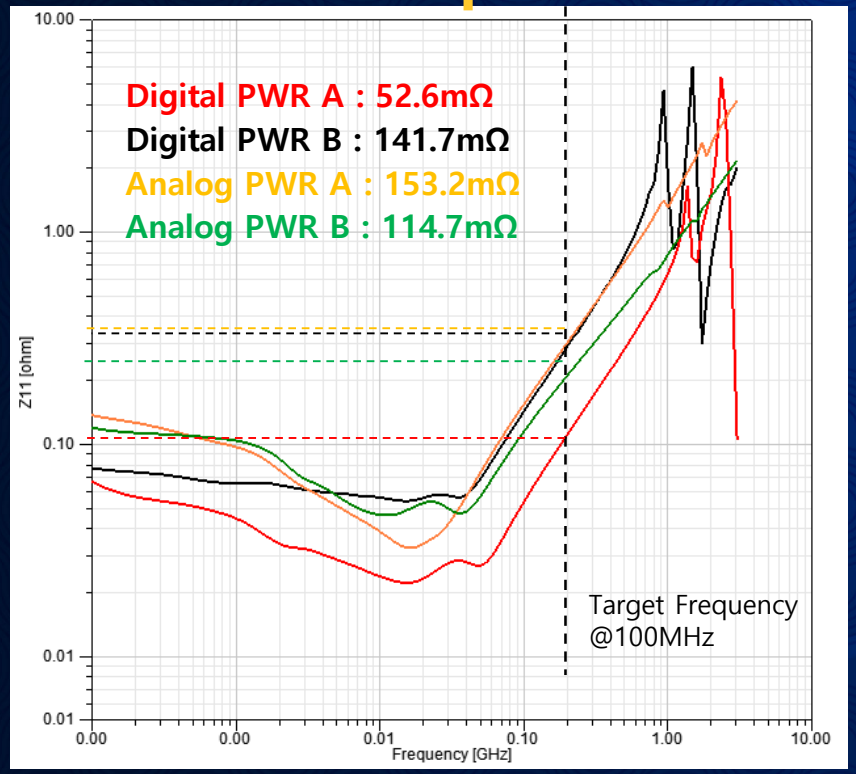
Direct connection between Decoupling Capacitor and Probe PAD



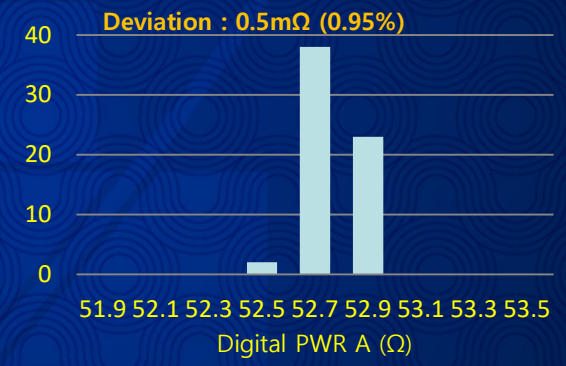
Electrical Characteristics : Power Integrity

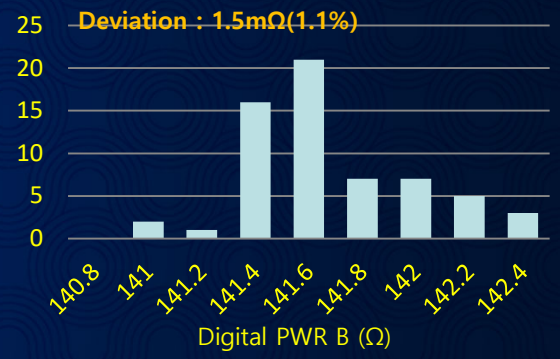
- Power impedances are 50~150mOhm for different power net
- Deviation of impedances between 63 DUT is only under 1%

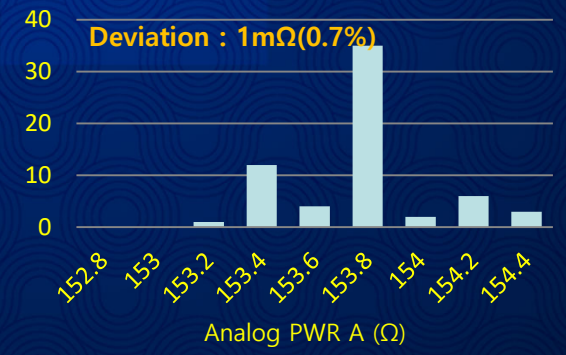
→ Uniform impedance values

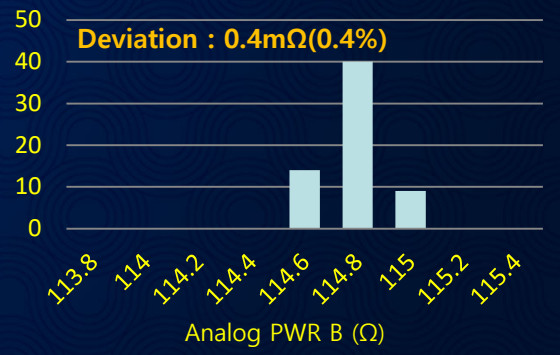


Impedance Deviation between DUTs [63DUT]





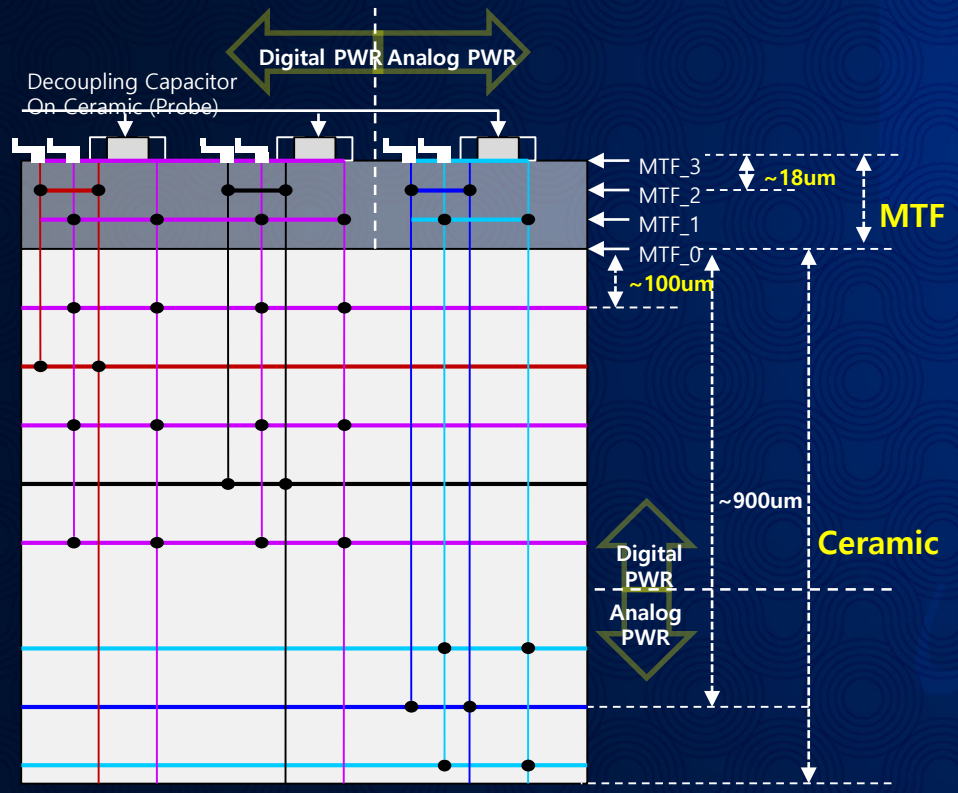


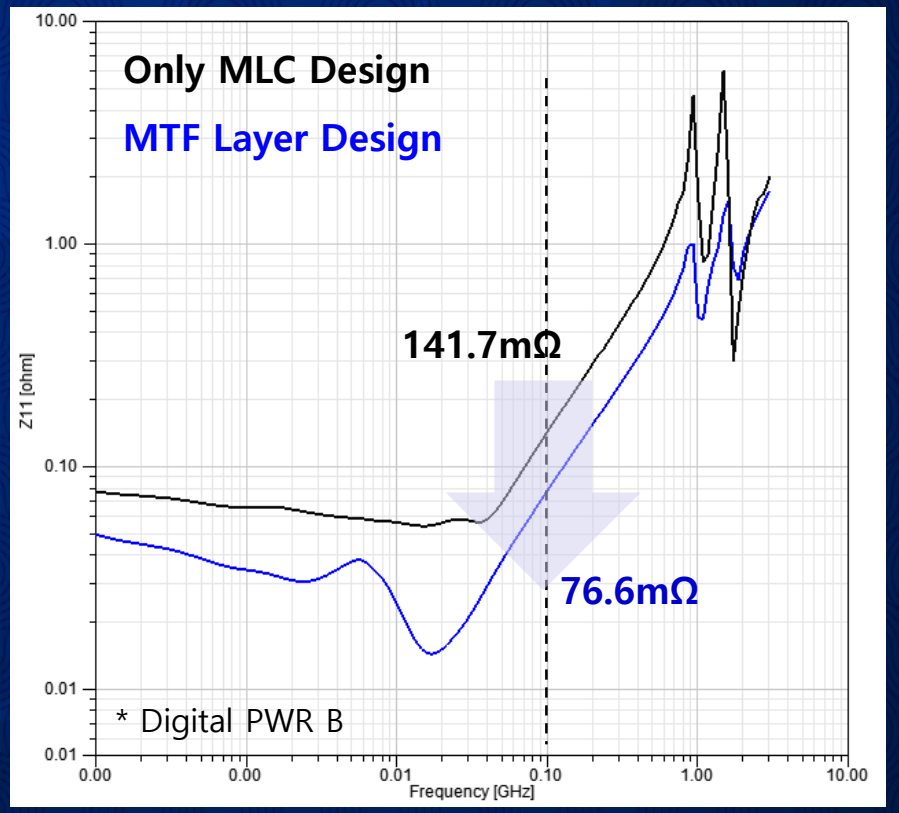


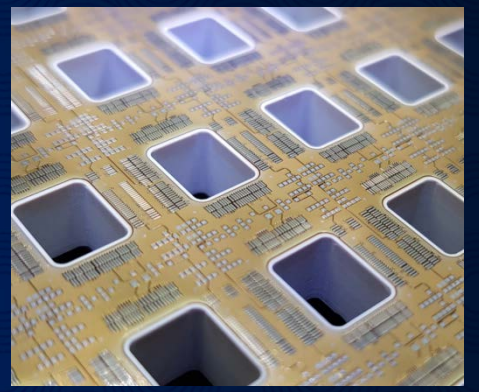
For Future

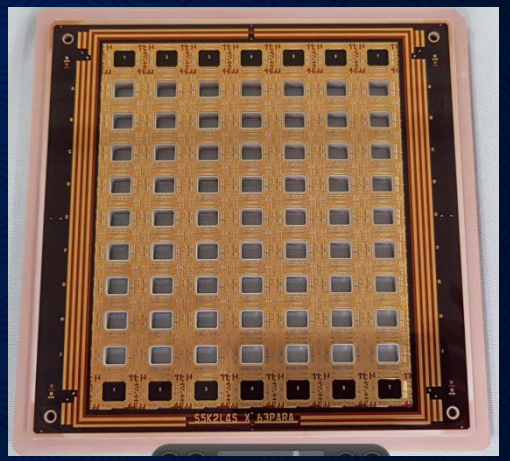
Advanced STF for Low Power Impedance

- **Multilayer Thin Film(MTF) on MLC can significantly reduce power noise level by minimizing power loop inductance(thin layer)**





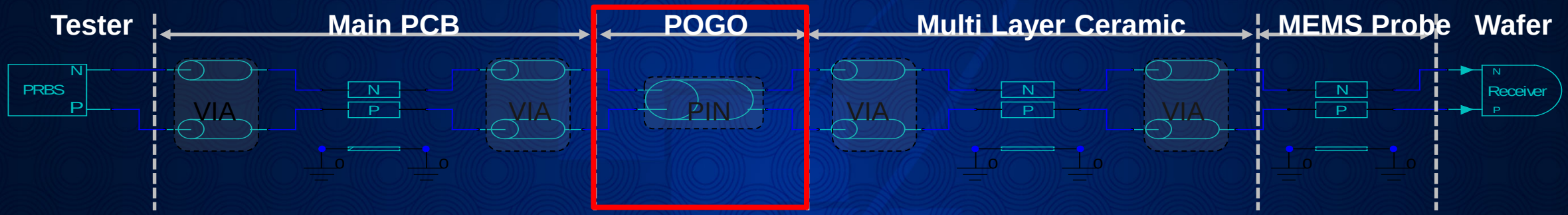




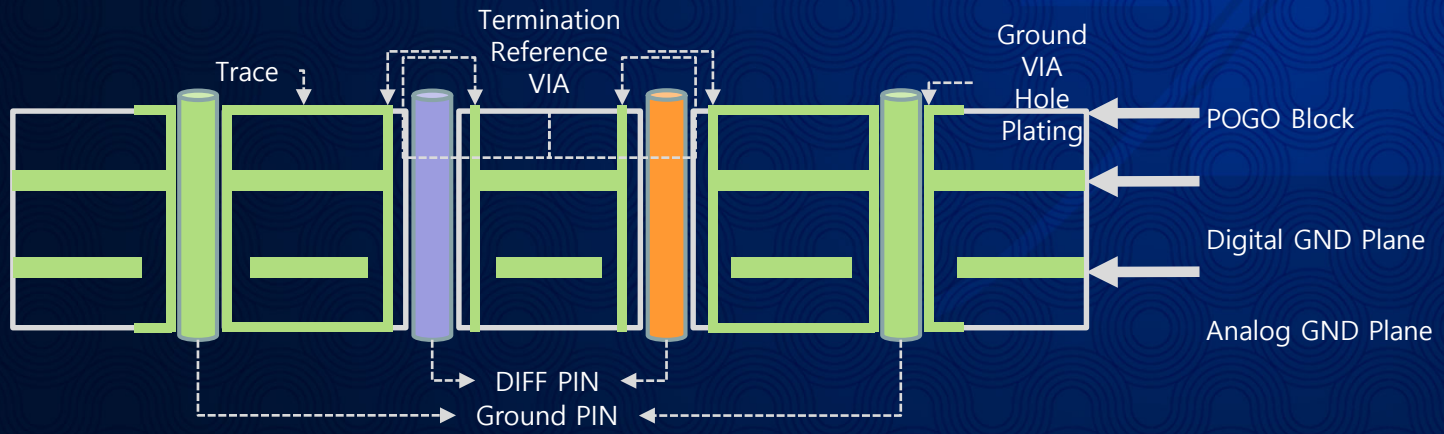
* Co-work with SEMCNS Co.LTD

2.5Gbps MIPI Solution

- **To enhance high speed loss, lowering impedance of high impedance zone(i.e. interposer) is crucial**



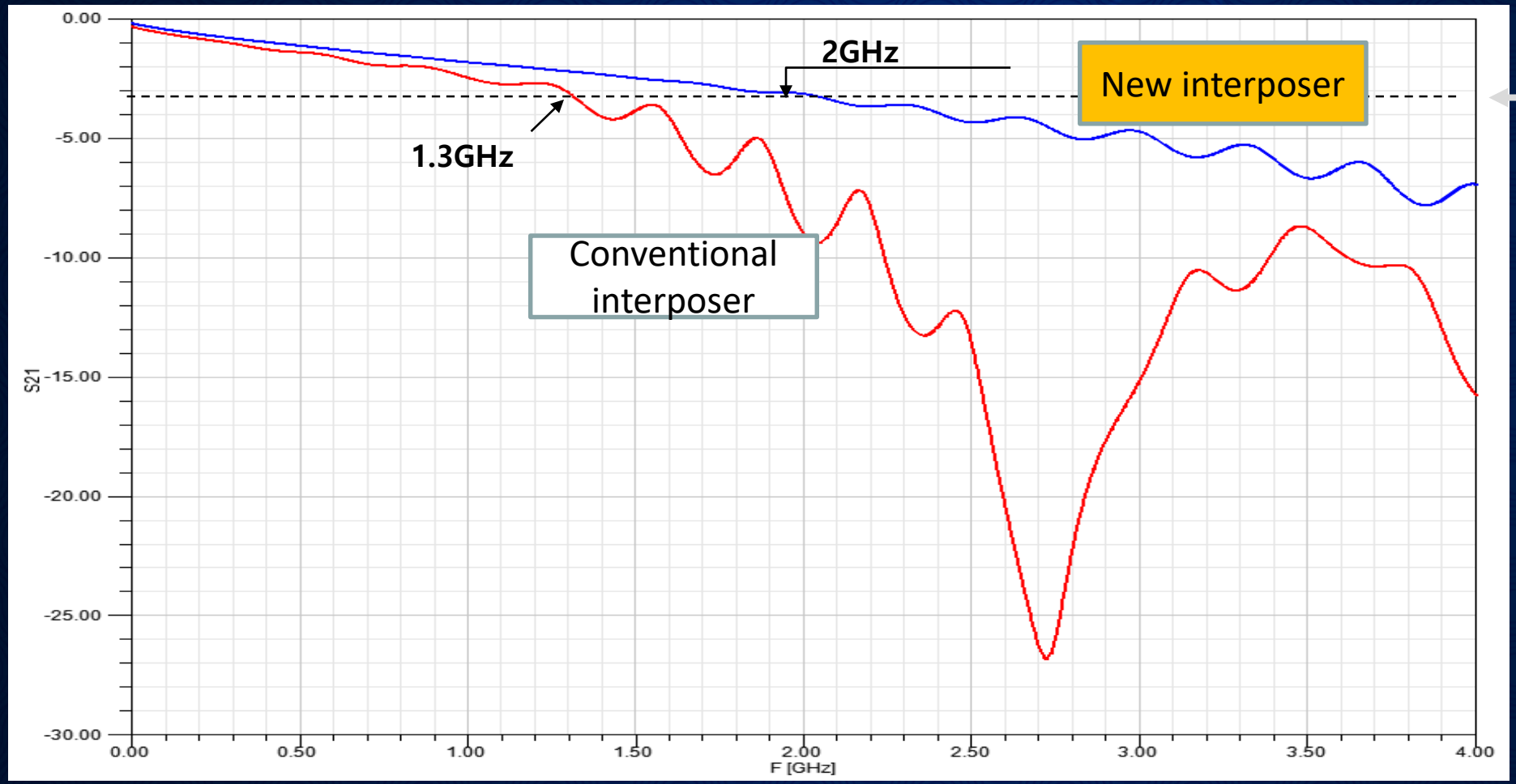
✓ **POGO PIN Impedance Match (Patent Pending)**



- **Using MLB for pogo housing, pseudo coaxial transmission line structure can be attained**

2.5Gbps MIPI Solution

- **3dB band width is greatly enhanced : 1.3 --> 2.0GHz**

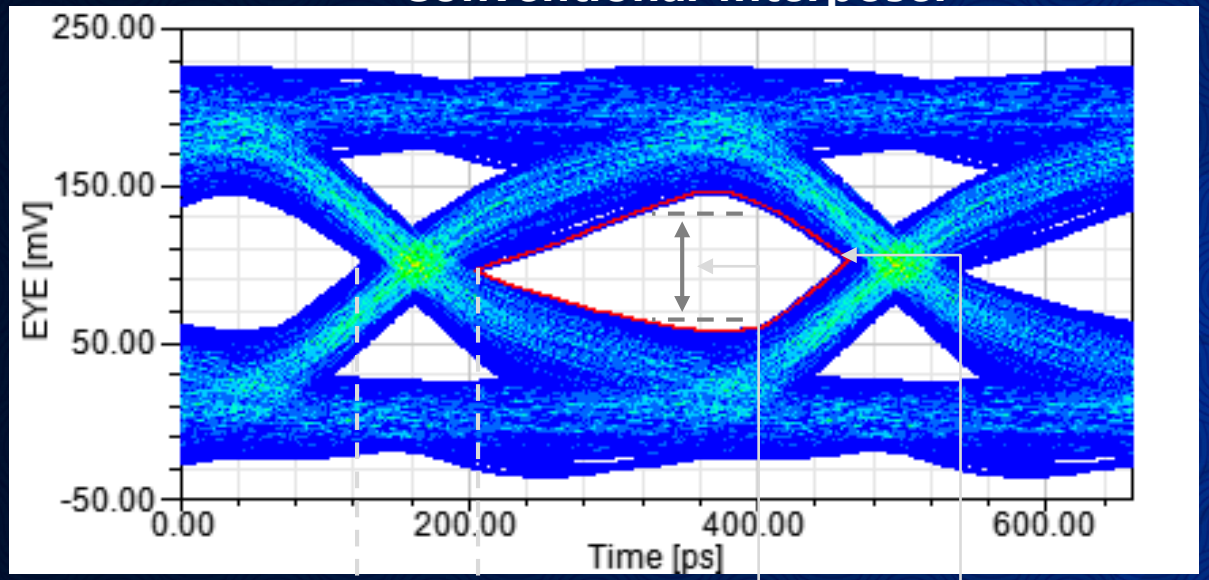


* Simulation Frequency
: 0Hz~20GHz [20MHz Step]

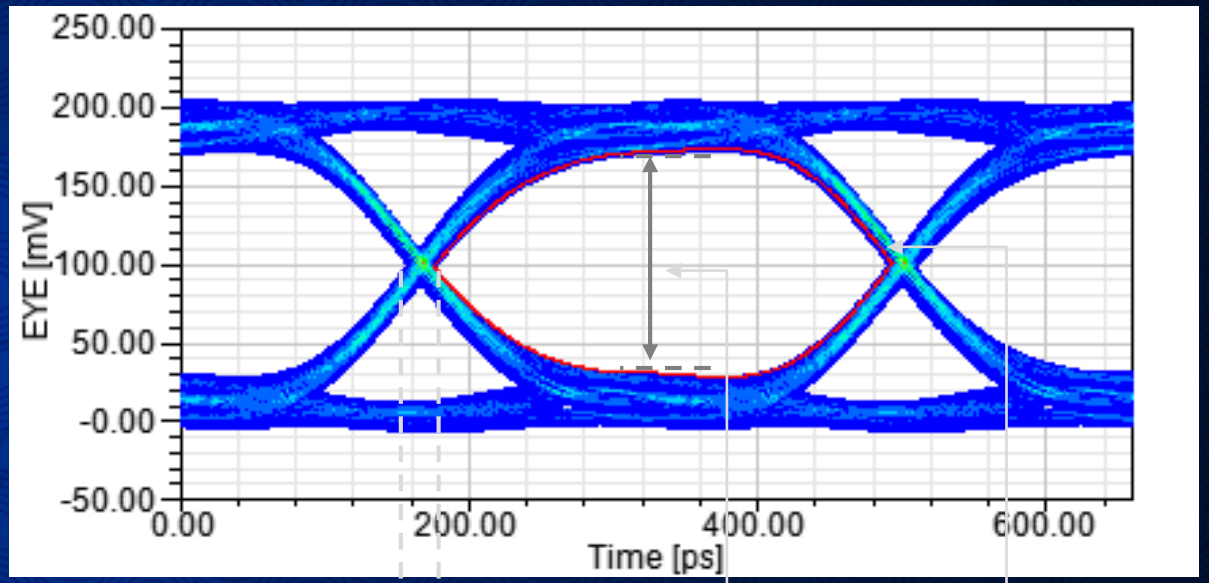
2.5Gbps MIPI Solution

- **Eye characteristics at 3Gbps is much improved**

Conventional Interposer



New concept interposer



* VIN : 200mV
* Bit Pattern : PRBS
* Tr/f : 100ps (0~100%)
* Termination : 100Ω
* PRBS Length : 2^10-1

- Probe Card Path tPD : 1.95ns

Summary

- **Using 2D MEMS technology, high performance CIS probing can be possible**

- **Due to design flexibility of 2D MEMS probe, various special needs for CIS testing can be satisfied**
  - CCC, scrub mark, Al particle control, low impedance

- **For noise immunity and high frequency testing, we propose new STF and interposer solution**

Acknowledgement

Korea Instrument

YoungJun PARK, Probe Design
Sanghyuk Yoon, Bonding Technology
Seongyong Oh, Manufacturing Technology
Dongjoo Won , MLC Design

Q & A

Hybrid (Mixed probe types) vertical probe card

Bryan Lee
(TEPS)
James Park
(TEPS)

Taiwan, October 18-19, 2018

Overview

- Background of development
- Goals
- Methods
- Results
- Summary
- Future work

Background

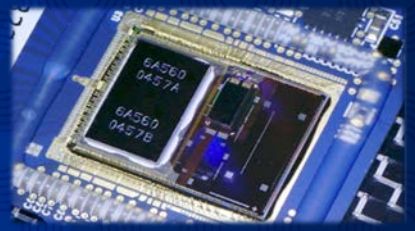
- **Why Hybrid Probe Card?**

A. The fourth industrial revolution effect.

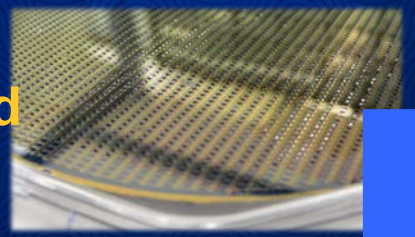
B. Increase wafer production
which is mounted components.

C. Gradual incensement in wafer demand

Hybrid Integration



Single Chipset



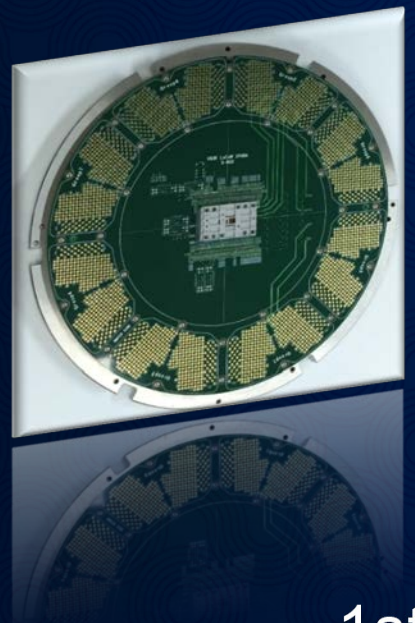
Wafer Scale Manufacturing

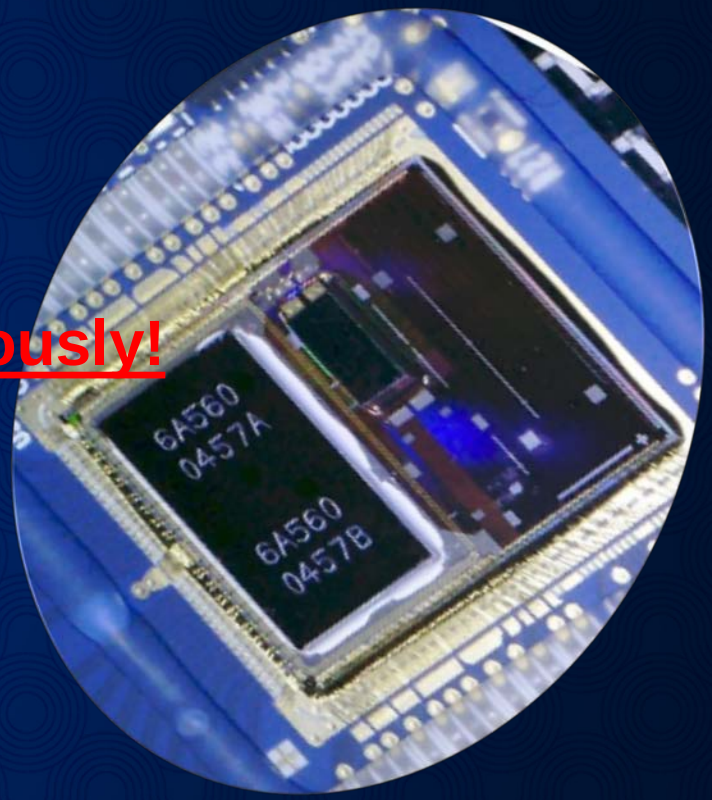
***Demand Increase Trend!**

Background

- **Why necessary!**

- **Wafer test / component test ⟶ Package Test.**
- **Wafer test + component mounted ⟶ Test simultaneously!**





=Cost & time reduction !!!!!

Background

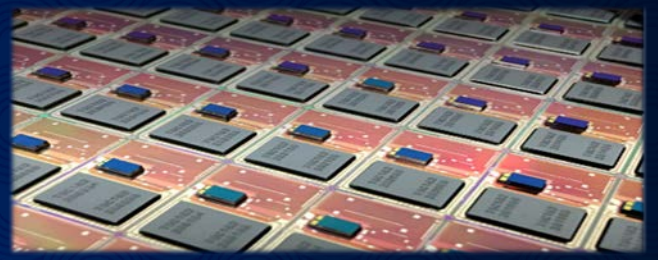
- **Production content**

A. In consideration of the characteristics of component pads and die pads.(Gram force differences)

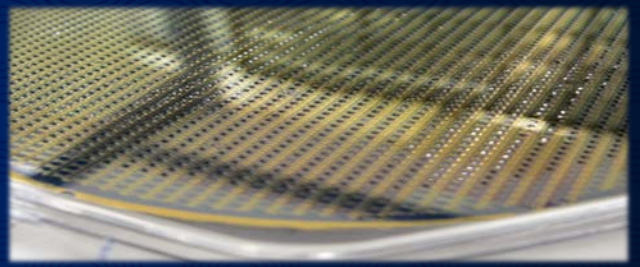
B. Minimize component damage & interference.

C. Expectation for application technology.
(HBM& Wafer Fan out)

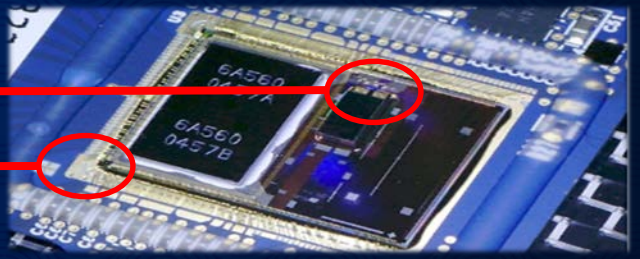
! Difference of Pads characteristic.



Hybrid Integration



Wafer Scale Manufacturing



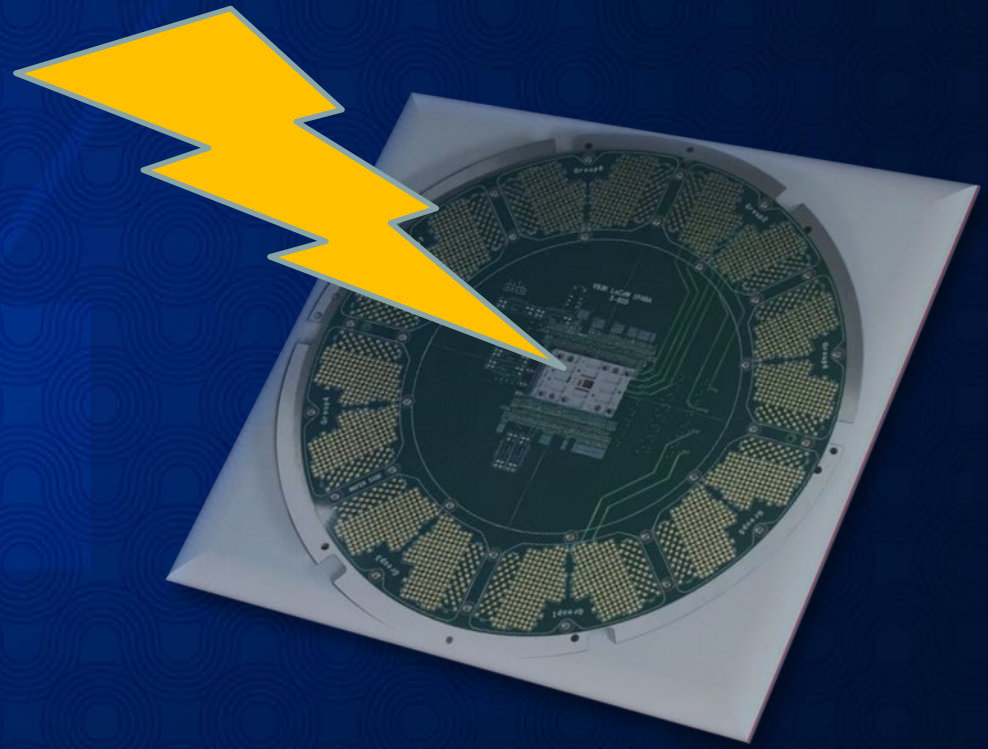
Single Chipset

Goals

A. Select the probe that matches the characteristics of the component on the wafer.

B. Prevent wafer pad damage and minimize component damage.

C. Develop a customized Hybrid Probe Card.



Methods

- **Specification**

Parameters	Specification
Total Probes	506
Para	x1
Minimum pad pitch	102um
Pad Material	Al(P-Die) / Au(Lamp)
Temperature	25C
Pad Size	70.7 x 70.7um
P-die Pad CCC	0.3 ~ 0.4A
Lamp Pad CCC	1A

***Customer requirement**

→ Lamp pad : CCC & CRES => Used Au pogo probe.

→ P-die Pad : CCC & CRES => Used Vertical probe.

***Lamp Pad : Au(Gold) 1A CCC**

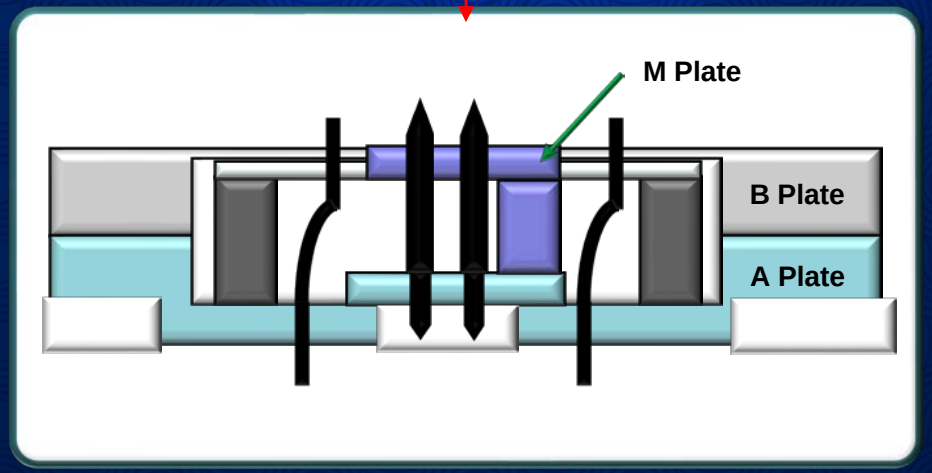
***P-die Pad : (Al Pad) 400mA CCC**

Methods

- **Concept**

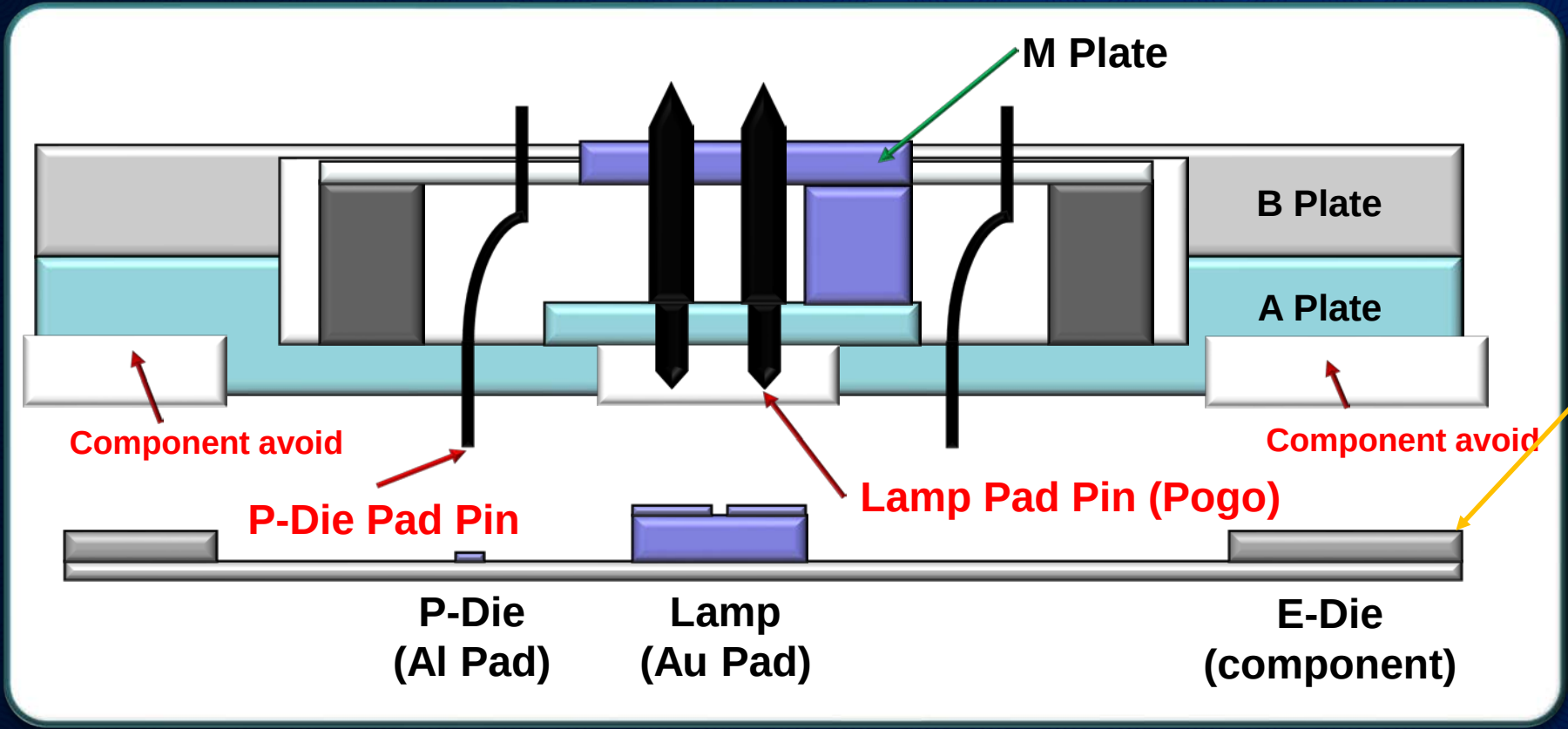
Vertical probe card(Wafer) ⟷ VS ⟶ Pogo probe card(Package)

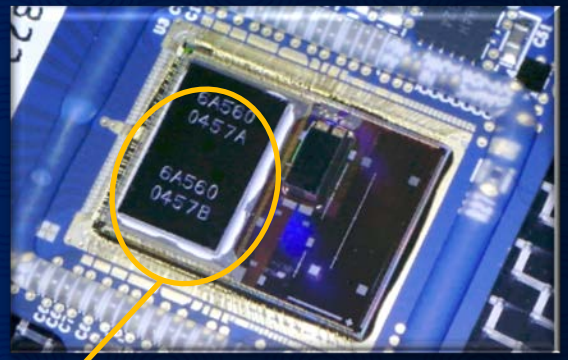
Hybrid probe card



Methods

- **E-die disturbance**





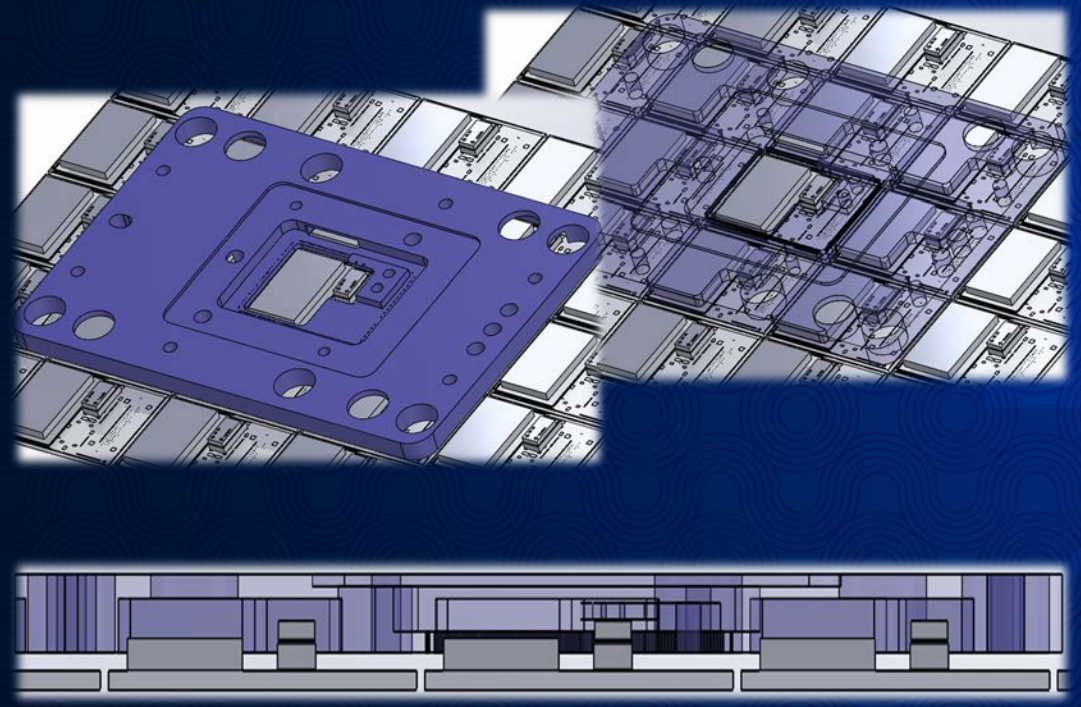
A. Consideration for characteristic of contact pad's

B. Probe length limitation(Overcome)

C. Used Different type probes

Methods

- **E-die disturbance**

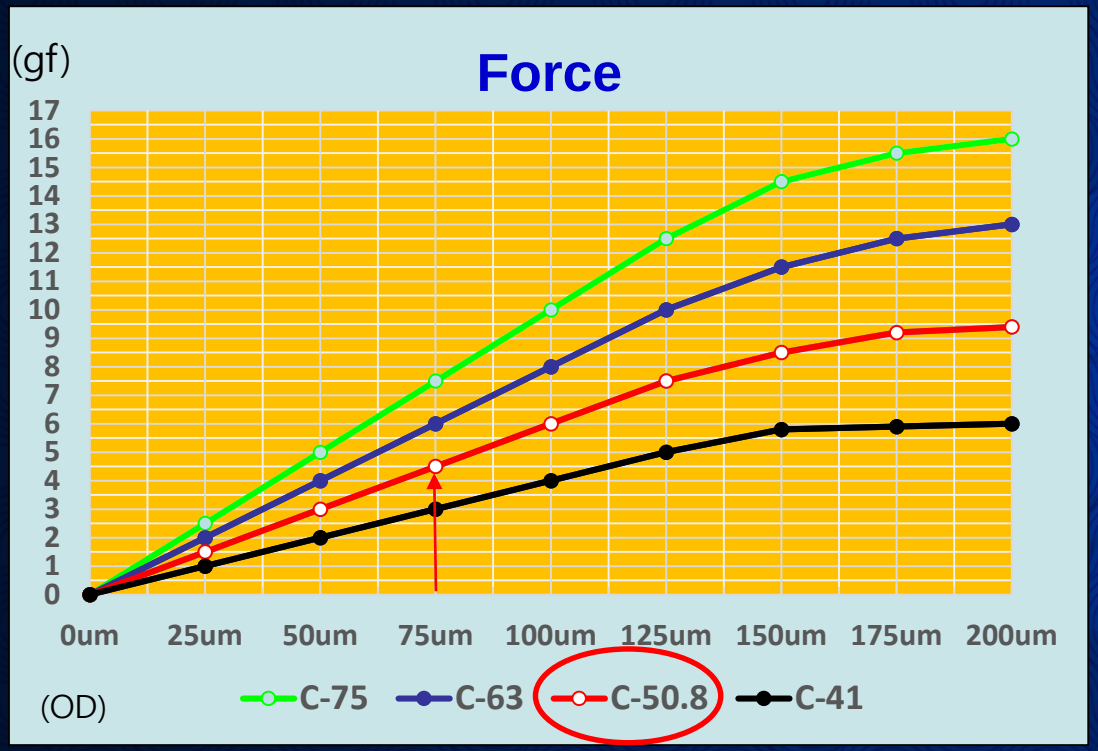


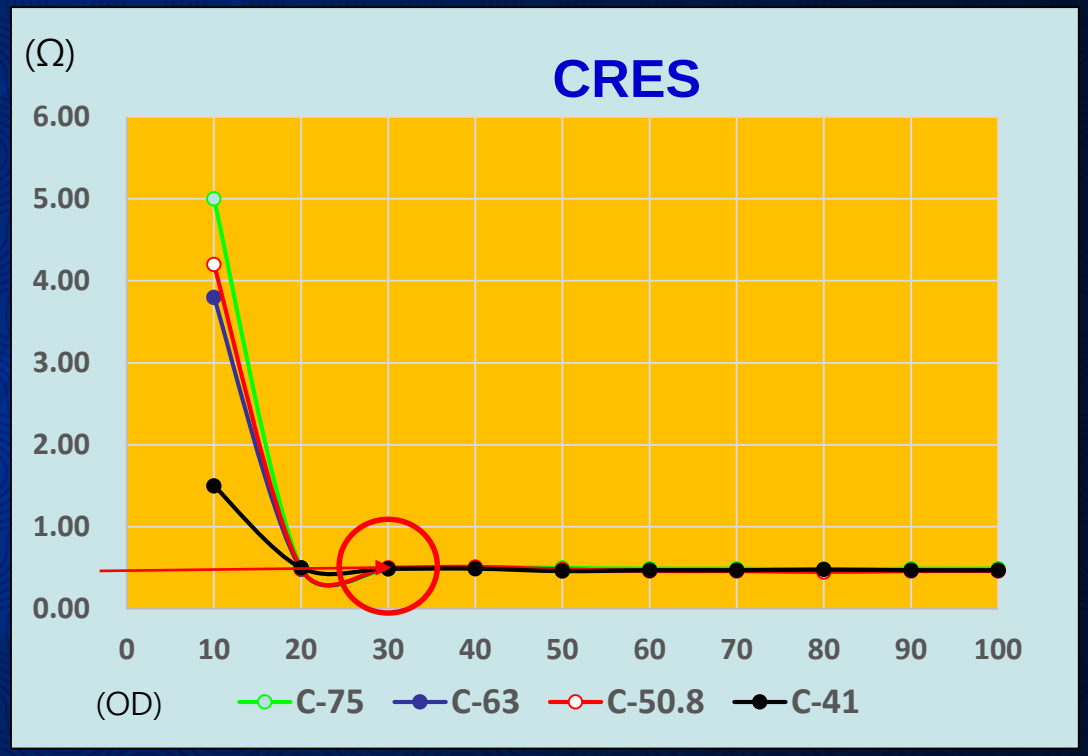
A. Set up e-die avoidance section to avoid disturbance.

B. Based on user specification

Methods

- **Investigate Force & CRES(Vertical)**



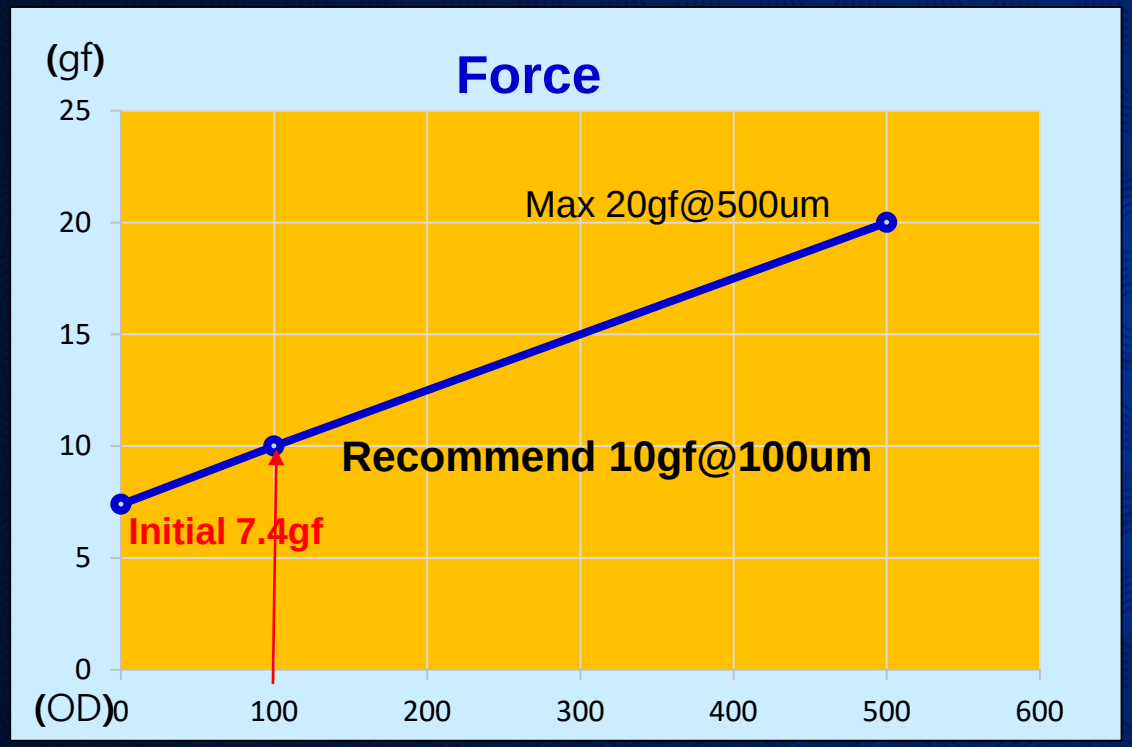


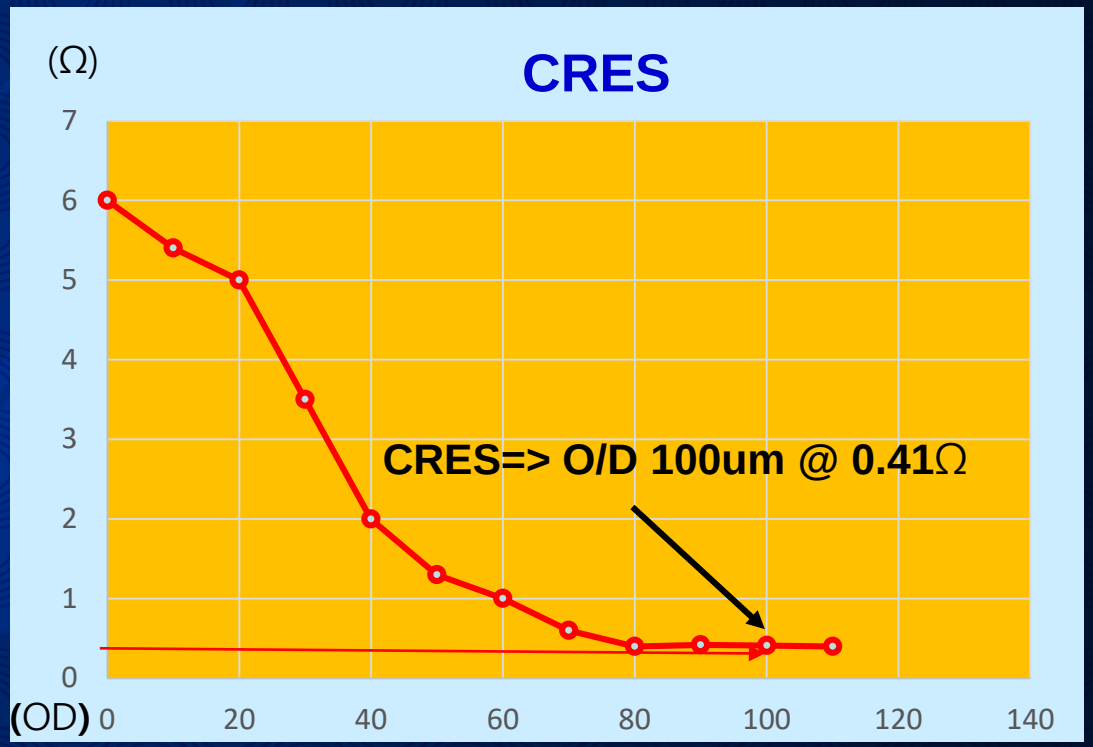
50.8um Dia. O/D 75um => 4.5gf stable

O/D 30um => 0.5Ω Stable

Methods

- **Investigate Force & CRES(Pogo)**



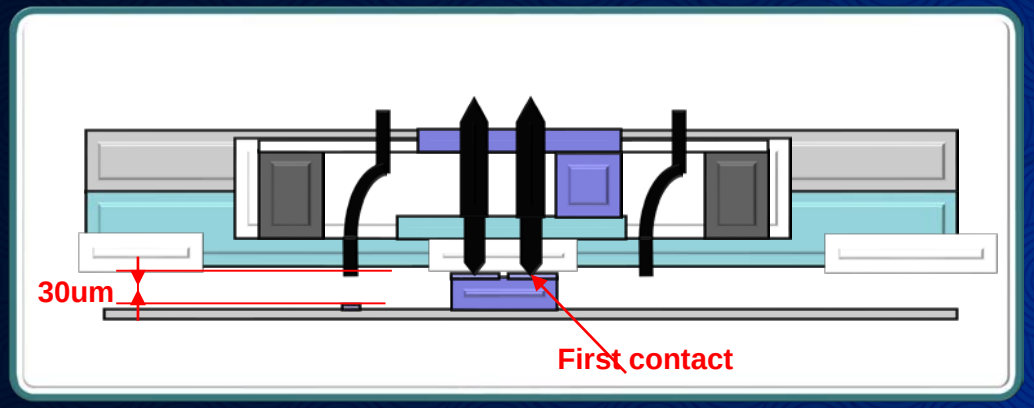


Initial : 7.4gf. O/D 100um => 10gf stable

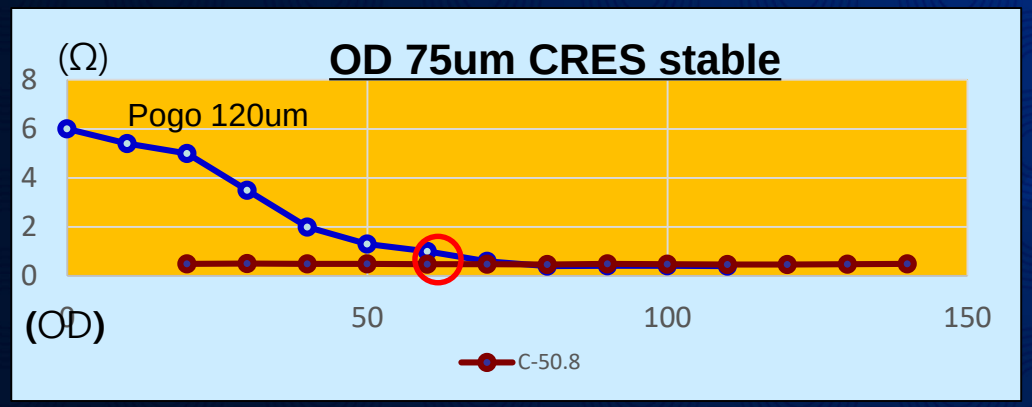
CRES => 0.41Ω Stable

Methods

- **Solution**



30Um First contact for Pogo CRES at OD 75Um
(Vertical Test OD : 75um / Pogo Test OD : 105um)



Diameter	Recommend OD	Probe Force	CCC	Cres.
Pogo(120um)	100um	10gf	1.5A	0.41Ω
Vertical(50.8um)	75um	4.5gf	0.45A	0.50Ω

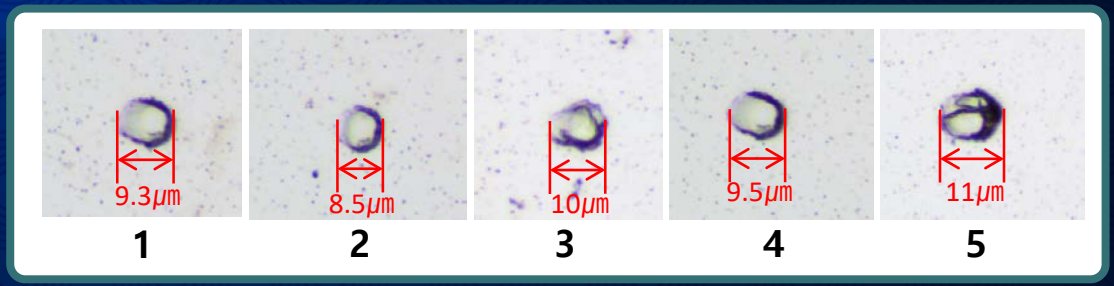
Results

- **Scrub mark & Probe force**

  - ❖ Tip Dia. : From 8Um
  - ❖ O/D 75Um => gf. = 4.35~4.52gf

    => Scrub mark size =8.5~11Um

  - ❖ Temperature : 25 ℃



Results

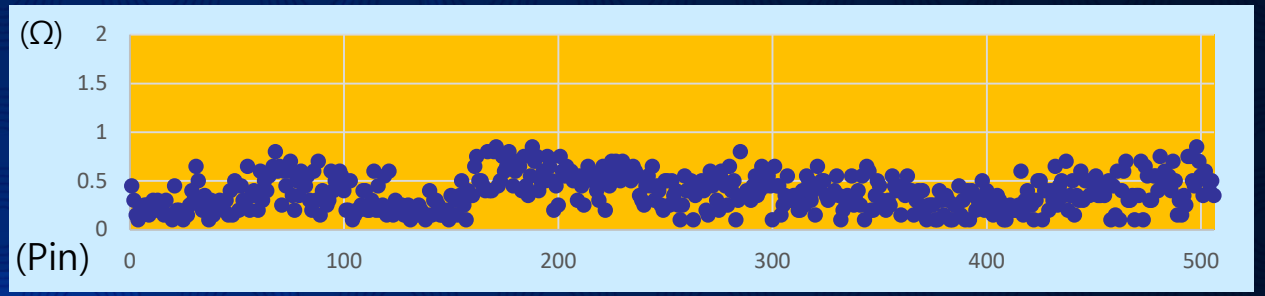
- **CRES under 1 Ohm.**

❖ **Stable CRES on Al wafer**

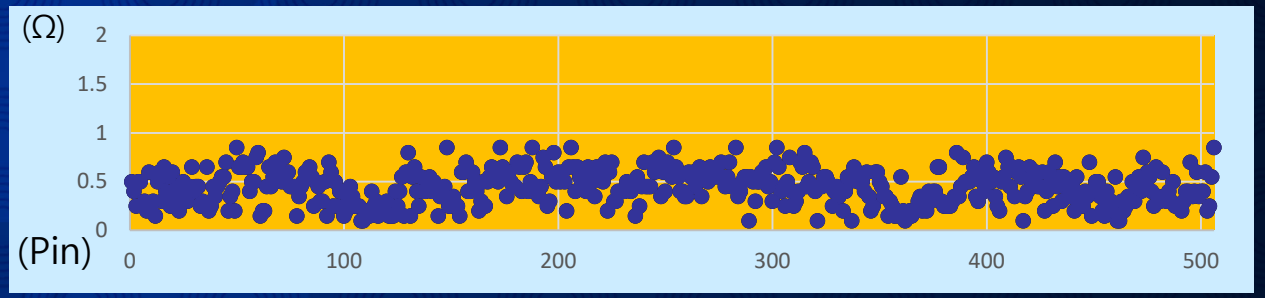
❖ **Cleaning OD : 40um**

❖ **Cleaning recipe: 100x TD / 5x Up/Down**

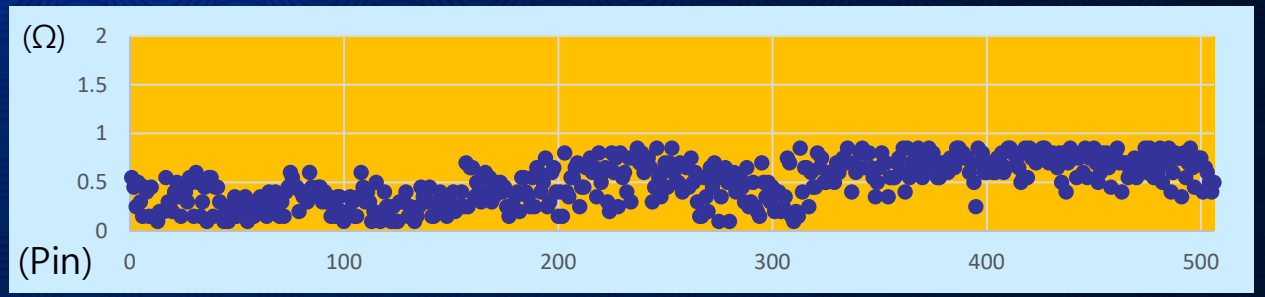
10k TD



50k TD



100k TD



Results

- **Evaluation**

Summary

A. Proper pin force & CRES for each component characteristic.

B. Minimize test skip by disturbance avoid section.

C. Probe card which is able to test component mounted wafer.

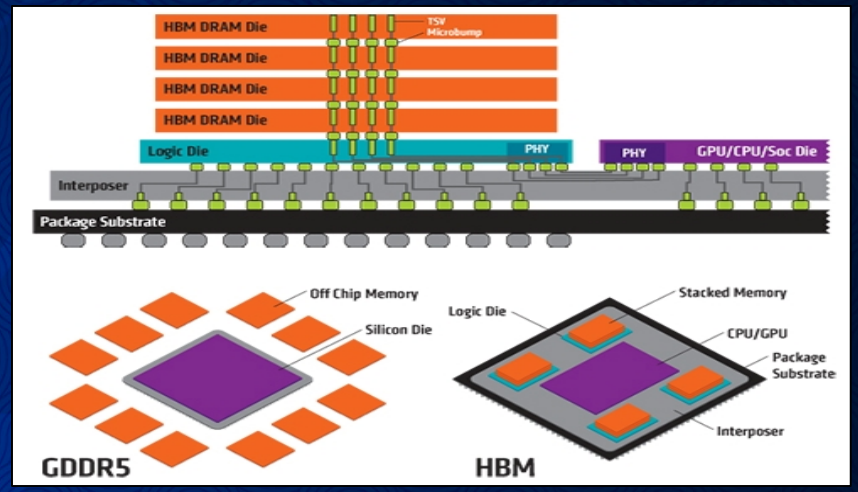
D. Various type of component mounted wafer test.

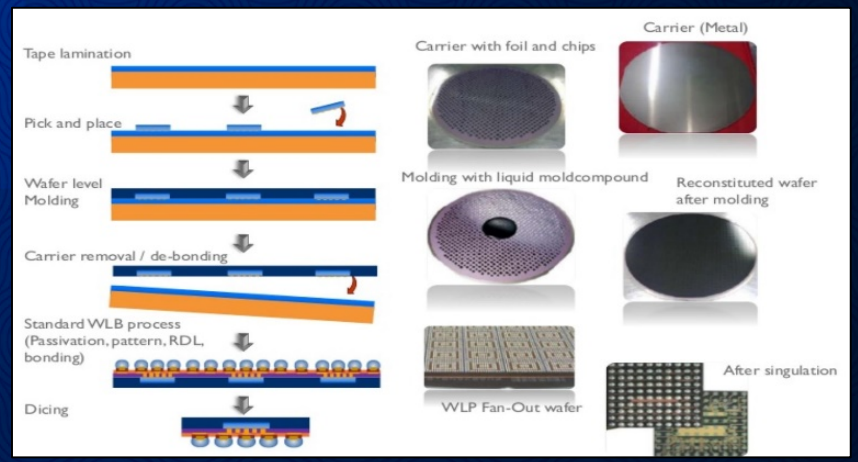
E. Reduction test time and costs.

Future work

- Pad + Package R&D.
- Multi para. production.
- Fine Pitch R&D.

- HBM. (High Bandwidth Memory)
- Wafer Fan out.





Thank you very much

Contact :
Victor Park
CEO, TEPS
teps0301@gmail.com

KGD – Known Good >POWER< Die
Diced Wafer Test at 7 kV and 1000 A

Mauro Serra
CREA Test

Jens Lochbaum
INFOTECH Automation

Rainer Gaggl
T.I.P.S. Messtechnik

Taiwan, October 18-19, 2018

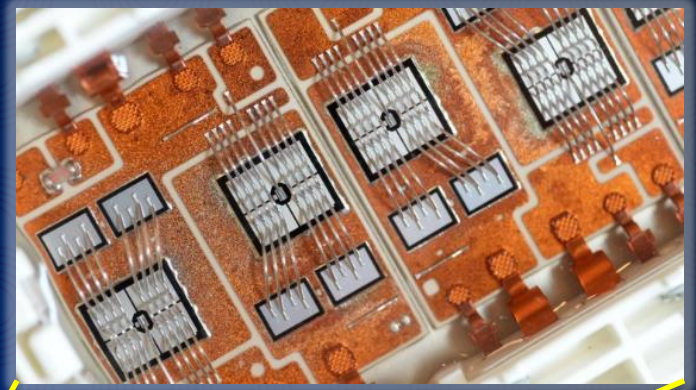
Overview

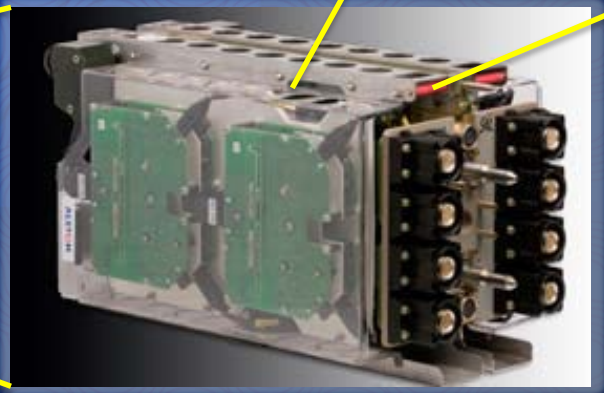
- IGBT Power Modules
- Classical chip test versus "KGD"?
- Challenges: Electric - Physics –Thermal
- Electrical Power Tests
- Chip Handling
- KGD Contactor
- Integration into a System and Challenges
- KGD "Turnkey" Test Cell
- Summary

IGBT Power Modules

High Speed Train (here: Alstom AGV)

IGBT and Diode chips mounted into a single power module (typically up to 32 chips)

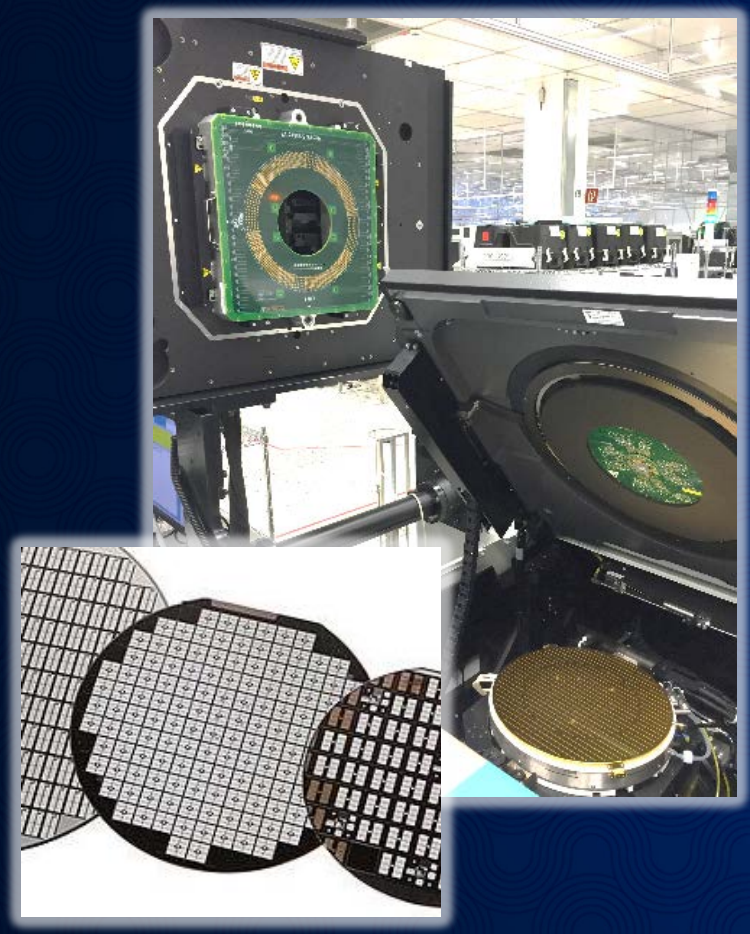




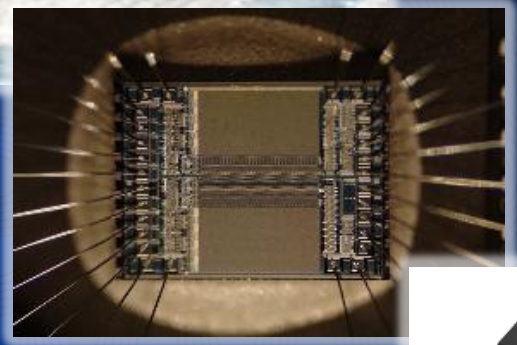
IGBT Power Module, 6.5 kV – 1500 A

Photo courtesy: Alstom

"Classical" Semiconductor Assembly and Test Process

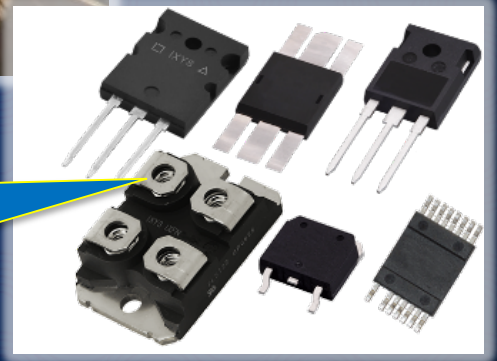


dicing...



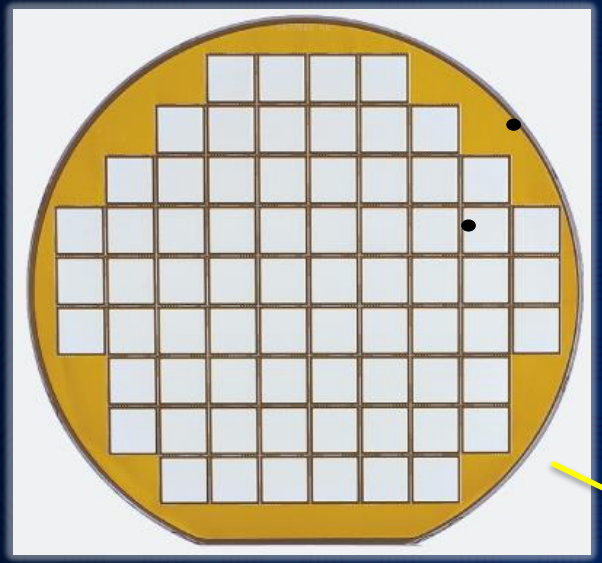
...assembly

typically
single die
or 2 dies

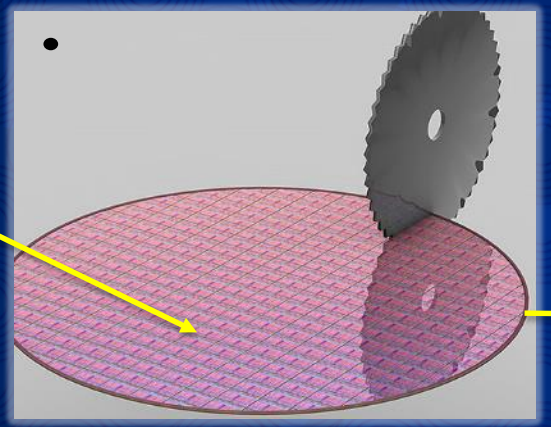


Wafer Sort on Prober... **....Dicing, Assembly....** **...Packaged Device Test**

Modules Yield...it's all about Statistics

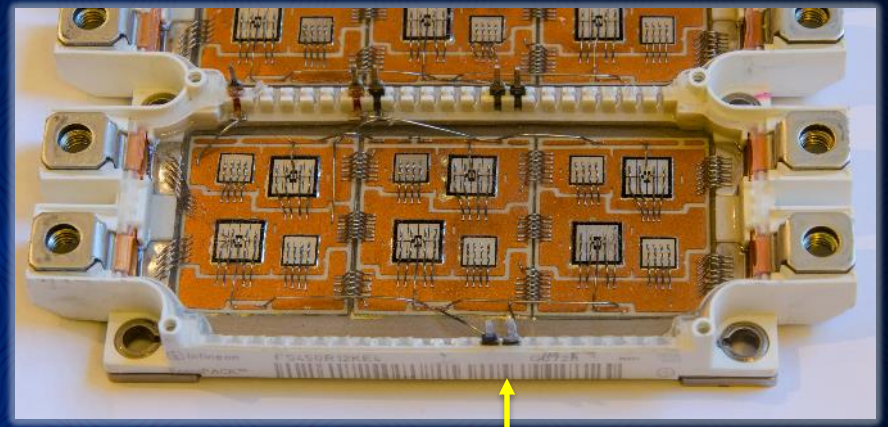


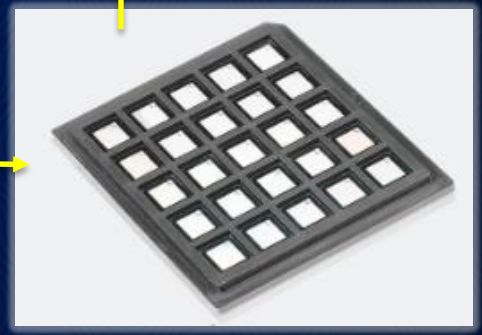
Wafer tested



Cutting damage,
Dicing yield

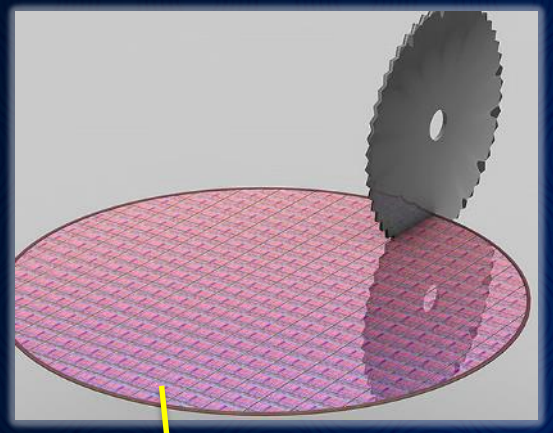
?





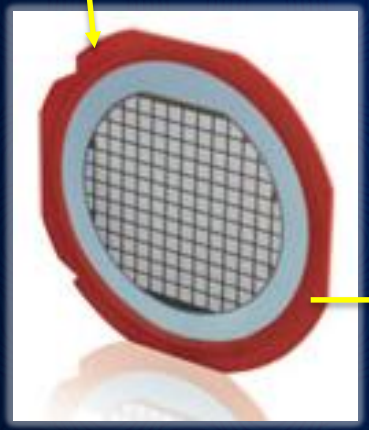
dicing process yield	single package yield	12x module combined yield	32x module combined yield
99%	99%	89%	72%
98%	98%	78%	52%
90%	90%	28%	3%

"Known Good Die" - Concept



Dicing

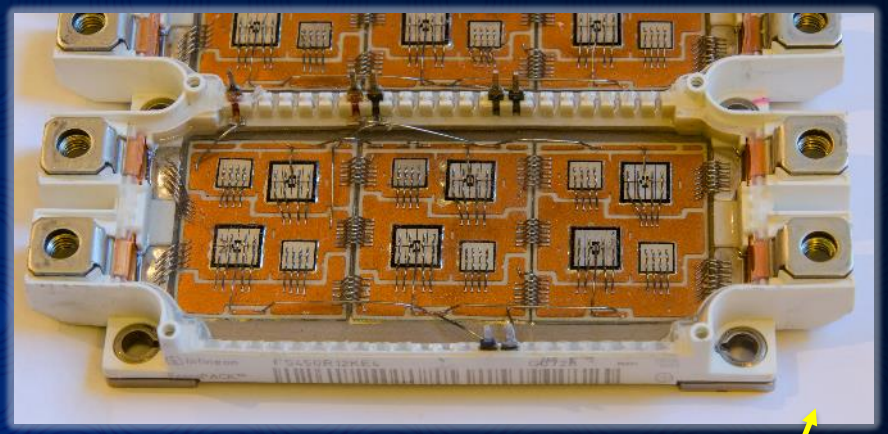
?



Diced Wafer
on Film Frame

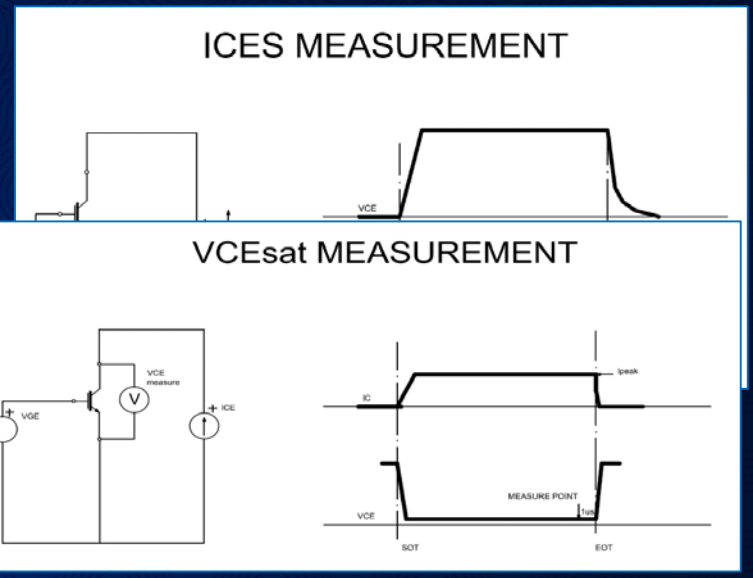
KGD Test - Singulated Chips

Module Assembly – with
Known Good Dies !



"Power" Die – Electrical Tests

2 main test regimes: Static and Dynamic Tests



– **Static Tests (DC) :** device steady state parameters verification (no large power dissipation in D.U.T.)

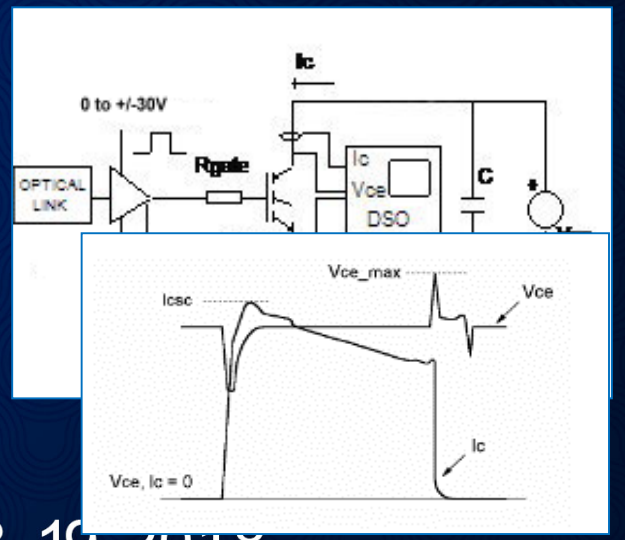
examples:

- High voltage leakage test ...up to **10 kV – but just a few mA**
- Vcesat, Rdson (high current test) ...**up to 200 A – but just a few V**
- Vgeth (gate threshold test)

– **Dynamic Tests (AC)**: device switching parameters verification large power dissipation in D.U.T, both high voltage and high current are **present at the same time)**

examples:

- double pulse test: switching losses of IGBT, diode recovery
- avalanche test: dissipation of breakthrough energy into DUT
- short circuit withstanding test: highest current – **1000+ A**!



Dynamic Test - Example

Unclamped Inductive Switching - **UIS** or **Avalanche** Test

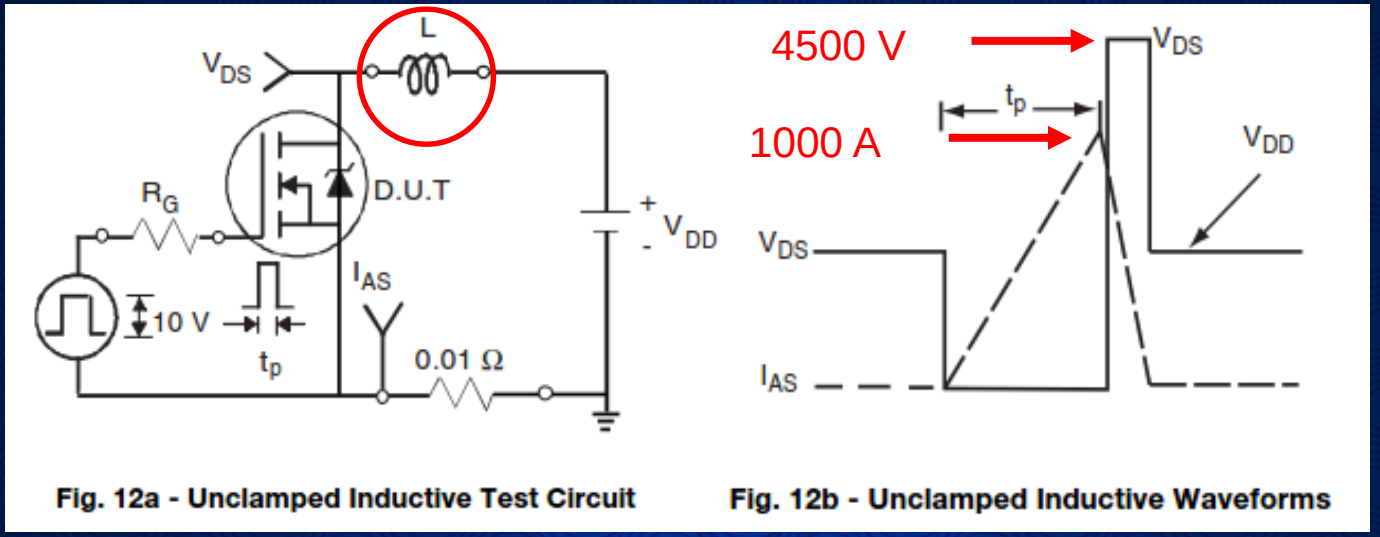


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

from Vishay data sheet

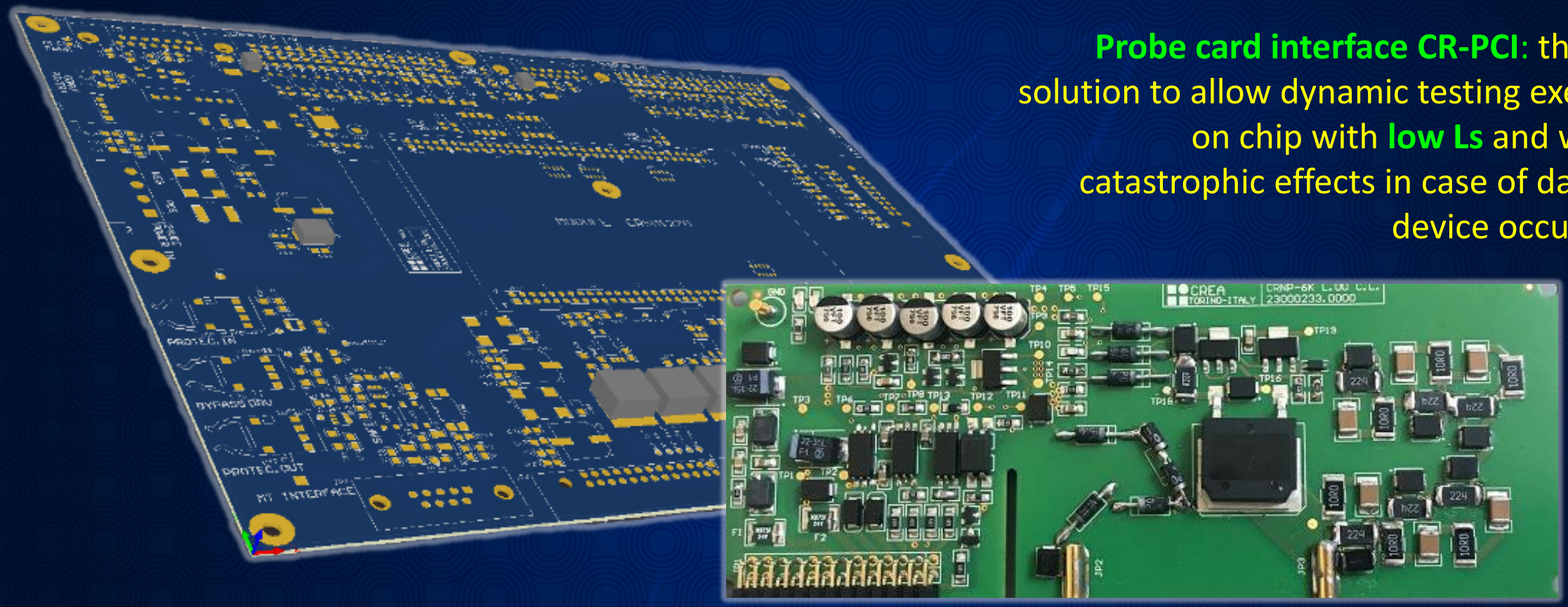
- **Energy** stored in inductor **is dissipated inside D.U.T.** at switch off.....

.... if everithing goes right.

- If things go wrong (DUT shorted): energy **is dissipated elsewhere**, and it IS dissipated (in probes, backside contact...)

- It's similar to speeding downhill without brakes on:

LOW STRAY INDUCTANCE Technology

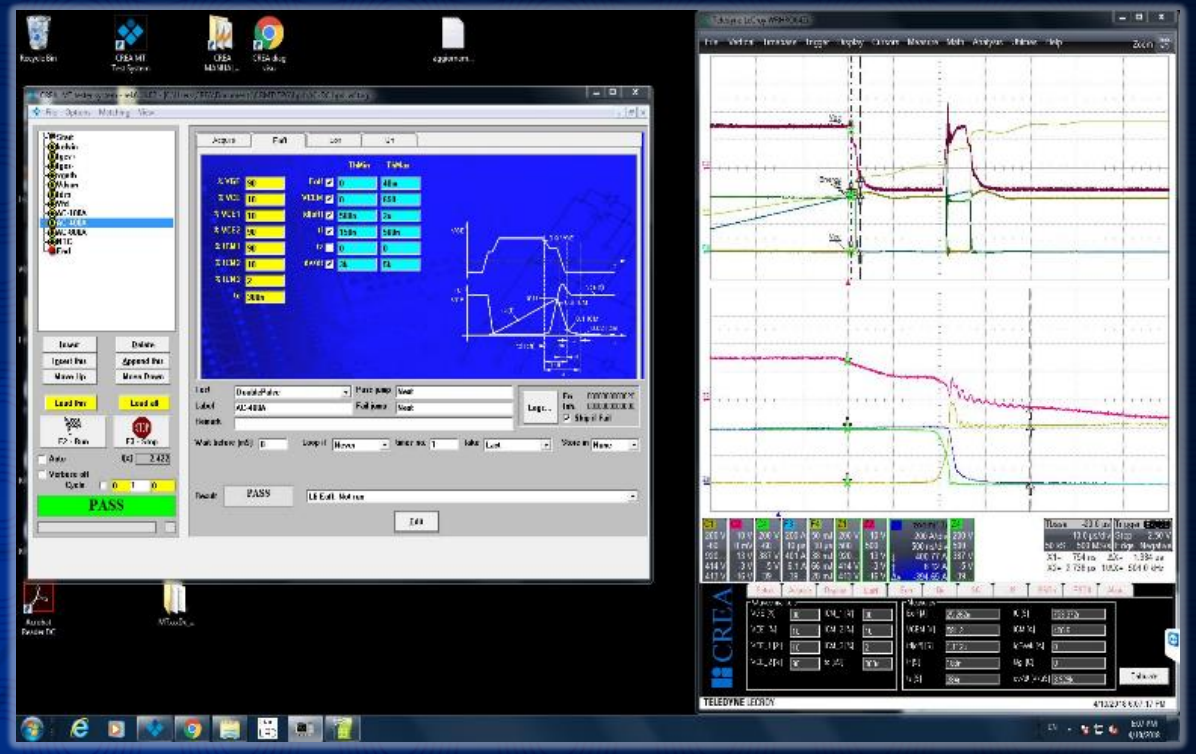


Probe card interface CR-PCI: the CREA solution to allow dynamic testing execution on chip with **low Ls** and without catastrophic effects in case of damaged device occurrence.

1st Annual SWTest Asia | Taiwan, October 18-19, 2018

CREA
SEMICONDUCTOR TEST EQUIPMENT

ATE Cabinet & Test Software



System Screen for AC Turn off measurement, 650V/400 A device

Power DYN generator **4500V/1000A**, max pulse time **1ms**

Floating gate drivers (up to **7KV**): **±30V**

Low output stray inductance design **(<50nH** at the sys bus bar)

Overcurrent protection fast circuitry to prevent system and accessories damage

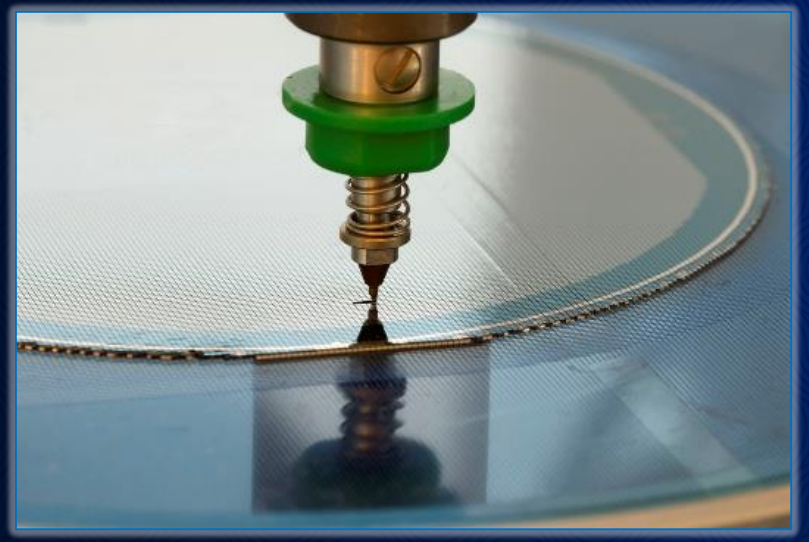
Handler interface: TTL, TCP/IP or GPIB

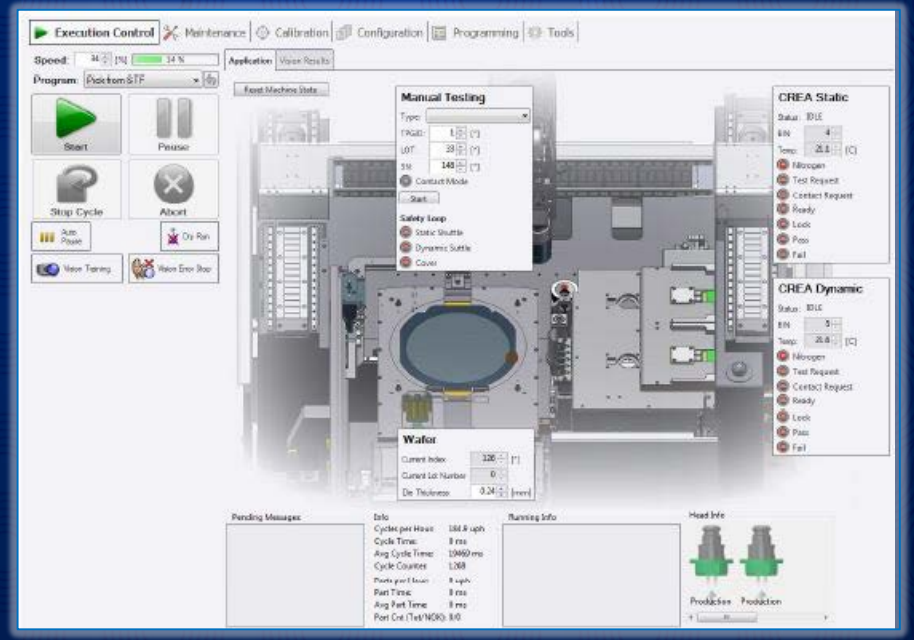
CREA SEMICONDUCTOR TEST EQUIPMENT

Handling the Chip...

- "Classical" KGD test: handling of diced wafer with **frame prober** - but this doesn't work here...
- High Current flow goes through backside of chip, this can't be supported by a film frame.

-> **dedicated chip handler** with contactor required here!





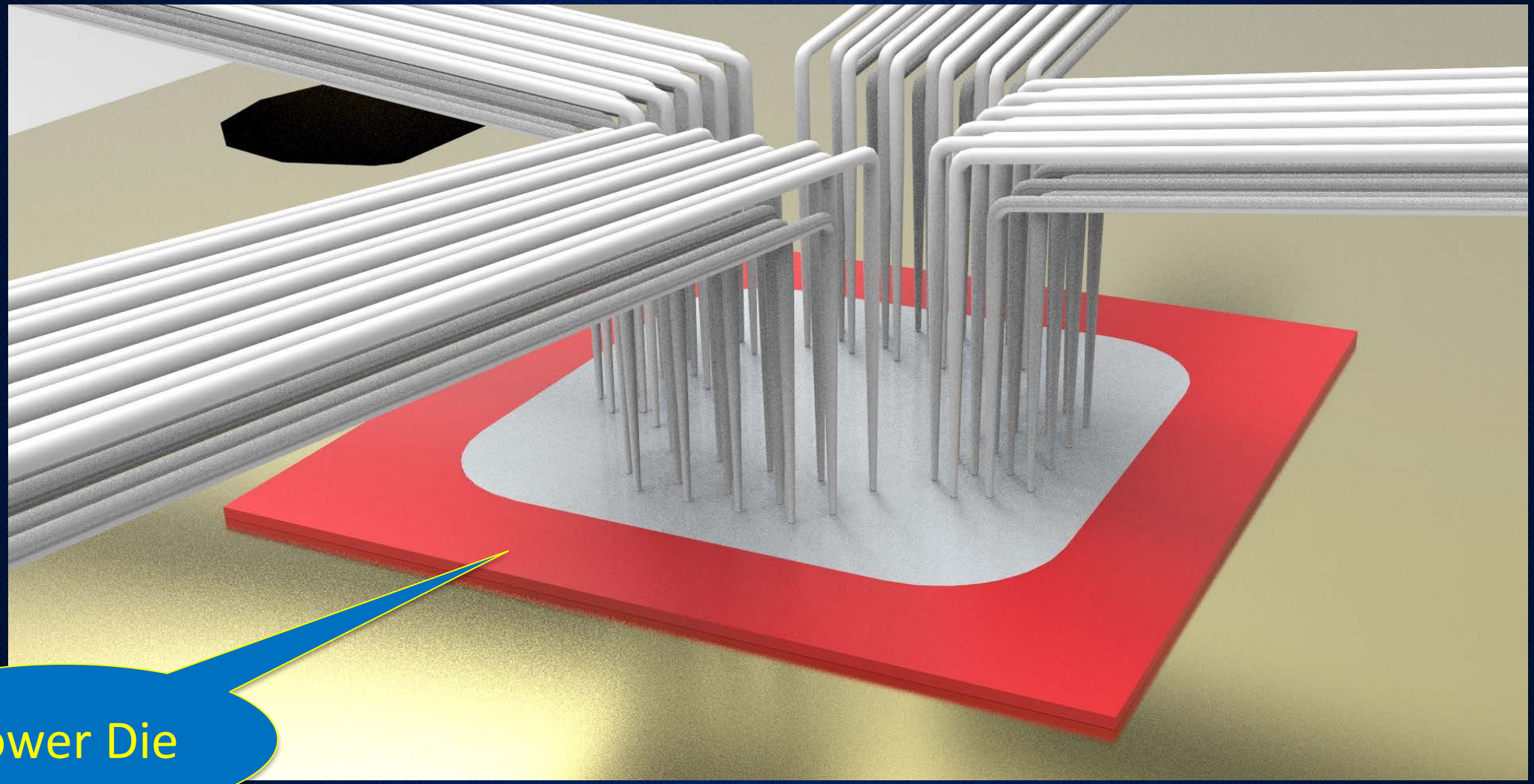
INFOTECH automation

"The Missing Link": Making Contact !

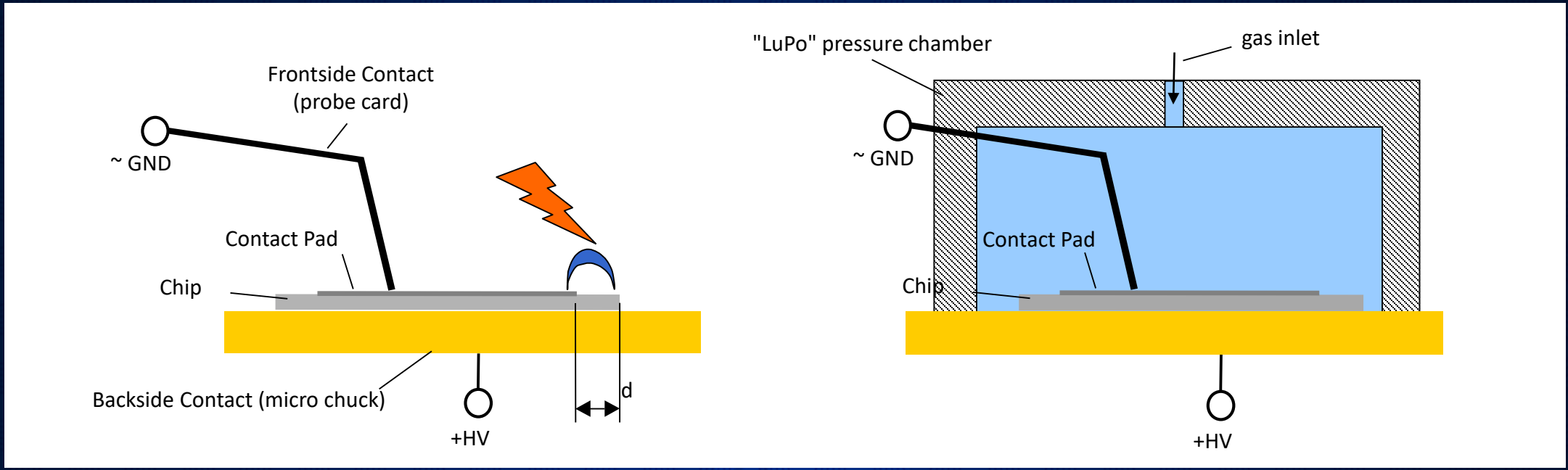
- Requirements for the KGD contactor:
  - High Voltage: up to **10 kV**
  - High Current: up to **1000 A**
  - High Temperature: up to **150 °C** test temperature
  - **Low Inductance solution** for dynamic test

Hmmmm...

Making Contact….



Contacting the Chip: High Voltage !

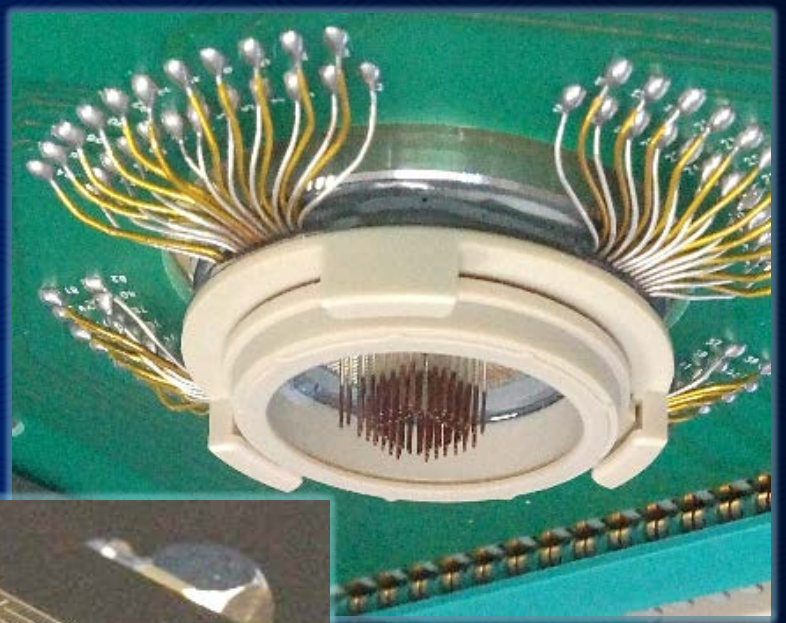


- **Bare chip:** electrical field strength across the "termination area" exceeds breakthrough field strength...
- ...and if tested at ambient atmosphere: **Arcing !**
- **"LuPo" pressure chamber** employed to create compressed air atmosphere making use of "Paschen Law" from gas discharge physics – **arcing suppressed!**

Contacting the Chip: High Current !

-> (Pulsed) Currents up to 1000+ A have to be transferred safely into and out of the chip

-> High Precision required for precise electrical test results (Kelvin force/sense contacts)



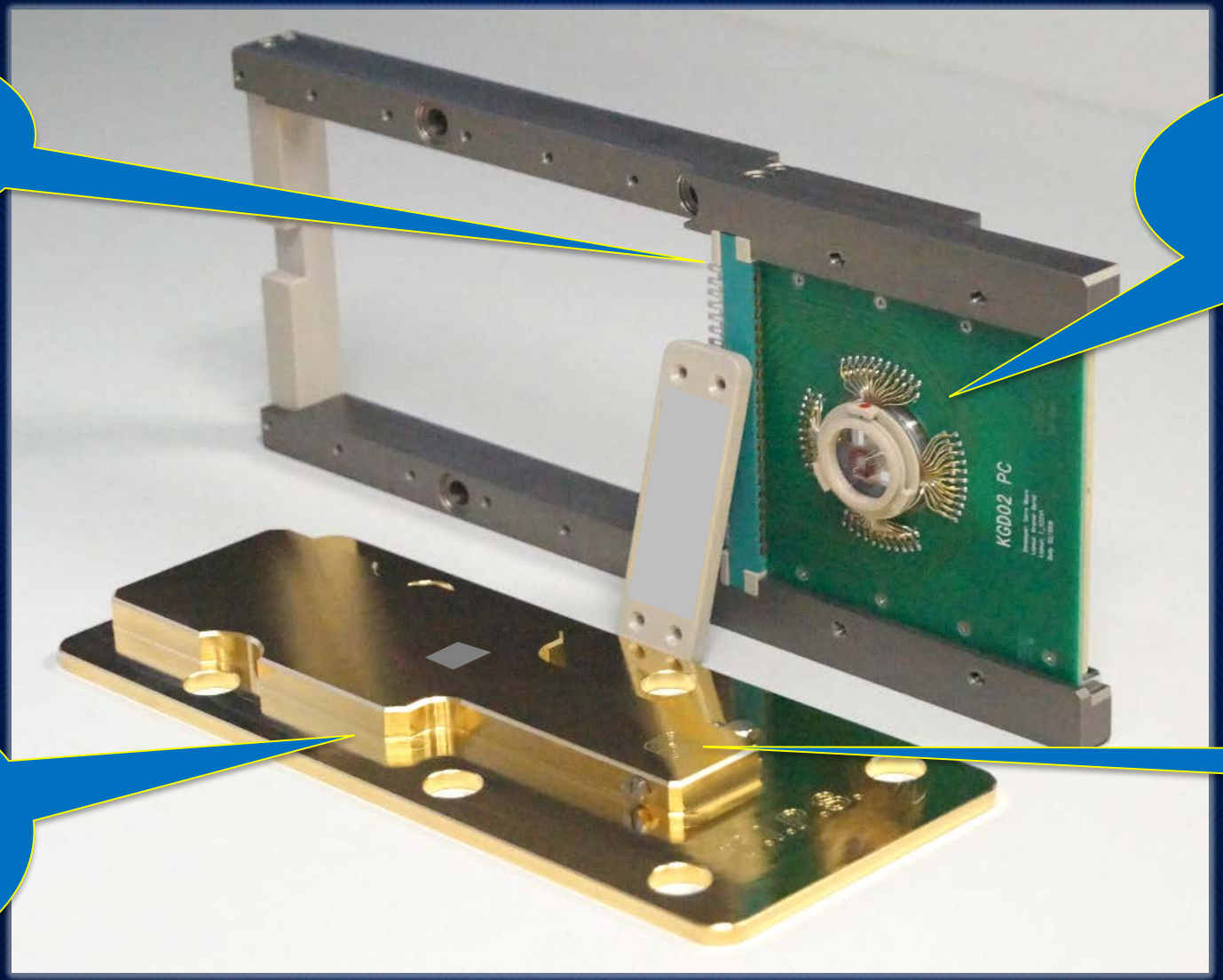
- Frontside Contact
  - Pogos? A nightmare on chip bond pads...
  - Test sockets: ?? handling fragile bare chips...

  -> **Probe Card**!
  - Well established performance for chip front side proven in wafer test.

- Backside Contact
  - fast chip transfer capability
  - very high current capability

  -> **Micro Chuck**!
  - vacuum chip handling
  - backside Kelvin sensing
  - high temperature capable

KGD Chip Contactor



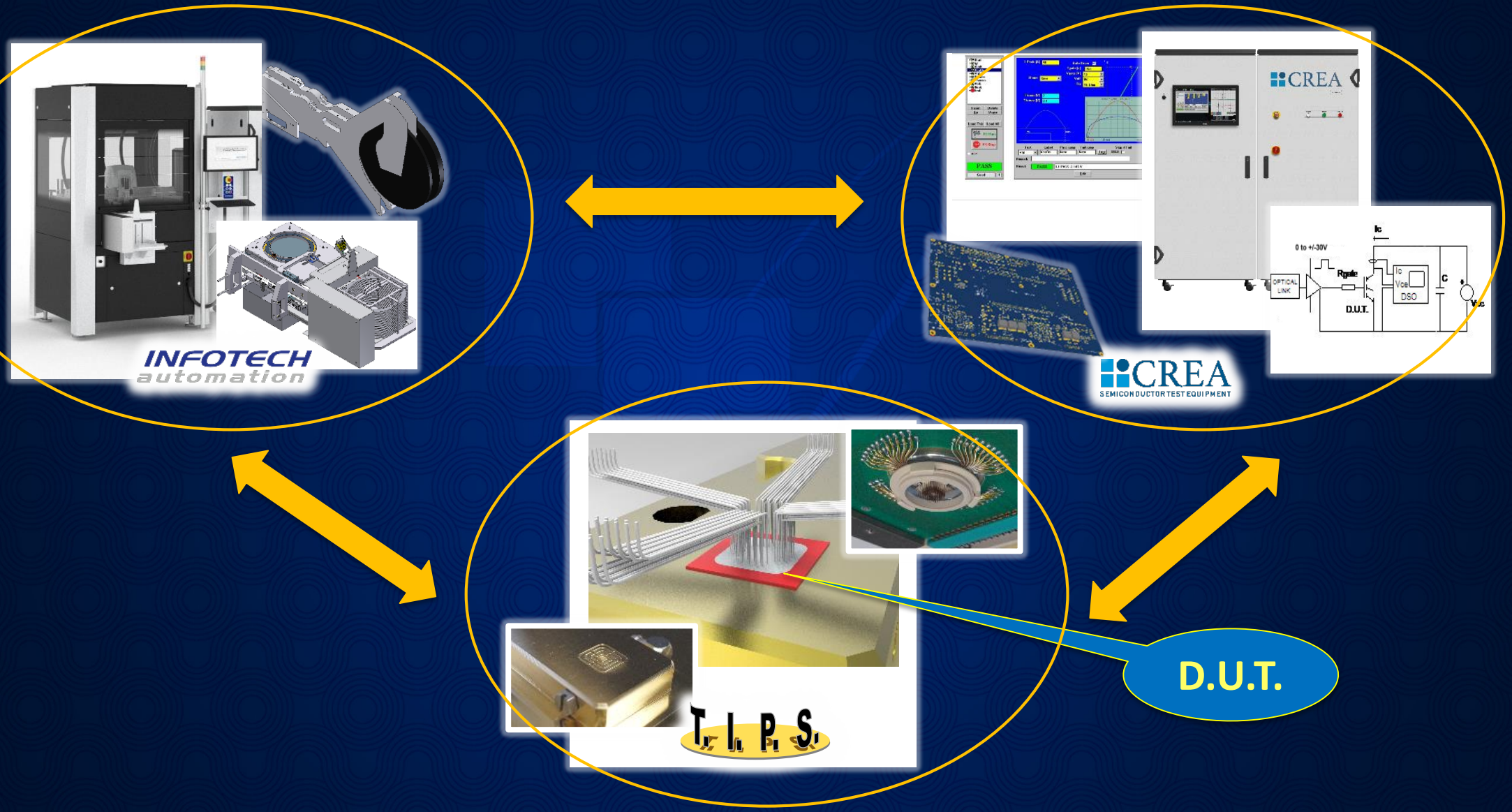
Probe Card holder, edge connector

"LuPo" Probe Card, low inductance design

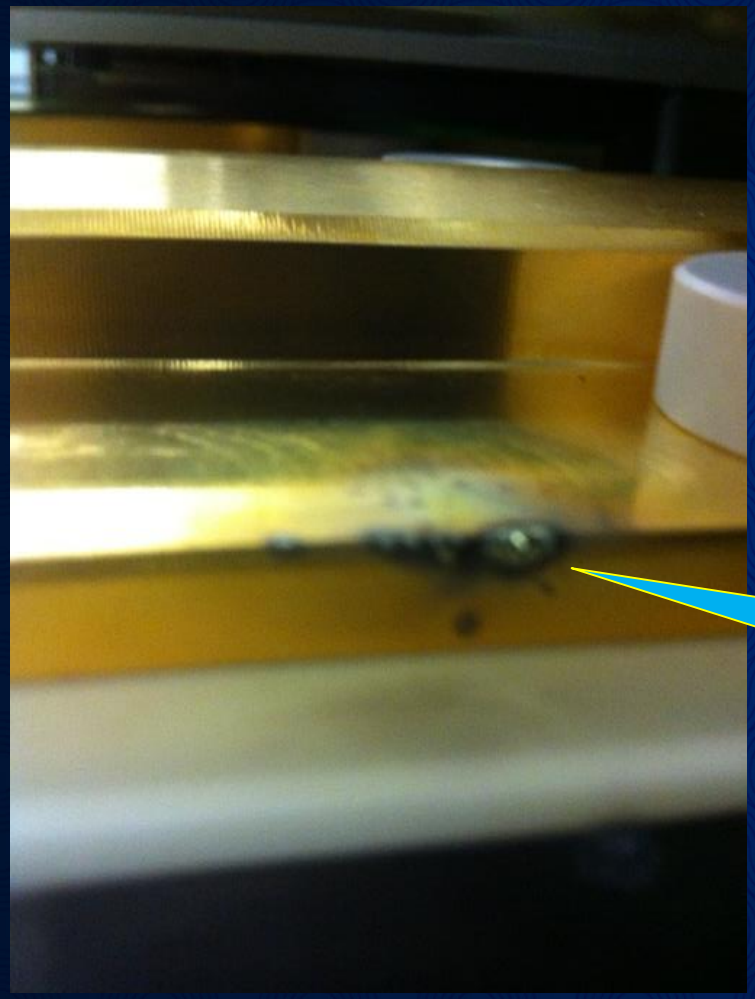
Micro Chuck, up to 10 kV, to be mounted on heater – 150 °C

Chip test location

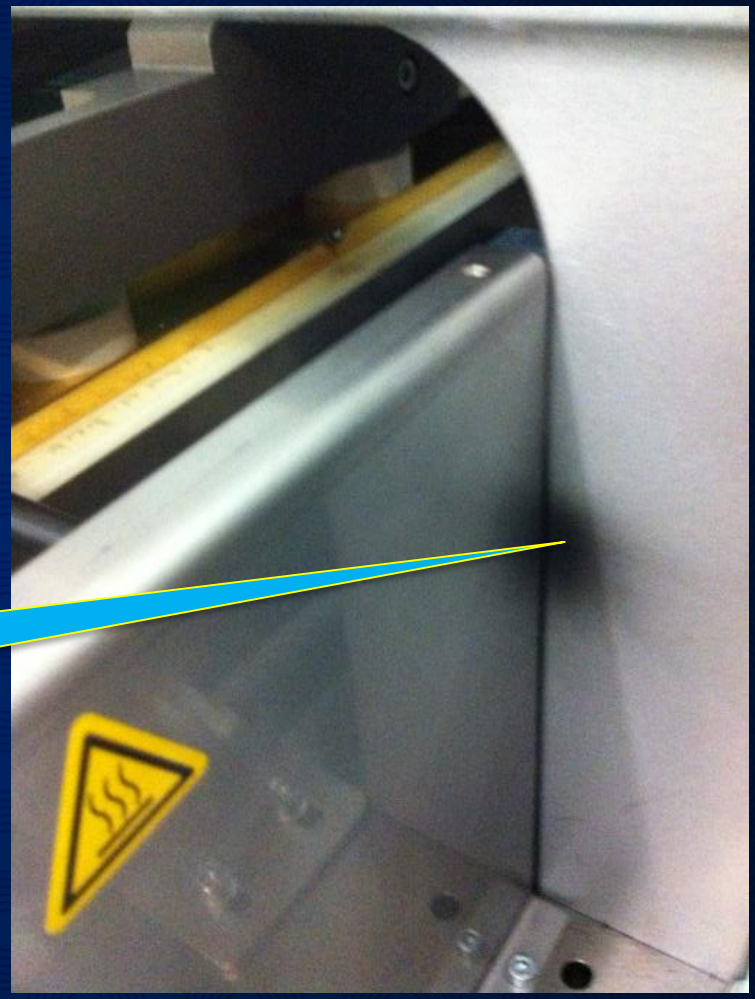
Integration into a System



Integration went smooth...



Arcing Burn Marks from insulation failure!



...mostly...

At the End: What does matter is the Result!

KGD > POWER < Test Cell

Summary

- KGD "Power" test shows its specific challenges from electrical, mechanical and physics point of view
- 3 individual companies - each deeply specialized in their field - have successfully created a turnkey solution
- end customer has been relieved of headaches for integration, finding the right sub-suppliers...
- State-of-the-Art "KGD Power Test Cell"
- "Limits of Test" – pushed a bit more forward...

Acknowledgements

- our staff at CREA, Infotech and T.I.P.S. Messtechnik
- a customer with confidence in a turnkey solution

THANK YOU!

A High-density Area-array Probe-unit with Non-discontinuous Fan-out Structure without Space Transformer using Monolithic Fabrication Method

Gunsei Kimoto
Takayuki Kakinuma
Masao Seimiya
ProbeAce Co.,Ltd.

Taiwan, October 18-19, 2018

Outline

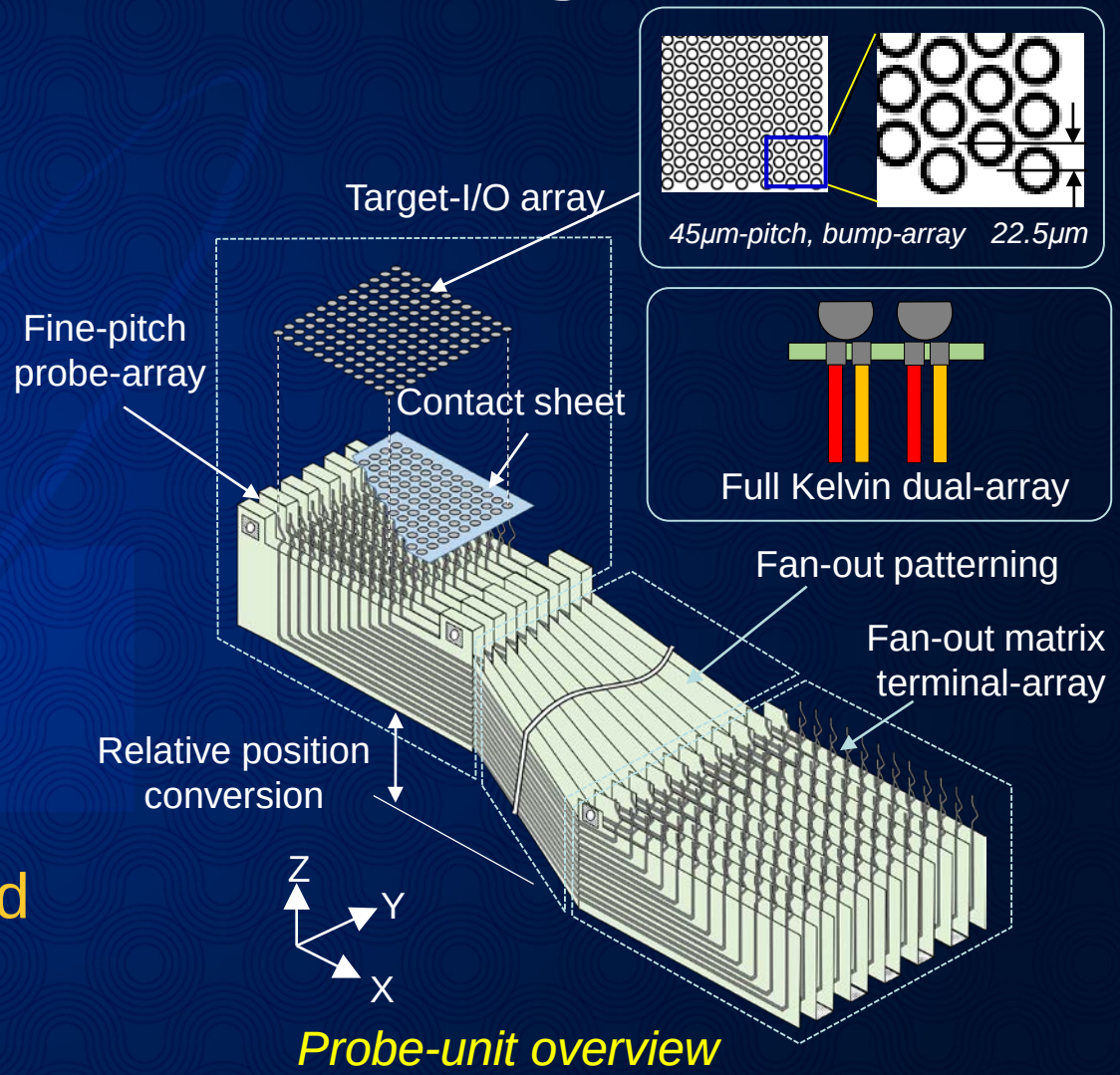
- Introduction
- Probe-unit design challenges
- Advantageous functions
- Comparison with current technology
- Monolithic fabrication method
- High-durability probing
- Results of Ni-electroforming Process
- Summary/Continuing challenges

Introduction

- **IC trend**
  - Shrinking die sizes with increasing I/O density, with the demand for higher performance
  - I/O configuration must be fine-pitch and area-array shape geometrically, both at the die and the advanced package level.
- **Probe card cost**
  - Increasing advanced probe card cost
  - Various kinds of probing technology type
  - High cost factor of high-precision assembling, high-layer substrates
- **Our work so far**
  - AMMECS® (Advanced Micro-Mechanical･Electrical･Chemical System) method has been introduced at SWTW2013, 2014.

Probe-unit Design Challenges

- Higher density area-array probing
  - 45 μm-pitch 5K-bumps: 22.5 μm-pitch in staggered
  - Full-Kelvin probing: half-pitch dual-array per bump
  - 10K-pins Kelvin probe-array demonstrated
  - Scalability for 50K-bump class
- Non-discontinuous fan-out structure
  - Probe-to-terminal direct patterning
- Extremely cost-effectiveness
  - Monolithic Fabrication Method
- Higher durability probing
  - Non-scrub probing with contact-pad-sheet
- Easy connection and installation on a board
  - Fan-out terminal matrix of 0.5 mm-pitch
  - Flexible relative position conversion



Probe-unit overview

Advantageous Four Functions of the Probe-unit

1. Densification:

- Fine-pitch probe-array was formed for contacting target high I/O density.
- Both for device and package test

2. Fan-out:

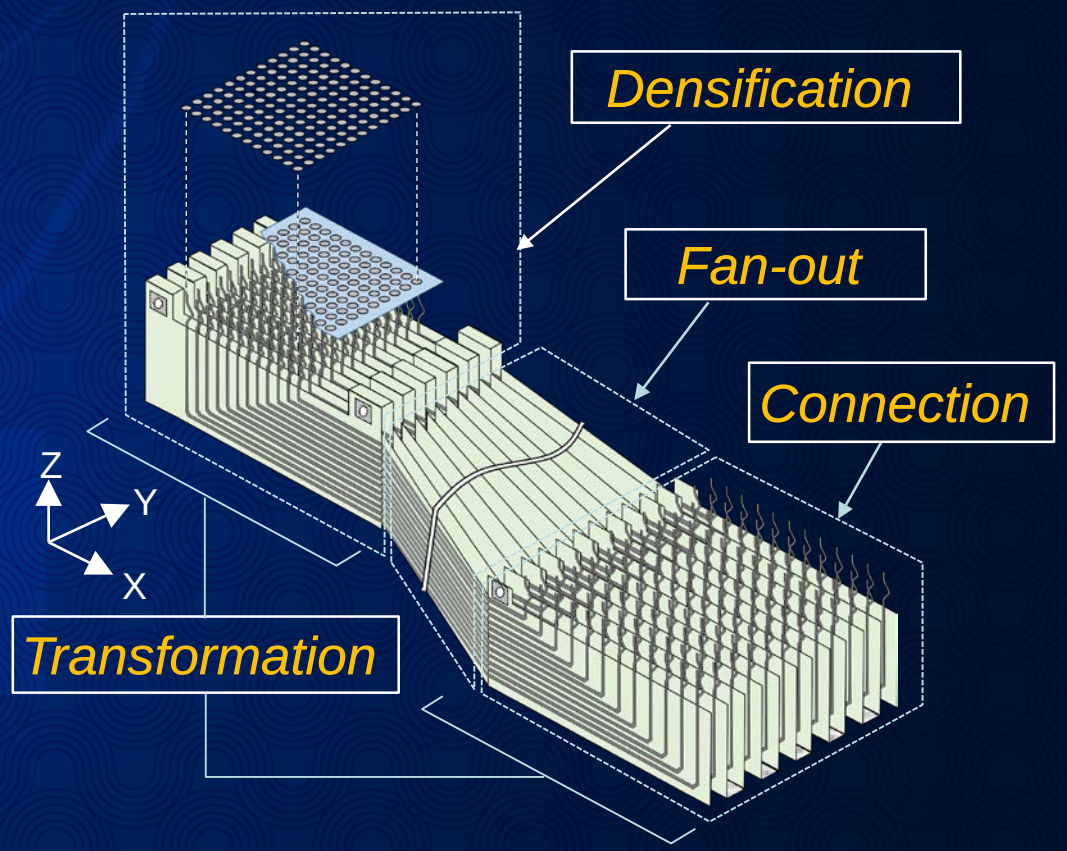
- Fan-out patterns were seamlessly continued from probe to optional test/monitor area.
- Without any space-transformers or interposers

3. Connection:

- A fan-out matrix terminal-array was formed for contacting test/monitor terminals.
- Also consists of spring contact pins.

4. Transformation:

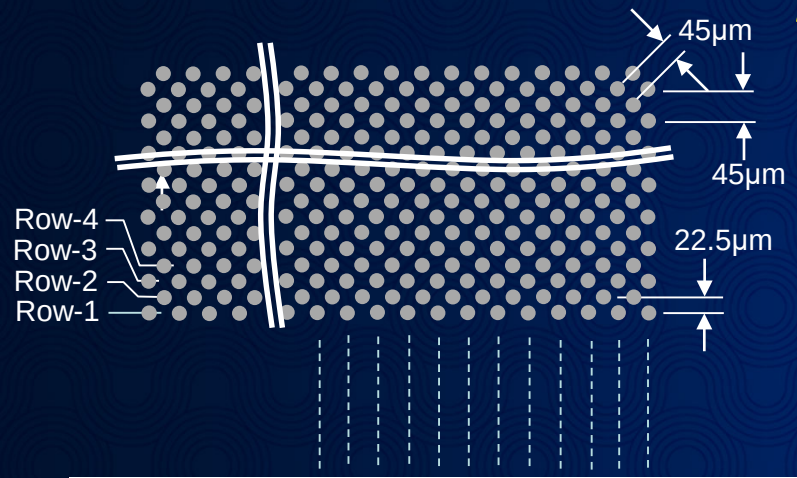
- Relative position conversion between a probe-array and fan-out matrix terminal-array
- Enabling flexible placement on a board or test-system



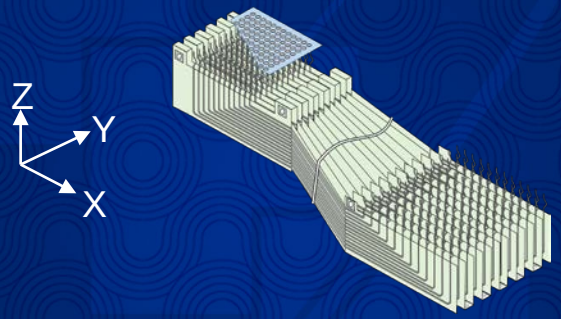
Probe-unit overview

Basic Probe-unit Design Concept

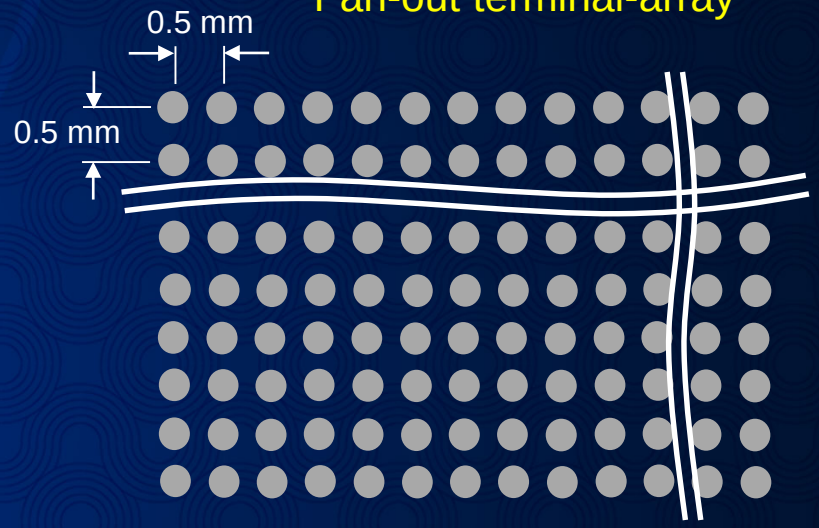
Fine-pitch bump-array

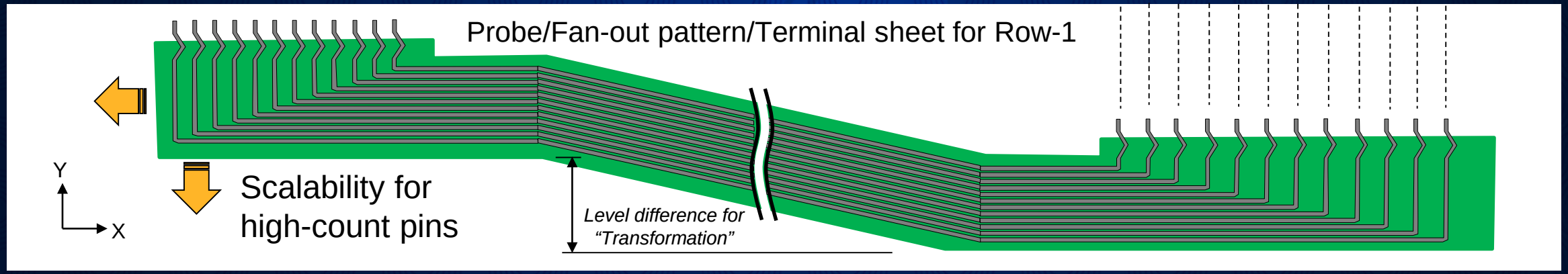


Single component from fine-pitch area to fan-out area with "scalability"

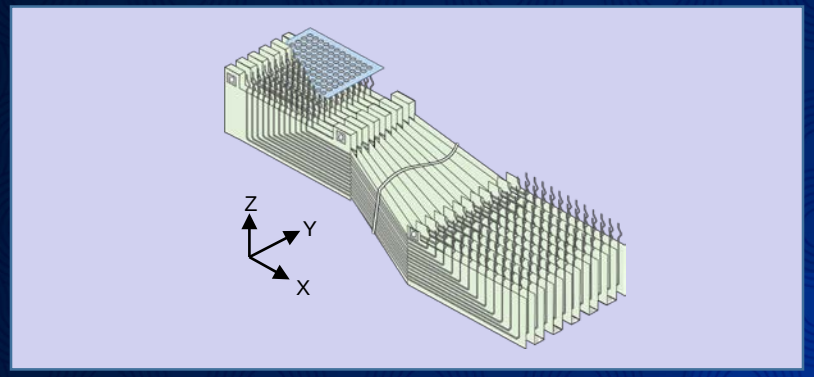
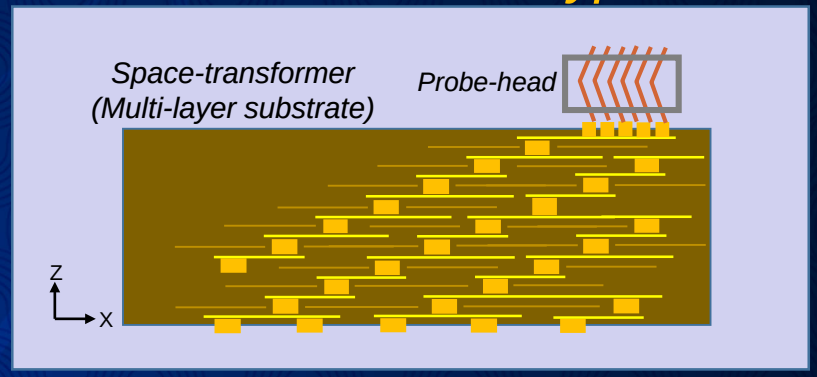


Fan-out terminal-array

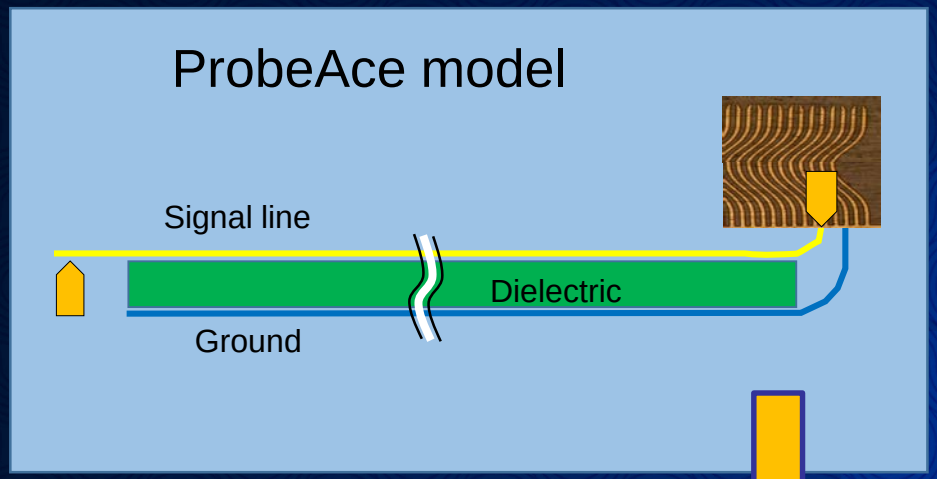


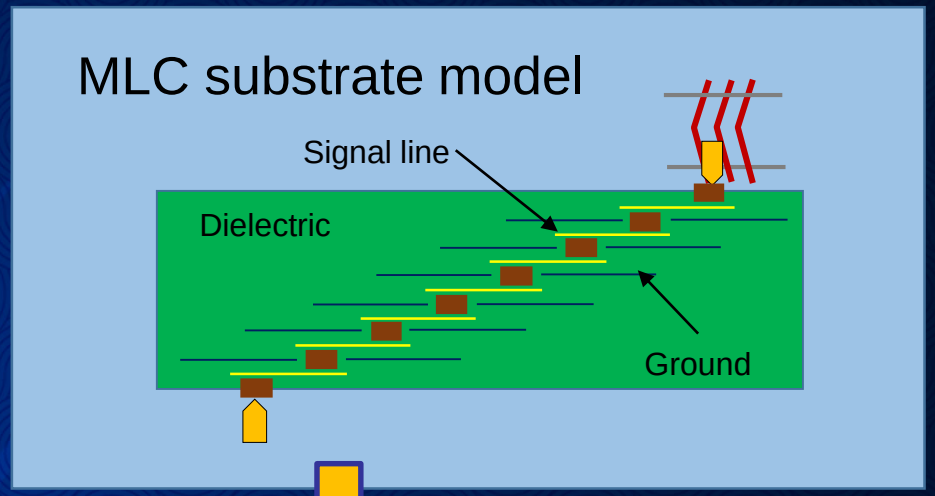


Comparison with Current Technology

ProbeAce Probe-unit	*MEMS Vertical Type*
	
Cost-effectiveness ● Single component from fine-pitch to fan-out area ● The same process of main functions; probes, patterns, contact-sheet, positioning parts, etc. ● Higher pin-count and finer pitch scalability	● One-pin, one-part ● High-precision skilled assembly ● High-cost multi-layer substrates
Mechanical performance ● Freeing from manual assembly	● High-precision skilled assembly
Electrical performance ● Non-discontinuous signal path	● Many discontinuous signal path

Comparison for Impedance Continuity

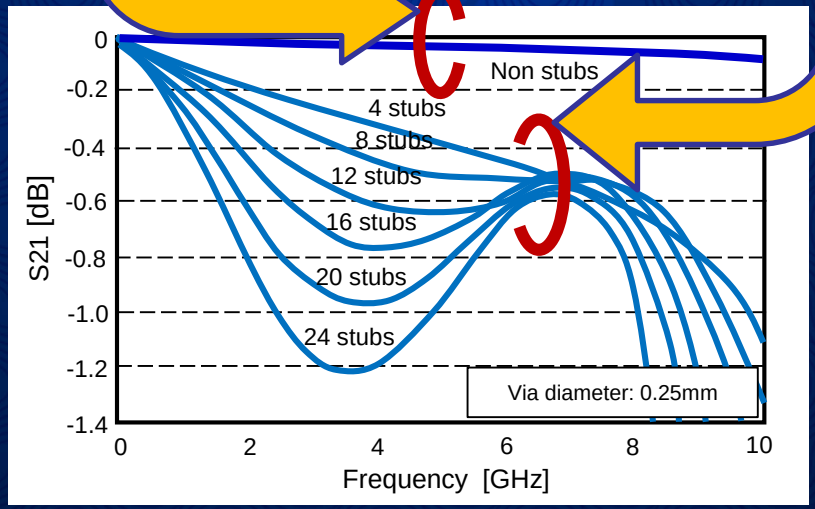




- Non-discontinuous micro-strip-line model from probe to terminal

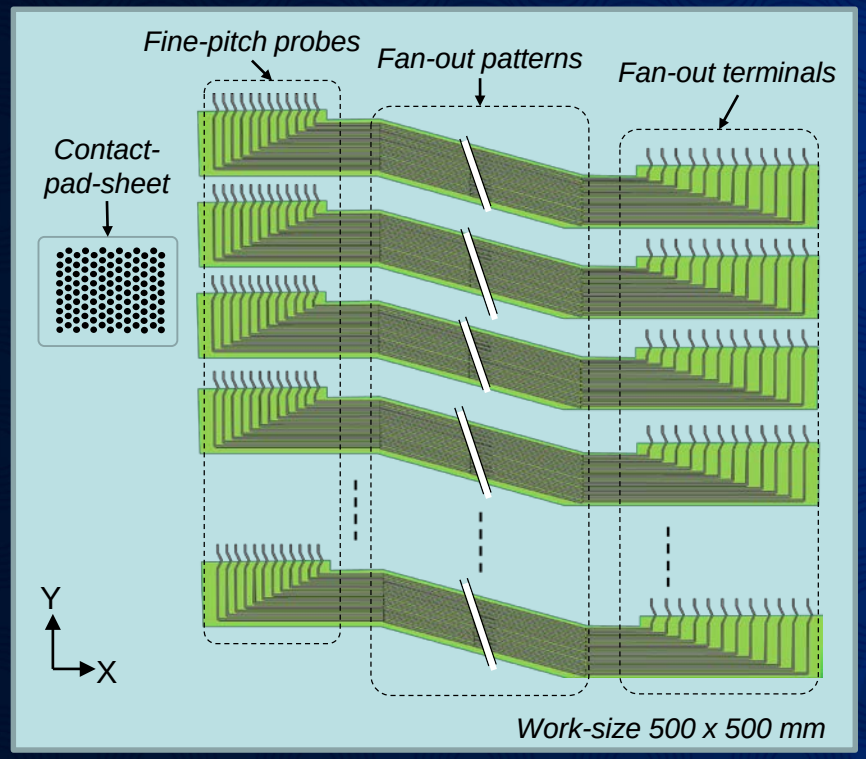
- Many discontinuous signal path in a high-layer substrate

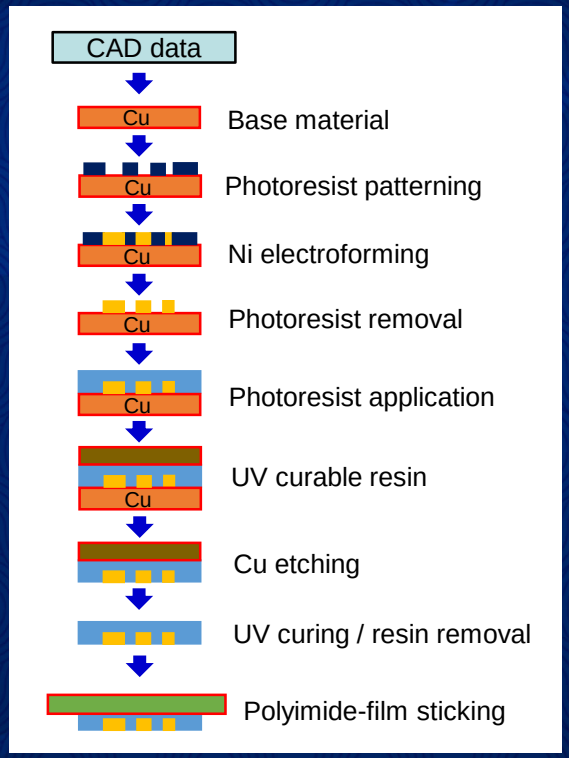
Insertion loss simulation depending on via-holes (stubs) number



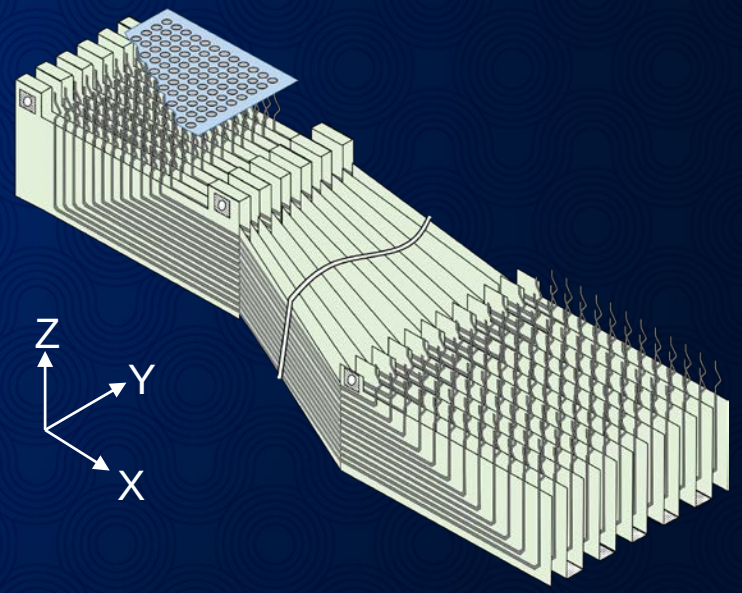
Monolithic Fabrication Method

- **Major functions were created from a single work material.**





The final assembly shape was formed by folding and cutting.



Two-dimensional design and fabrication stage

Three-dimensional assembly stage

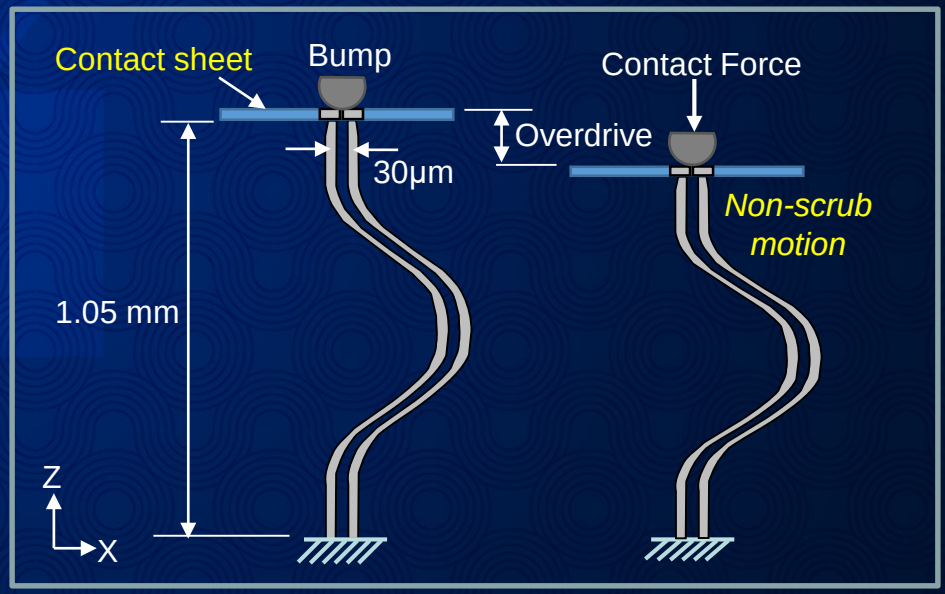
Monolithic Fabrication Method

- **Design step:**
  - Entire patterns of probes, patterns, terminal-probes, contact-pad-sheet, and insulating film shapes were designed on a single X-Y coordinate plane.
  - Every coordinate data were managed as an interrelated in a common coordinate.
- **1st-fabrication stage; Electroforming (e.f.) process**
  - All patterns were formed by electroforming of “Nickel aminosulfonate” two-dimensionally.
  - X-directional pin-accuracy was basically established in this stage.
- **2nd-fabrication stage; Assembly process**
  - The final assembly shape was formed by folding like “Origami” (paper-folding) and cutting.
  - Freeing from high-precision assembly process, by Y-directional positioning patterns.
  - Massive probes and fan-out patterns were manufactured significantly cheaper and faster.

Solution for High-durability Probing

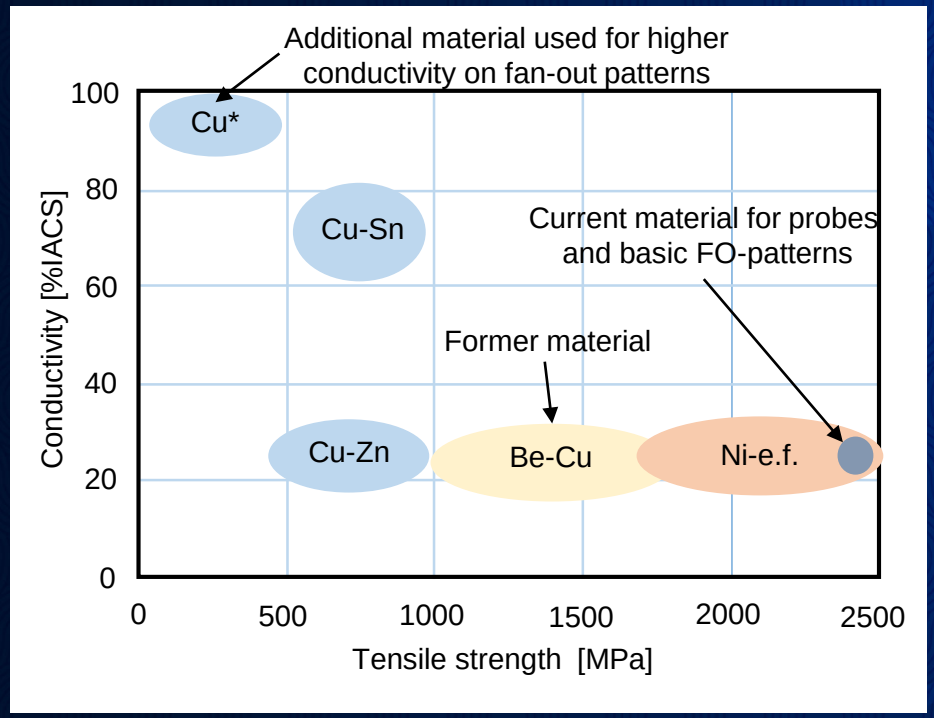
- **Requirements for high-durability probing**
  - High yield-strength material
  - Probing design in the elastic region
  - Minimizing wear of probe material and pad/bump material for preventing contamination

- **PA basic probe design concept**
  - *"Non-scrub"* motion probe design
  - Probing with *"Contact-sheet"*

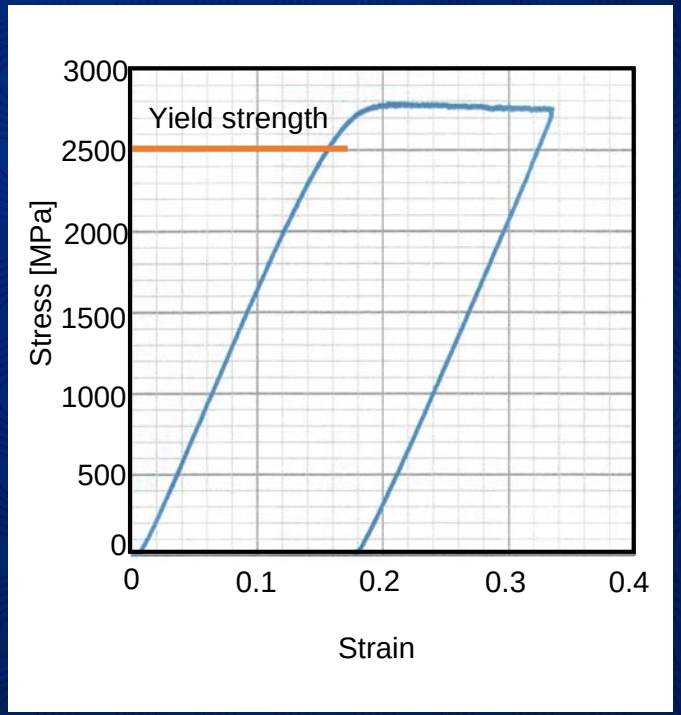


High Yield-strength Material

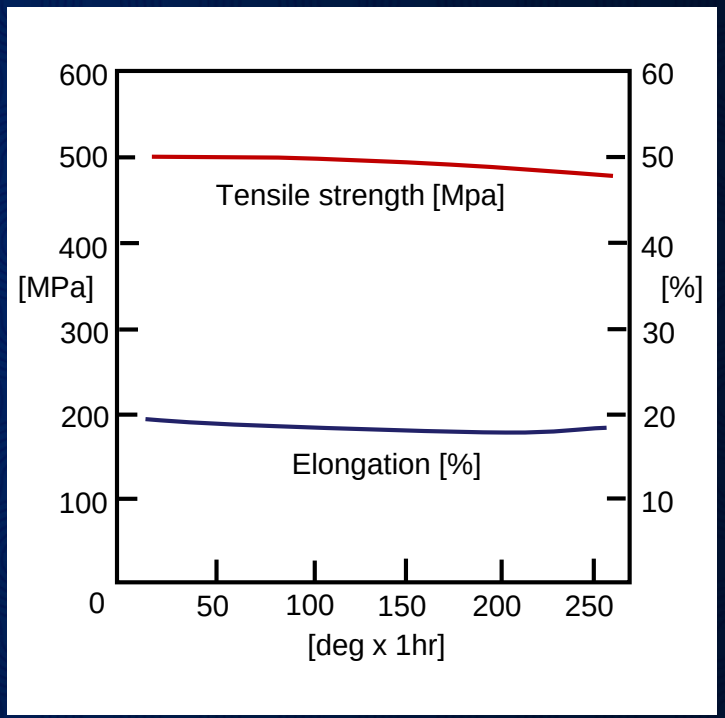
- **Newly developed Ni-aminosulfonate for electroforming**
- **High-yield-strength and high-temperature-stability**



Relation between Tensile-strength and Conductivity



Stress-Strain Curve



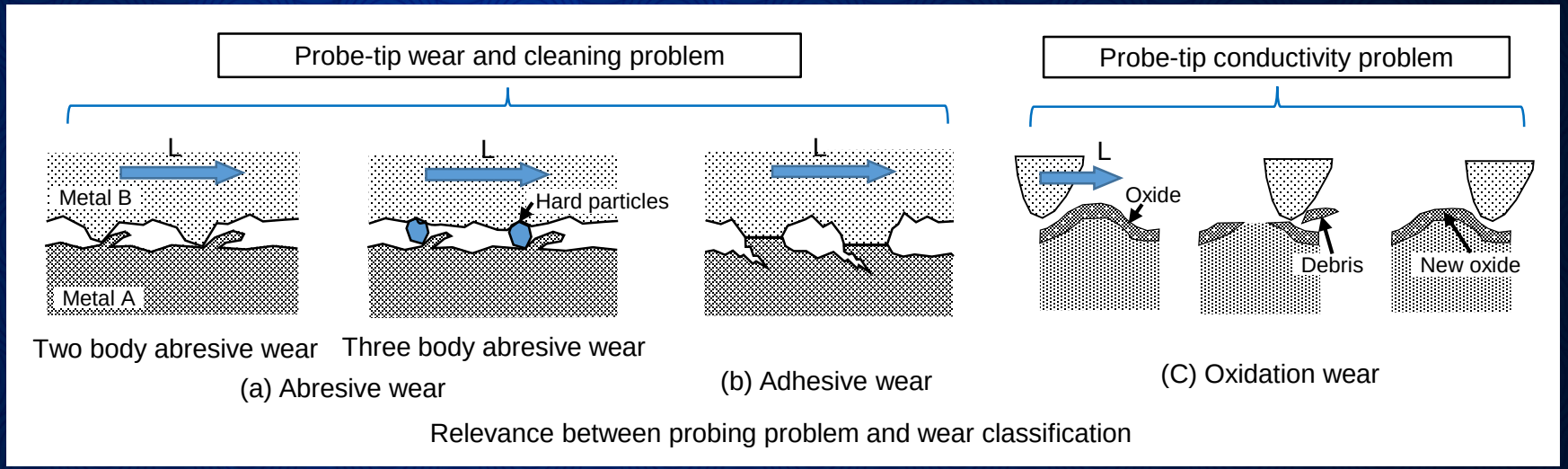
Characteristics of general sample Ni-e.f. material at high temperature

Probing and Wear Mechanism Method

- **Probing action can be generally associated with well-known wear mechanism method.**
  - Abrasive wear is the most frequently encountered wear mechanisms in conventional probing.
  - Oxidation wear is induced by frictional heating, including the contact-resistance problem.

$$V = k \cdot L \cdot Ar$$

V: wear volume,
L: sliding distance,
Ar: real contact area
k: wear coefficient;
reflected by particle shapes (or asperities), sliding speed, etc.



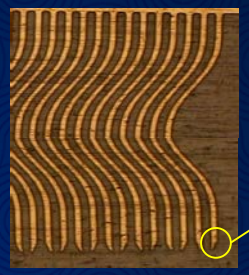
- ***Sliding distance (Non-scrub): L=0 → Wear volume: V=0***

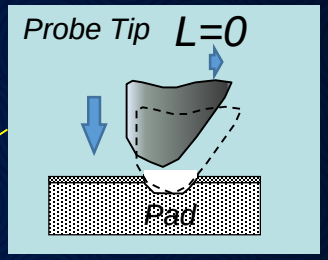
Non-scrub Probing Design

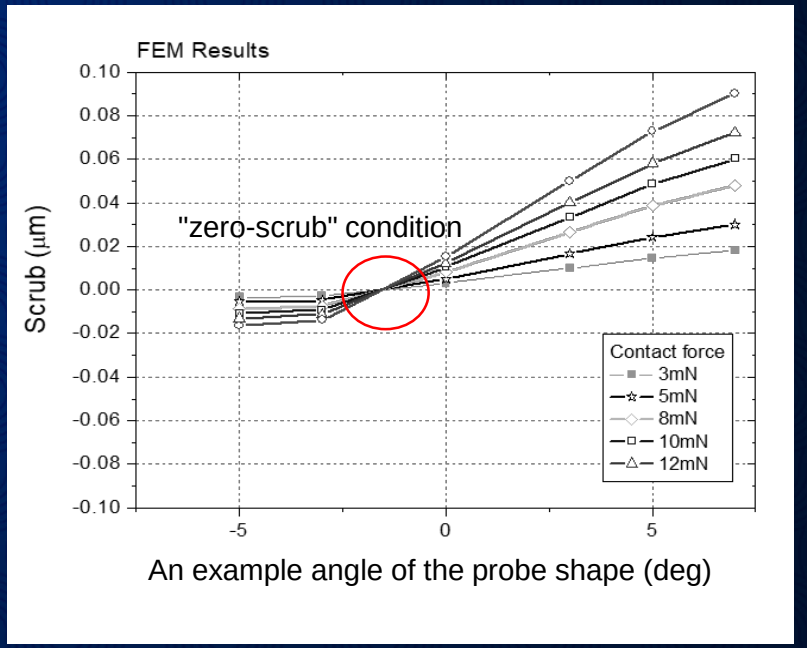
- **Non-scrub probing (sliding distance: L=0) as a solution of:**
  - Minimizing wear of probe material for maintaining the contact shape
  - Minimizing wear of pad material for preventing the contamination
  - Ensuring the conductivity by penetrating the oxide film

- **FEM results of a probe shape parameter to decide "zero-scrub (L=0)" motion:**
  - Optimizing probe contact shape with no dependence on the contact force

$V=k \cdot L \cdot Ar$

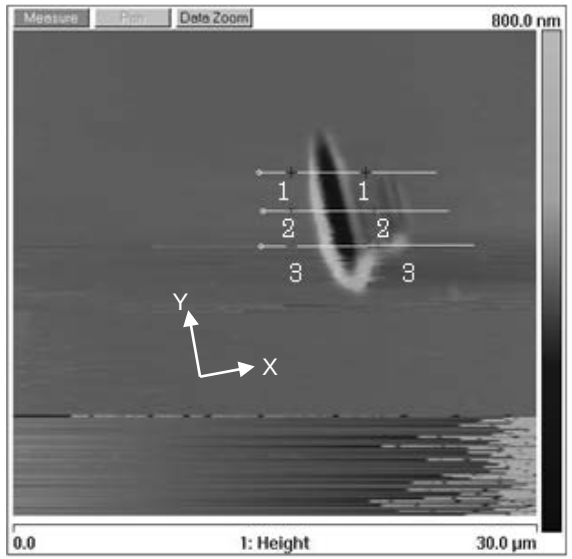




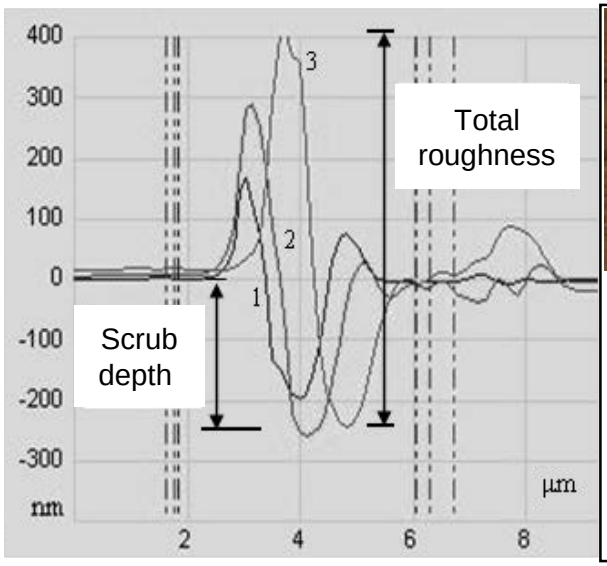


Non-scrub Probing Design

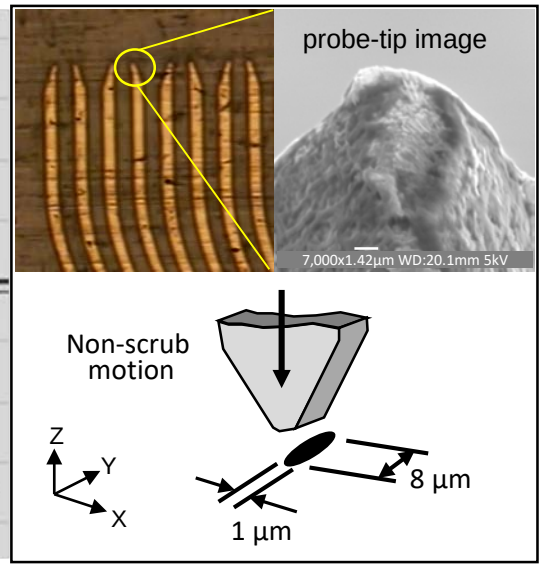
- **Non-scrub design probe motion indicates the minimum probe mark without X-directional sliding.**
- **Scrub depth of 250 nm is good enough to break through the oxide coating of 10 nm-order.**



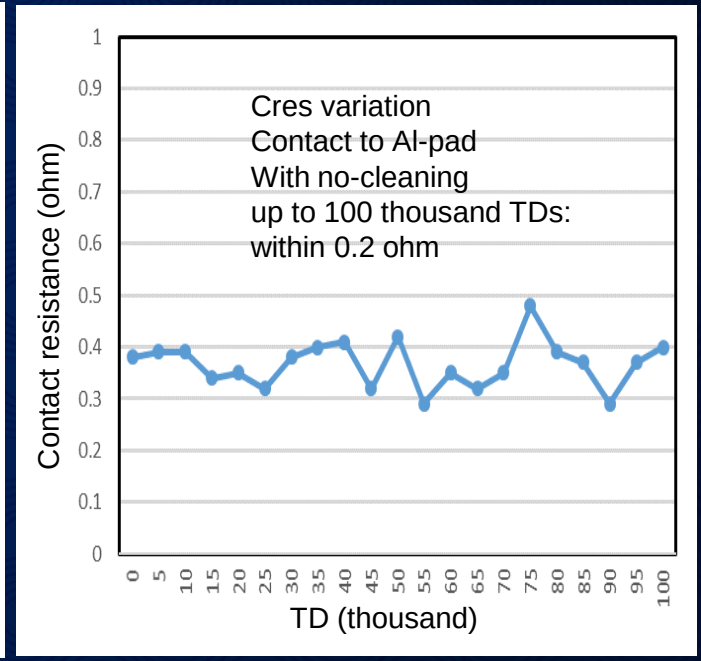
Deformation at F=10mN



Scrub depth measurement



Relation between probe-tip shape and deformation

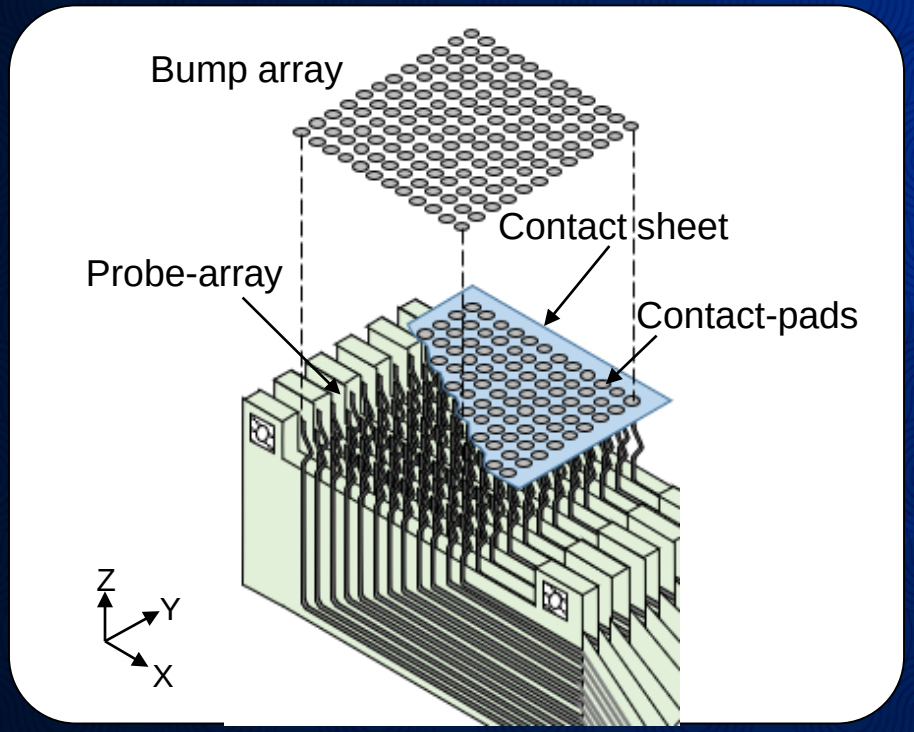


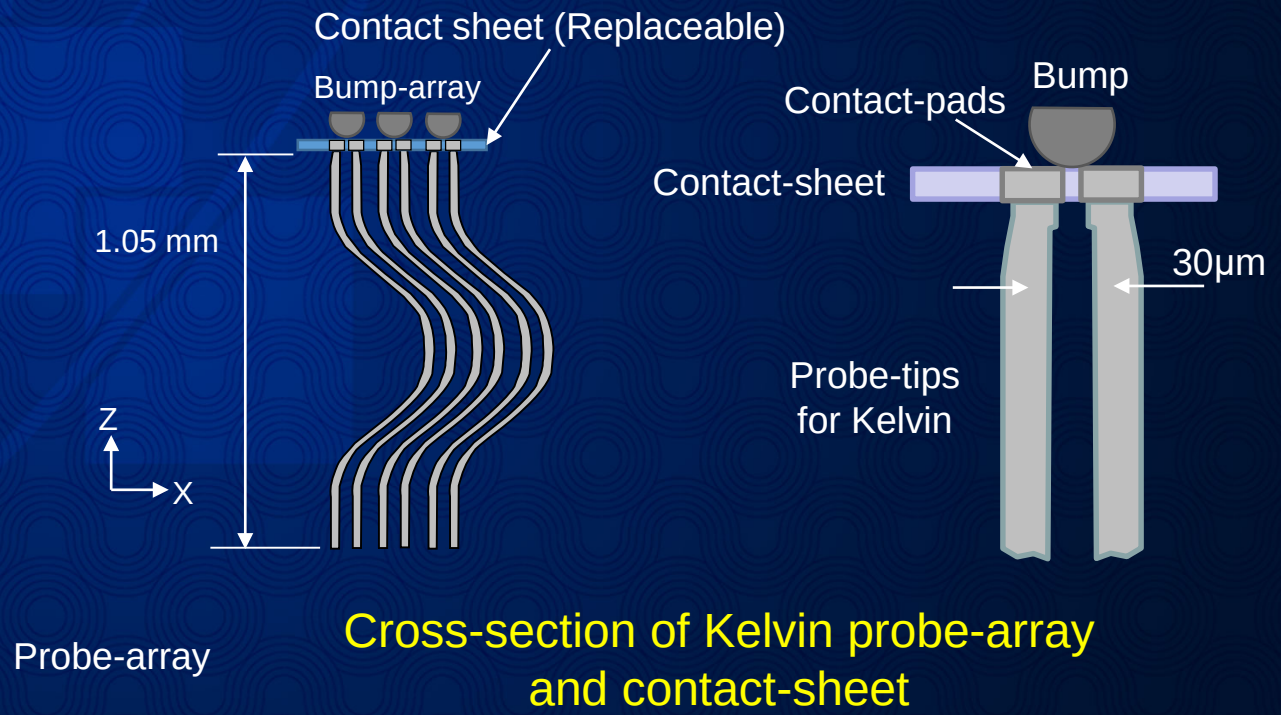
Probe mark of the non-scrub design probe at contact force of 10 mN

Non-cleaning 100 thousand TD

Probing with Contact-sheet

- **“Contact-sheet (contact pad-array sheet)” was fabricated in the same Ni-e.f. process and assembled with covering all tips of probe-array.**
- **Precision Ni-e.f process ensures XY-accuracy for bump-array.**
- **Contact-sheet is replaceable for “cleaning.”**

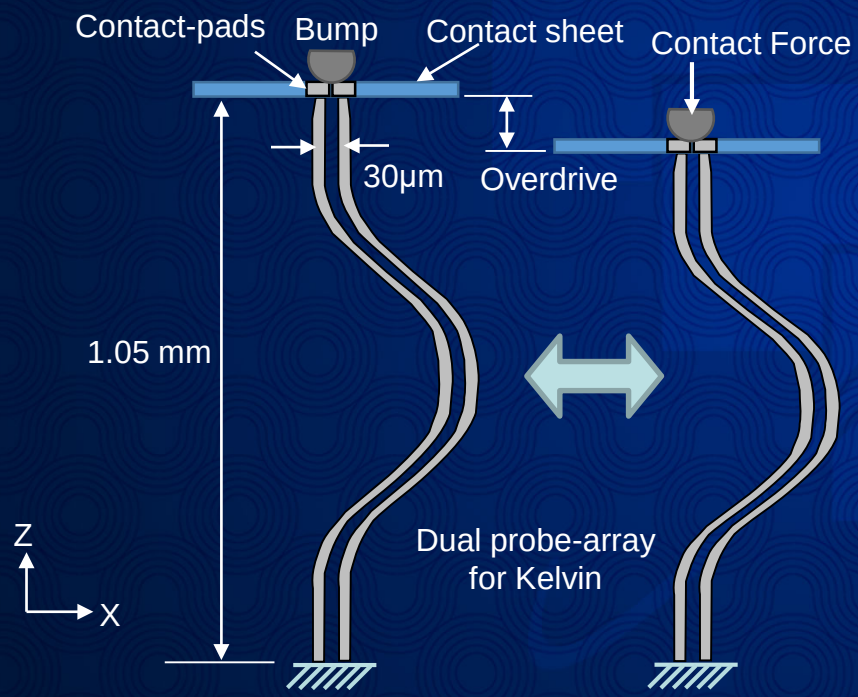




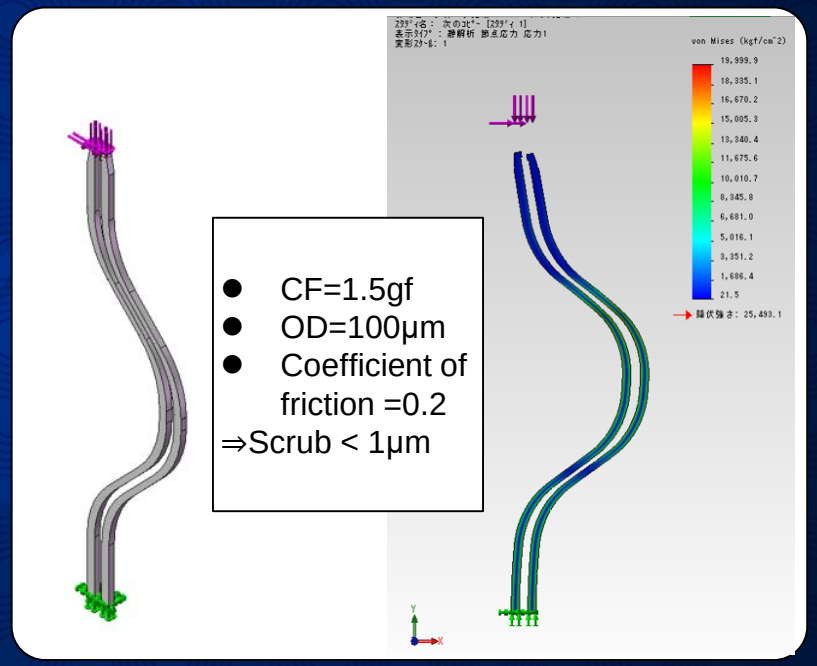
Cross-section of Kelvin probe-array and contact-sheet

Probing with Contact-sheet

- **"Probe-tip" and "Contact-sheet" move together by *XY-friction* at touchdown.**



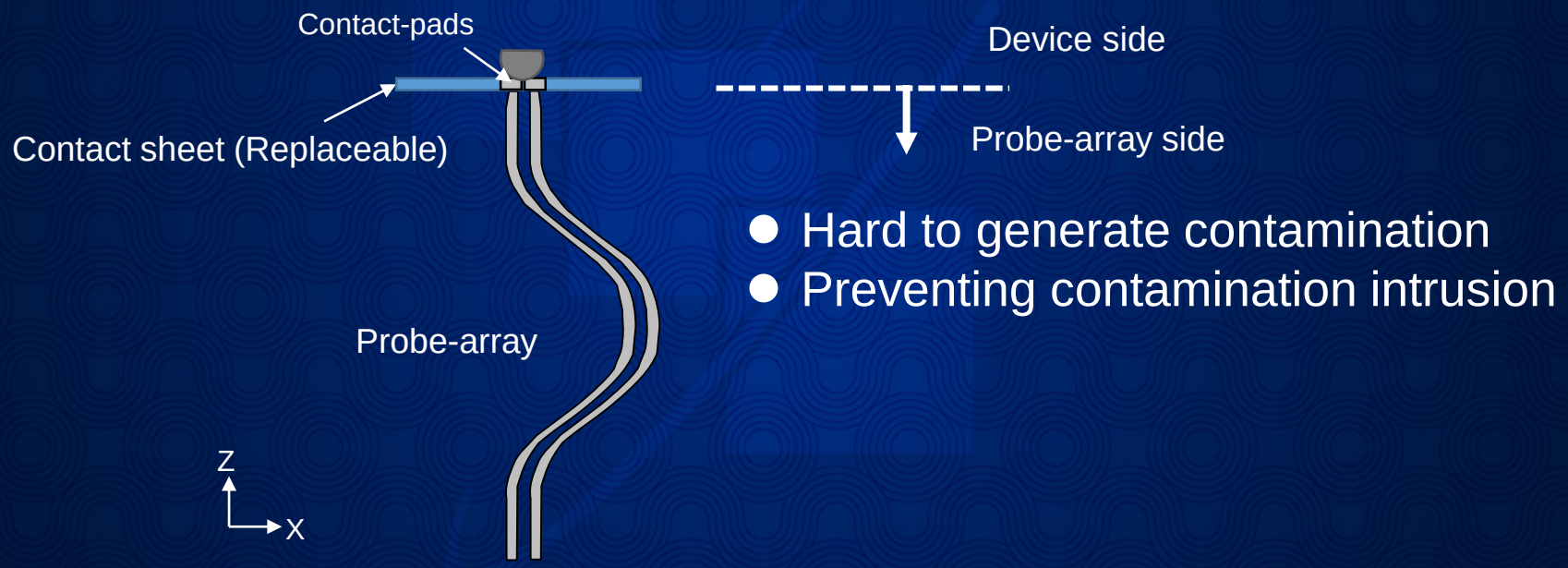
Touchdown motion



CF/OD/Scrub simulation with COF

Effective of Probing with Contact-sheet

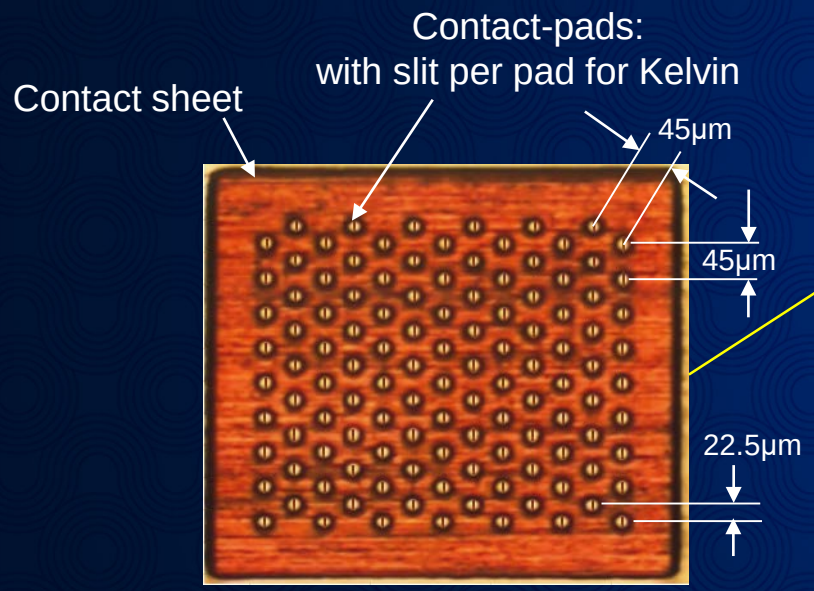
- **Hard to generate contamination by contacting non-scrub probe-tip with contact-pad of the same material**
- **Preventing contamination intrusion from device side**



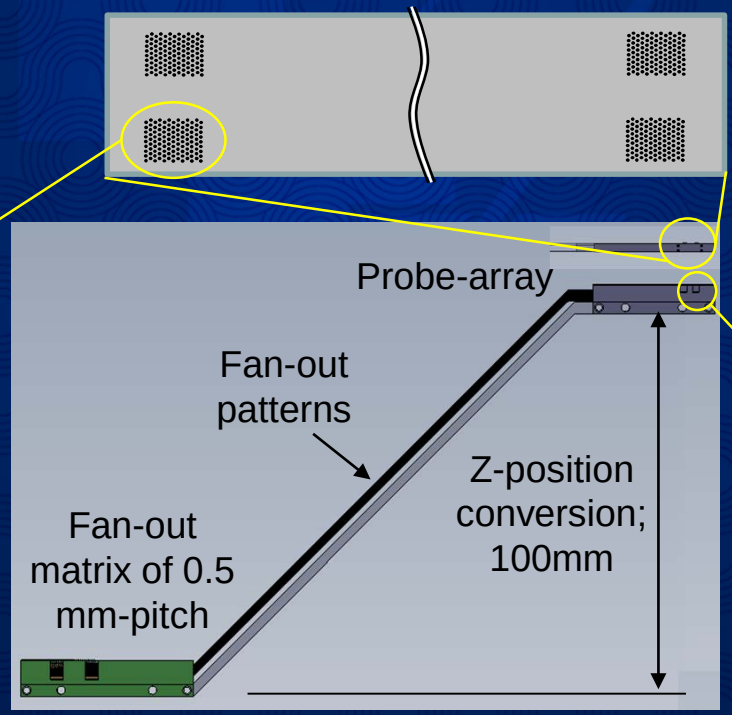
Cross-section of probe-array and contact-sheet

Results of Ni-e.f. Process

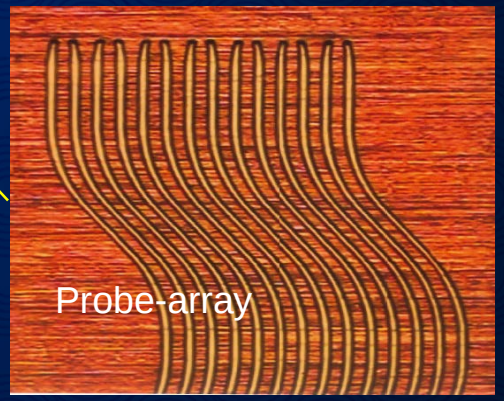
- **Probe-unit of Kelvin contact for 45 µm-pitch, 5000-bumps**
- **Probe and patterning accuracy: less than 2 µm**



Contact-pad-sheet for selected 117-pins

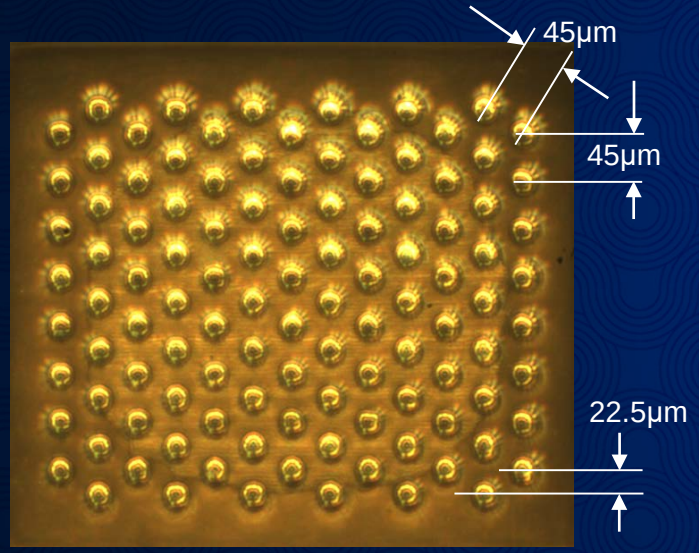


Dual Probe-tips for Kelvin

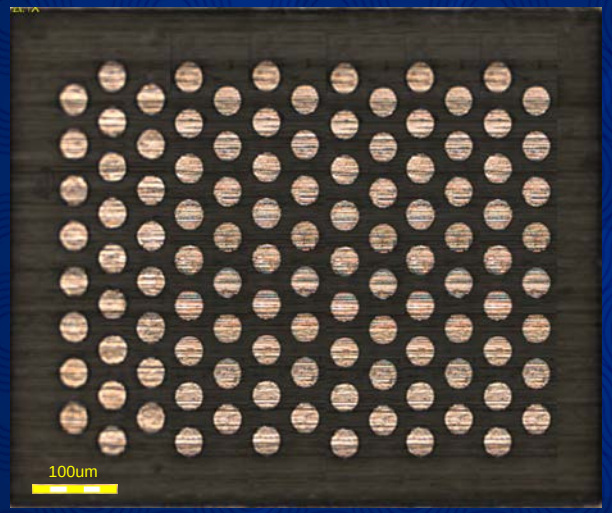


Results of Ni-e.f. Process

- **Pad-array in the contact-pad-sheet**
- **Contact-pad with slit for Kelvin contact**

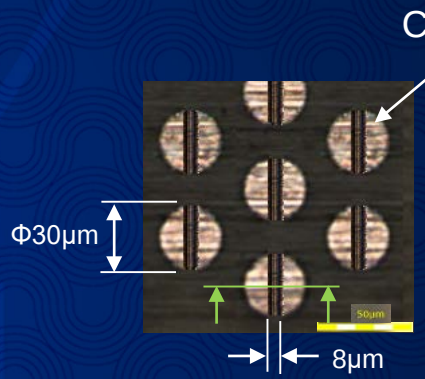


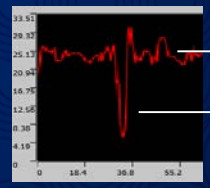
Bump contact side



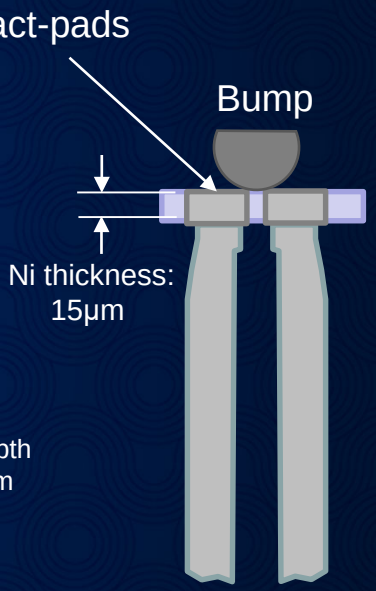
Probe contact side

Pad-array in the contact-pad-sheet





Cross-sectional profile



Probe-tips for Kelvin

Contact-pad
with slit per pad for Kelvin

Summary and Continuing challenges

- **Achievement of Probe-unit design and manufacturing method characterized by:**
  - Densification; finer pitch and higher pin-count scalability
  - Non-discontinuous fan-out, easy connection and installation
  - Cost-effective structure and manufacturing
  - Higher durability probing
- **Demonstration of Probe-unit for 45 µm-pitch bump Kelvin contact**
  - Fine-pitch of 22.5 µm-pitch, 10K-pin for Kelvin contact
  - Probe and pattern Ni-e.f. accuracy: less than 2 µm
  - Contact-pad with slit for Kelvin contact
- **Continuing challenges**
  - Connectivity and Durability test