TCAM | BCAM

eFlexCAM Custom Embedded CAM Compilers

Unlike pre-defined, packaged component products, silicon-proven eFlexCAM custom CAM compilers let you choose and compile features that fit your design's unique needs to optimize power, performance or area. Available from 14/16nm to 180nm, our CAM compilers are customized to meet IDM and leading foundry processes.

When flexibility is everything, eFlexCAM compilers deliver up to 75-percent power reduction, no LPM-related table management, and auto-pruning for reduced table size. eFlexCAM simply keeps it small, fast and low power.

When Flexibility is Everything

As the demand for digital content explodes, so does the demand for network speed. This has driven the need for processing packets at wire speed.

Memory processing tends to be the bottleneck in network performance. If memory cannot keep up with increasingly fast processors, the processors have to wait, stalling the system. Specialty memories address the problem in a variety of ways. Ternary content-addressable memories (TCAMs) are unique — they search an entire memory database in one cycle. eSilicon's 14/16nm TCAMs can provide up to 2.5 billion search results in one second (BSPS).

Silicon-Proven eFlexCAM from 14/16nm to 180nm

eSilicon has delivered embedded TCAMs to networking customers since 2000, helping them meet the demand for wire-speed packet processing, access control lists and other requirements of high-bandwidth delivery.

eSilicon offers a broad range of silicon-proven, feature-rich, high-performance, high-density eFlex™ embedded CAM compilers. Our eFlexCAM™ compilers provide high-efficiency, cost-effective solutions for applications such as network search engines, cache for network processors, QoS services, classifications, Ethernet, ATM switches and other diverse networking applications. Silicon-proven search speeds for the 14/16nm TCAM exceed 1.2 BSPS under worst case operating conditions, and up to 2.5 BSPS under typical operating conditions.

In addition to a full set of standard features, our eFlexCAM compilers provide a comprehensive set of user-selectable features that are chosen at compile time. You can choose just the features that you need for a specific application to optimize power, performance or area (PPA).

eFlexCAM designs are available in 14/16nm to 180nm geometries, customized to meet challenging PPA requirements of IDM and leading foundry processes. We can supply CAM instances or compilers to fit the number of instances required.

Standard Features

- Binary (BCAM), ternary (TCAM), and mixed-mode architectures
- 14nm, 16nm, 28nm, 40nm, 65nm, 90nm, 130nm and 180nm
- Flexible selection of width and depth
- Up to 160Kb compiled, 1Mb cascading table size
- Up to 160 bits per word
- Easily cascadable to increase search depth without degradation in performance
- Single-cycle Compare operation
- Smart Power Management
- Fast cycle and access time: the 14/16nm TCAM delivers 1.2 BSPS worst case and up to 2.5 BSPS under typical conditions
- Valid-bit, global and local valid-bit reset
- Flexible masking (bit/group/global)
- Match Flag, Direct Hit Line Out
- Hand-crafted layout for high density and performance

User-Selectable Features

eFlexCAM compilers include many user-selectable features, such as:

- Priority encoder
- Redundancy
- Bit-write

Product Highlights

Flexibility

In contrast to pre-defined, packaged component CAM products, eSilicon's eFlexCAM compiler lets you choose and

compile the features you need to meet your design's specific requirements. This effective integration method, combined with full-custom, pitch-matched floor-planning and layout for each basic cell, results in a highly compact embedded CAM.

Efficient Power Management

Smart Power Management (SPM) architecture allows you to reduce power consumption by up to 75 percent for low-power applications. In the search operation, simply select a single table in Multi-Table Partition (MTP) mode, or a vertical segmented block of the CAM array in Multi-Width Search (MWS) mode. The remaining unselected portions of the CAM array will not be activated during the search operation to save power.

The four-quadrant architecture allows you to turn on only one quadrant at a time for searching, reducing peak current significantly. A low-power version of eFlexCAM employs a sense amplifier to reduce voltage swing of the Hitline and further reduce power required for search operations.

Longest Prefix Match Architecture: Requires No Table Management

As table size grows, table management becomes an issue when sorting entries for standard Longest Prefix Match (LPM) implementations. eFlexCAM LPM architecture eliminates table management associated with LPM. No sorting of entries is required when updating tables. Entries can be inserted at any location in the CAM array. Our LPM technique saves area through the removal of the Priority Encoder circuitry for Match Address operation.

Auto-Pruning to Reduce Table Size

Auto-Pruning is an additional option of the eFlexCAM compiler that allows the collapsing of entries with the same specific attribute, such as entries that have the same rule in a QoS table or the same Next Hop address. This option is implemented and executed during Write without the need for additional user control. Auto-Pruning can reduce the size requirement of a table by up to 30 percent as well as result in significant power savings during searching.

Features

Learning (LRN)

Learning is used to Write MISS data into the CAM array at the Next Available Address. LRN can be used for Write-Back functionality in cache applications.

Aging (AGN)

The Aging option allows the user to reset a Valid Bit (VB) of an entry that has not been hit for a pre-determined period of time, to reserve room in the CAM array for new entries. Aging Refresh (ARFS) control signal is used to reset the VB of all entries that have not been hit.

Multi-Width Search Modes (MWS)

eFlexCAM compilers support the option of multiple-width search mode. You can select from four different search modes: quarter-word (QW), half-word (HW), single-word (SW) and double-word (DW).

Easily Cascadable

For array efficiency and easy expansion of width and depth, cascading circuits are built in to avoid additional glue logic for building larger blocks.

Auto-Update (AUU)

AUU supports updating the CAM array without the need to provide an address. When selected, data on the DI bus will be automatically written into the CAM array at the Next Available Address (AVAL).

Next-Match Mode (NEXTM)

The Next-Match Mode feature allows you to sequentially get Match Addresses (MADR) of all entries that were HIT (Multiple-Hit) during a Compare operation. Matches are provided in order of decreasing priority at subsequent clock cycles.

Multi-Table Partition with Addressable Tag Bits (MTP)

MTP allows you to partition the CAM array into several tables with variable depths using additional tag-bits for table selection. The depth of each table is your choice, as long as each table has the same value for tag-bits. You can select single-table search to save power, or perform full searches across all tables simultaneously.

Look-Aside RAM Buffers (LARB)

With LARB, a RAM block with the same depth as the CAM array and variable width (user's choice) will be attached to the CAM instance for area optimization. This option is useful in cache applications, combined with the Write-Back (learning) option.

Dual-Port Search (DPS)

Dual-Port Search allows users to perform two searches in one clock cycle. For this special option, each CAM cell will have two hit lines and two Compare data-in signals.

Bidirectional I/O Option

If simultaneous Write and Read are not required, the user can select the bidirectional I/O option to combine Data-In and Data-Out buses. While the standard eFlexCAM configuration allows Write and Compare operations to occur during the same clock cycle, users who do not need this functionality can also combine the Write and Compare data buses to reduce the pin count.

Web Access and Download

All eSilicon IP is available in Navigator, our online IP exploration tool, at **https://star.esilicon.com**. Navigator provides access to eSilicon's full portfolio of IP products. Memory instances may be generated, analyzed and downloaded. Power, performance, and area (PPA) data is pre-loaded for easy data comparison and analysis.

Broad EDA Support

eSilicon memory compilers provide EDA views for leading EDA vendors, helping to ensure seamless integration of our embedded memories into your design flow.

Contact

Please contact us at **ipbu@esilicon.com** for more information, silicon quality results, white papers or data sheets, or visit Navigator at https://star.esilicon.com.

Other eFlex Custom Memories Offered by eSilicon

Types of Memory

- Single-port SRAM
- Dual-port SRAM
- Pseudo 2-Port SRAM
- One-port register file
- Two-port register file
- Cache memories
- ROM
- Asynchronous register file
- Four- to 12-port multi-port register files (MPRF)

Architectures

- High density
- Ultra-high speed
- Ultra-low power

Processes

- CMOS
- RF/mixed signal
- Automotive
- High voltage

eSilicon Headquarters
2130 Gold Street, Suite 100
San Jose, CA 95002
www.esilicon.com
https://star.esilicon.com
ipbu@esilicon.com
sales@esilicon.com
star@esilicon.com

1-408-635-6300
U.S. & Canada Toll Free:
1-877-7-MY-CHIP
(1-877-769-2447)