Specialist FPGA solutions for OTN, SONET/SDH and PDH networks

March 2012, V9

Contents

- About Aliathon
- Why Aliathon?
- Markets
- Products
- Partners
- Contact Details.

About Aliathon

Our Vision…

We are an self funded, sustainable and profitable organization. We deliver well packaged, efficient and cost effective FPGA solutions to network equipment manufacturers.

We achieve this by;

- Acting and delivering like the most flexible silicon solution on the planet.
- Working hand in hand with our clients to develop long term equitable partnerships instead of 1-off financial transactions.

Our people are motivated self starters who learn from & drive each other. In other words we don't carry passengers… We thrive on the challenges that our business presents, take pride in our work and make sure we enjoy the journey.

About Aliathon

Quick Facts….

- Founded 2001.
- 65+ combined years of complex systems and FPGA market experience.
- In-Depth Knowledge of Communications Standards.
- Market segment driven solutions portfolio.
- Ongoing Research Program.
  - Packet & Network Convergence

About Aliathon

Clients….

- Ranging from global telecommunications market makers to niche and bespoke communication solution providers.

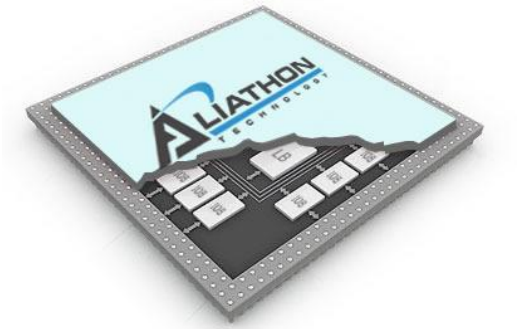
Markets….

- Aliathon operate across 5 main market segments;
  - Communications
  - Network Analytics / Service Assurance
  - Military
  - Test & Measurement
  - Video Networking

Why Aliathon?

Solutions….

- We develop innovative FPGA based solutions to help our customers process, terminate, generate, inspect, multiplex and attenuate every frame or packet carried through their OTN, SONET/SDH & PDH networks.
- We blend our TDM framing, mapping and packet solutions with your unique systems requirements to deliver the **perfect fit** for your project needs.



Why Aliathon?

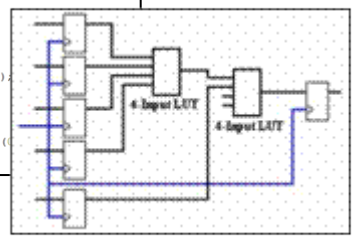
Technical / Commercial Flexibility…..

- Partnership business model designed to share risk & rewards.
- Professional support through entire product lifecycle.
- Perfect Fit - Only pay for what you want.
- Obsolescence proof
- FPGA Architecture expertise.
- FPGA Vendor independent.

Design Expertise…..

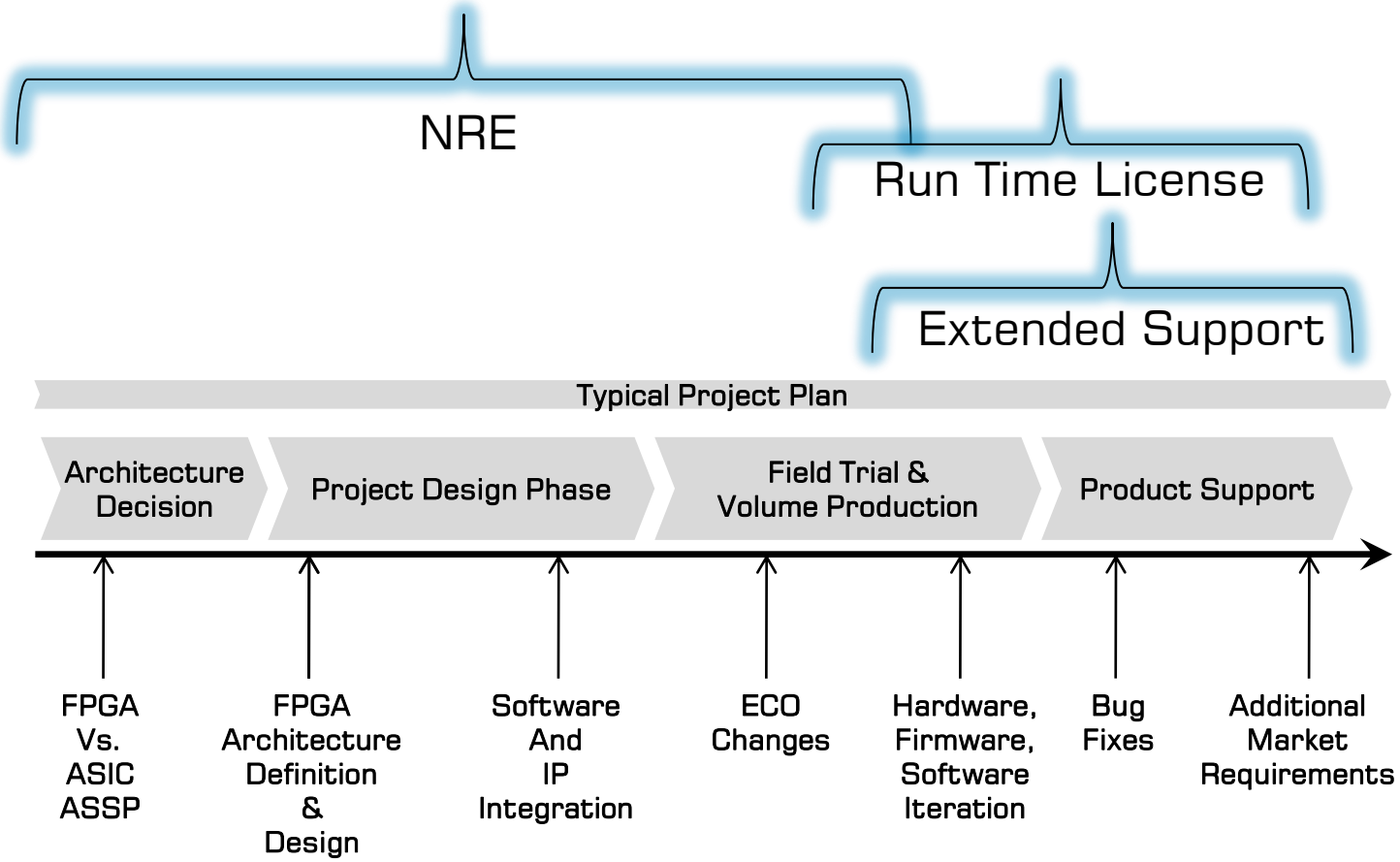
- Strong Software Design Background.
  - Highly Abstracted Design approach.
- Expert VHDL language knowledge.
  - HDL -> Gates…
  - Resource shared but functional coupling avoided…
  - Test & Verification (coverage & reuse).

```
subtype col_cnt_type       is std_logic_vector(6 downto 0);
type    col_cnt_array      is array (natural range <>) of col_cnt_type;
signal  pdh_col_pl         : col_cnt_array(0 to 4);
signal  pdh_vld_pl         : boolean_array(0 to 4);

-- pipeline for tu-demapper outputs
dmpl : process(reset,clk)
begin
  if reset then
    pdh_col_pl  <= (others => (others => '0'));
    pdh_vld_pl  <= (others => false);
  elsif rising_edge(clk) then
    pdh_col_pl  <= pdh_col_pl(1 to 4) & (lovc_col_cnt-"10");
    pdh_vld_pl  <= pdh_vld_pl(1 to 4) & (pdh_map="100");
  end if;
end process;

  elt1_byte_num <= pdh_col_pl(0)(4 downto 0) when pdh_vld_pl((
elt1_byte_num_i;
```



Why Aliathon?

Our Business Model



Why Aliathon?

Guaranteed Support when you need it most….

- Continue to reply on Aliathon's expertise, freeing up your team to concentrate on other tasks.
- Ensure longevity of support from Aliathon.
- Critical & Non-Critical Fault resolution.
- 200 hours direct access to solutions designers + 3 days on-site training.
- IP ports to different FPGA families, vendors and tools releases.
- Respond quicker to market/customer requirements.

Why Aliathon?

Support Options

Support Packages	Basic Support	Priority Telephone Support	Priority Email Support	Auto Updates	Cost	Support Contract Length	Support Scope
Basic	Yes	No	No	No	Free		
Bronze	Yes	Yes	Yes	Yes	15% project cost	6 months	Project
Silver	Yes	Yes	Yes	Yes	20% project cost	12 months	Project
Gold	Yes	Yes	Yes	Yes	30% project cost	24 months	Project
Corporate	Yes	Yes	Yes	Yes	Negotiable	Negotiable	Site/Global

Our Markets

Market Segments

Communications	Test & Measurement	Network Analytics / Assurance	Military	Video Networking
Mobile Backhaul (MBH)	Fibre-Optic Installation & Maintenance	Traffic Analysers / Monitors	Custom Comms Networks	Video / Data Network Interface Cards
Multi-Service Metro (MSPP, MSAN, ADM)	Bit-Error rate (BERT) Products	Intrusion Detection Systems	Global Information Grid (GIG) analytics	Optical Interfaces / Converters
Data Centre Interconnect / Datacom Networks Transport	Data Generators & Analysers	Cyber Security & Content Security Gateways		
40G/100G Transport / Transmission (LH DWDM)		Information Assurance		

Architectural Examples : Comms

Transponder

(Termination & Mapping at similar line rates, e.g. 100<>100, 40<>40 etc).

Client Rates

OTN	SONET/SDH	Packet
OTU4	OC768/STM256	10/40/100 GE
OTU3	OC192/STM64	
OTU2	OC48/STM16	
OTU1	OC12/STM4	
	OC3/STM1	

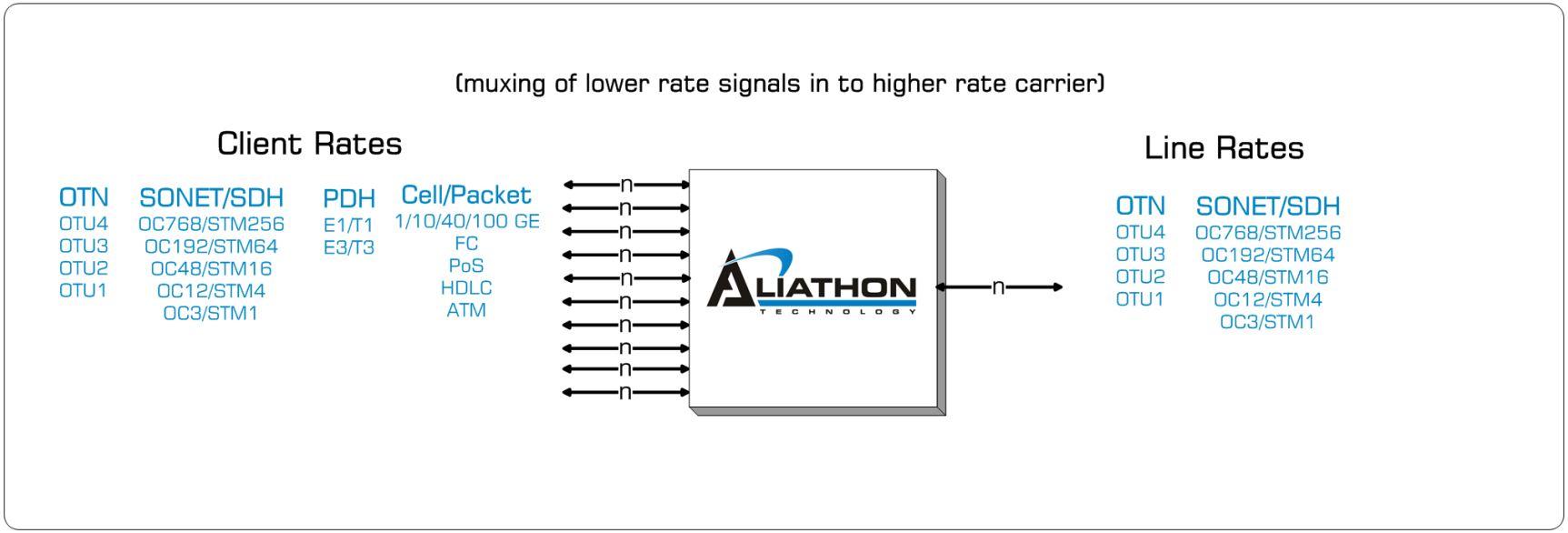
Line Rates

OTN	SONET/SDH
OTU4	OC768/STM256
OTU3	OC192/STM64
OTU2	OC48/STM16
OTU1	OC12/STM4
	OC3/STM1

Architectural Examples : Comms

Muxponder

(muxing of lower rate signals in to higher rate carrier)



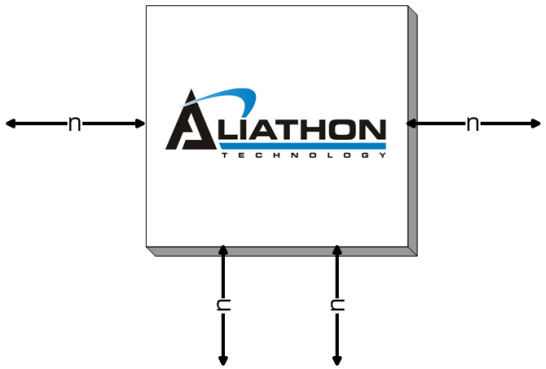
Architectural Examples : Comms

Add-Drop MUX

(add/drop of lower rate signals from higher rate carrier)

Client Rates

OTN	SONET/SDH
OTU4	OC768/STM256
OTU3	OC192/STM64
OTU2	OC48/STM16
OTU1	OC12/STM4
	OC3/STM1



Line Rates

OTN	SONET/SDH
OTU4	OC768/STM256
OTU3	OC192/STM64
OTU2	OC48/STM16
OTU1	OC12/STM4
	OC3/STM1

ADM Rates

OTN	SONET/SDH	PDH	Cell/Packet
OTU3	OC768/STM256	E1/T1	1/10/40 GE
OTU2	OC192/STM64	E3/T3	FC
OTU1	OC48/STM16		PoS
	OC12/STM4		HDLC
	OC3/STM1		ATM

Architectural Examples : Comms

Repeater / Regenerator

(termination and re-transmit using same payload structure)

Client Rates

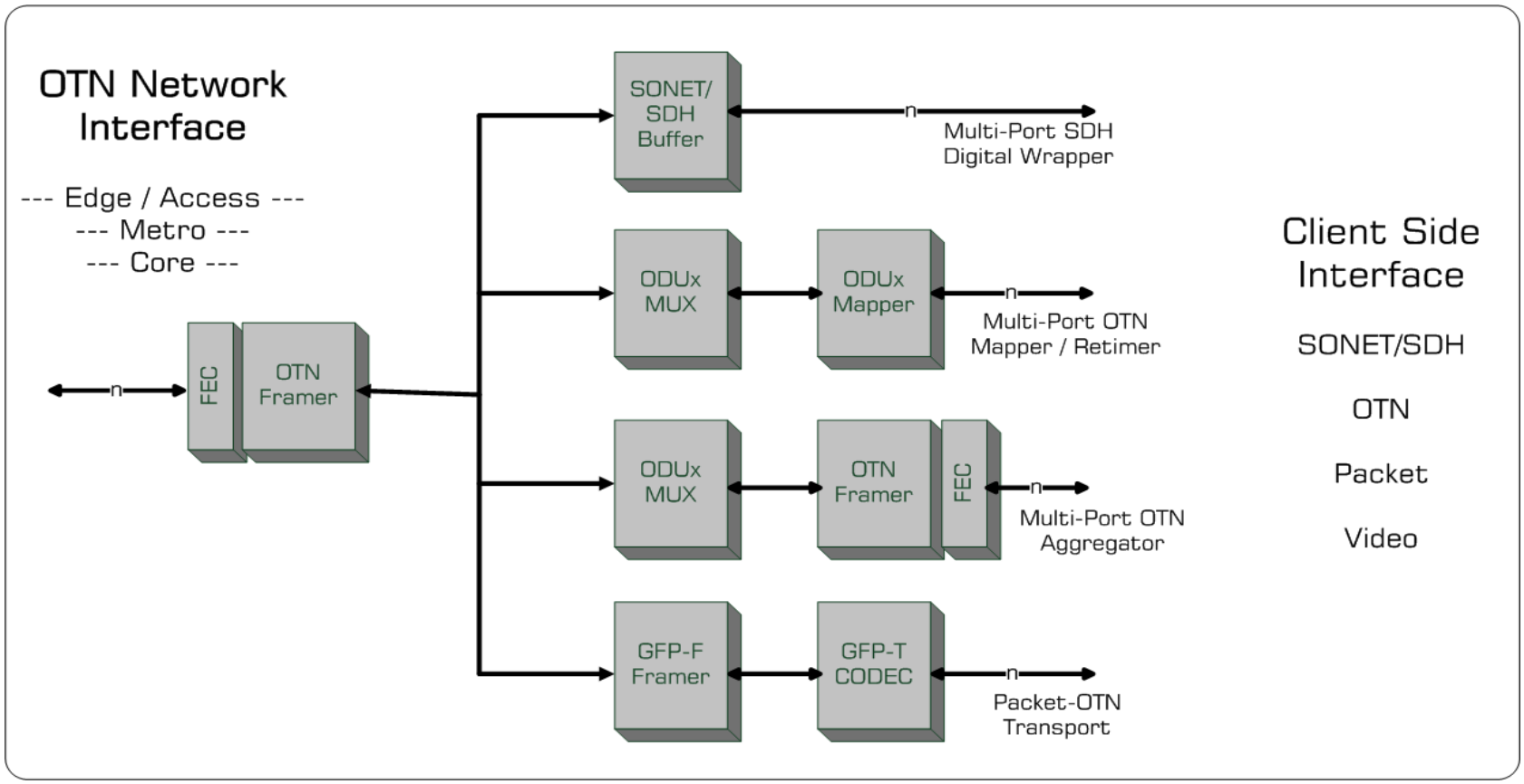
OTN	SONET/SDH
OTU4	OC768/STM256
OTU3	OC192/STM64
OTU2	OC48/STM16
OTU1	OC12/STM4
	OC3/STM1

Line Rates

OTN	SONET/SDH
OTU4	OC768/STM256
OTU3	OC192/STM64
OTU2	OC48/STM16
OTU1	OC12/STM4
	OC3/STM1

Our Solutions

Products: OTN



Products: OTN

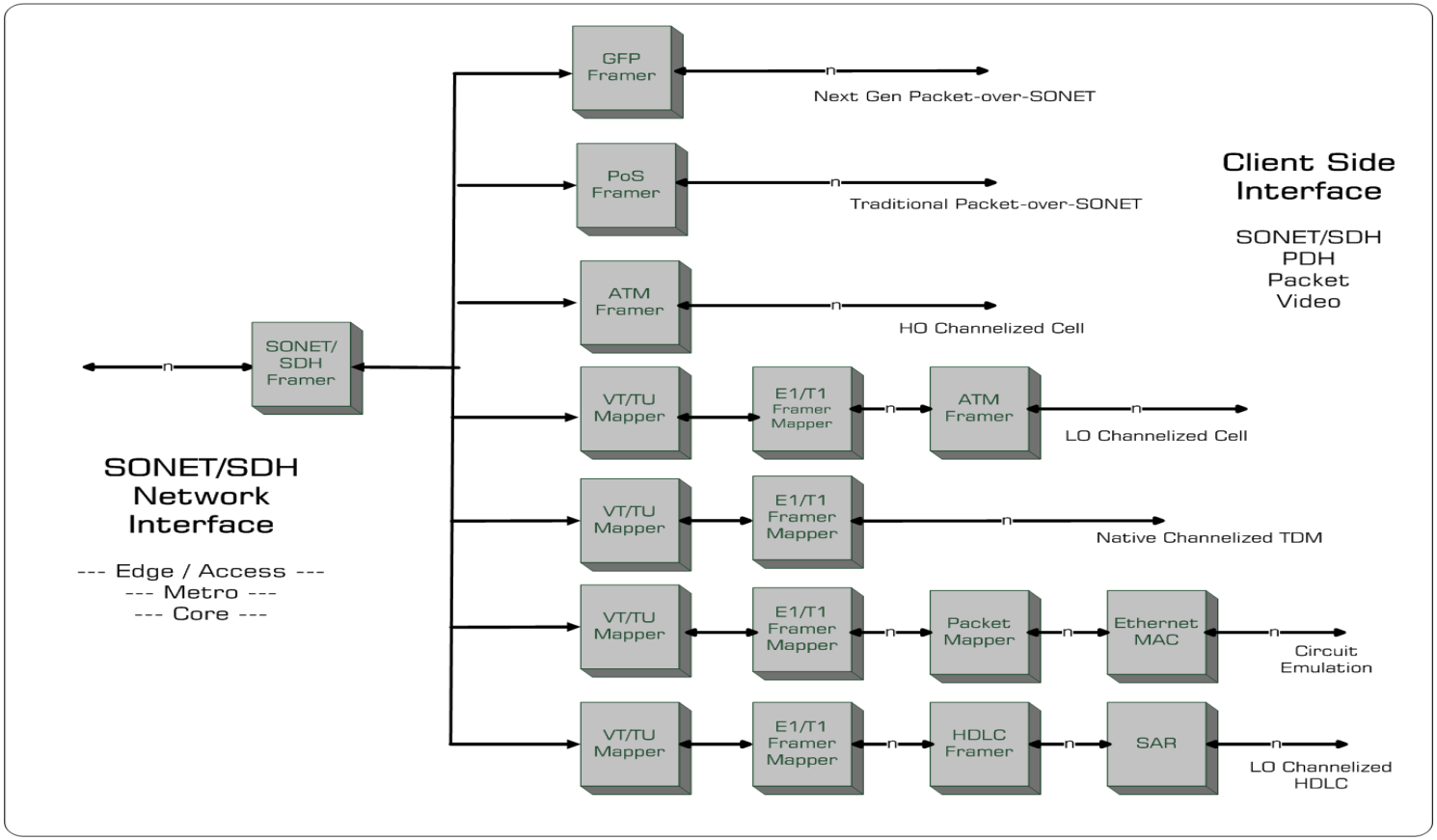
OTN Framer
•Supports OTU1-OTU4 line rates
•Conforms to G.709.
•G.709 FEC (GFEC) and optional EFEC support
•Processes OTUk, ODUk and OPUk overhead
•Supports synchronous (ATM, GFP) and asynchronous (SONET/SDH) payload mapping (accommodating positive/negative stuffing).

ODU Mux
•Supports G.708 Muxing of client ODU0/1/2/3 signals into ODU1/2/3/4
•Full OTN overhead processing for intermediate stages
•1 and 2 stage mux/demux functionality.

GFP-F (Framer)
•Compliant with ITU-T G.7041 specification.
•Generates/Synchronises to GFP data stream including IDLE frames.
•Provides GFP scrambling/descrambling.
•Full Overhead and Defect processing

GFP-T CODEC
•Compliant with ITU-T G.7041 specification.
•Encodes input blocks into 67 byte GFP-T blocks as per G.7041.
•Extracts 64 byte 8B/10B blocks of data from GFP-T frames.

Products: SONET/SDH



Products: SONET/SDH

SONET/SDH Framer
- Support for OC3/STM1, OC12/STM4, OC48/STM16, OC192/STM64 and OC768/STM256
- Single & multiple line interface support
- Conforms to G.707, G.806, G.783 and T1.105.
- Processes all STS/AU pointers and Higher Order paths.
- Full Overhead and Defect processing for all line interfaces and STS/VC paths

VT/TU Mapper
- Conforms to ITU G.707/ANSI T1.105
- Maps/Demaps multiple Lower Order VT/TU paths.
- All permutations of mapping path and VT/TU type supported
- Generates/Processes all VT/TU pointers.
- Full Lower Order Path Overhead processing

E1/T1 Mapper/Framer
- Framing and deframing for up to 1008/1344 E1/T1 channels (enough for a full OC48/STM16).
- Asyncronous and syncronous TU payload mapping/demapping
- Conforms to ITU G.704/ANSI T1.403.
- Frame generation and synchronization for T1, J1 and E1 PDH signals.
- Full Overhead and Defect processing per channel.
- Channel frame formats may be configured dynamically and independently, and asyncronous channel timing is supported.

Products: SONET/SDH

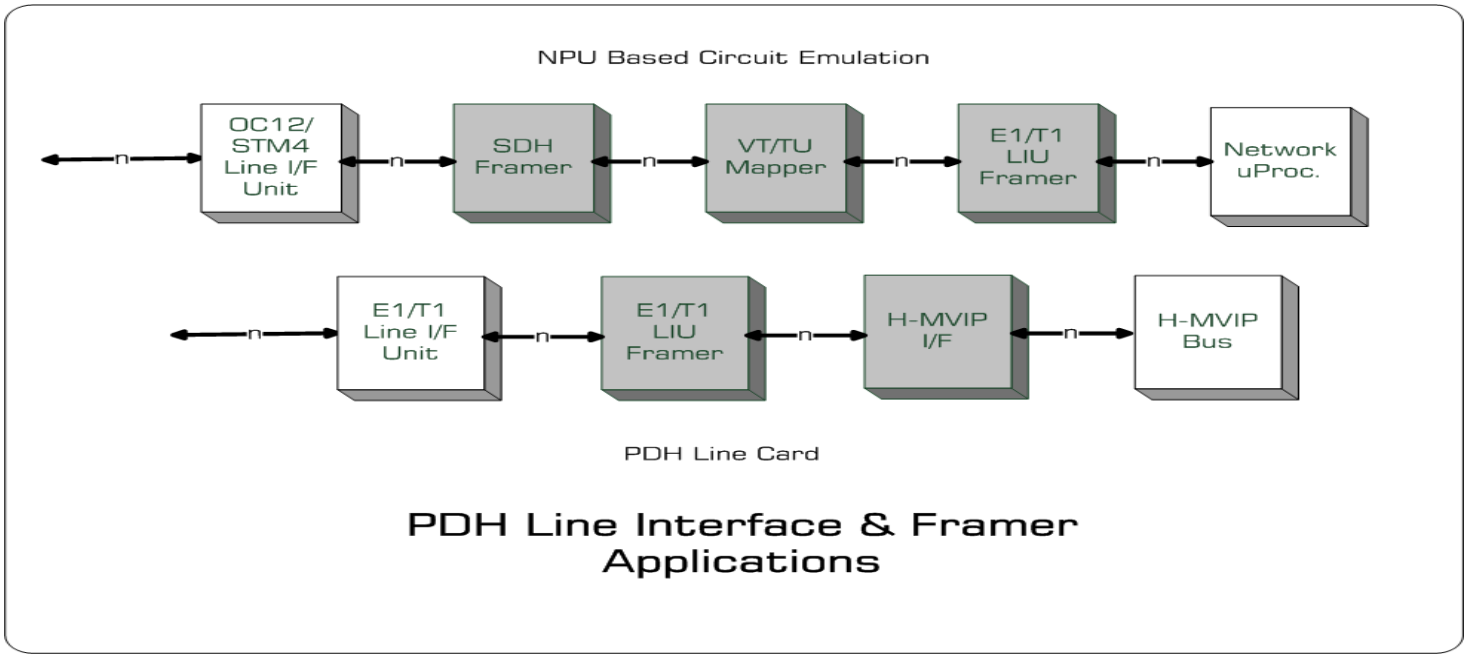
E3/T3 Mapper/Framer
•Performs frame synchronization and generation for T3, J3 and E3 PDH signals.
•Asyncronous and syncronous STS1/VC3 payload mapping/demapping
•Conforms to ITU G.704/ANSI T1.403.
•Core is capable of framing and deframing up to 24 channels (enough for a full 2 x OC12/STM4).
•Full Overhead and Defect processing per channel.
•Channel frame formats may be configured dynamically and independently, and asyncronous channel timing is supprted.

POS Framer
•Supports OC3/STM1 through to OC192/STM64.
•Designed to process concatenated SONET/SDH payloads.
•Support for CRC-16 and CRC-32.

ATM Framer
•Conforms to ITU I.432.1.
•Processes data for multiple independent TDM ATM streams.
•Configurable IDLE and Unassigned Cell insertion, detection and deletion.
•Optional HEC insertion; HEC error detection and correction.

HDLC Framer
•Multi-channel HDLC support (>8k channels)
•Supports bit-synchronous and byte-synchronous HDLC.
•Configuration may be applied to each stream independently, and changed dynamically.
•Full Overhead and Defect processing per channel

Products: PDH



Products: PDH

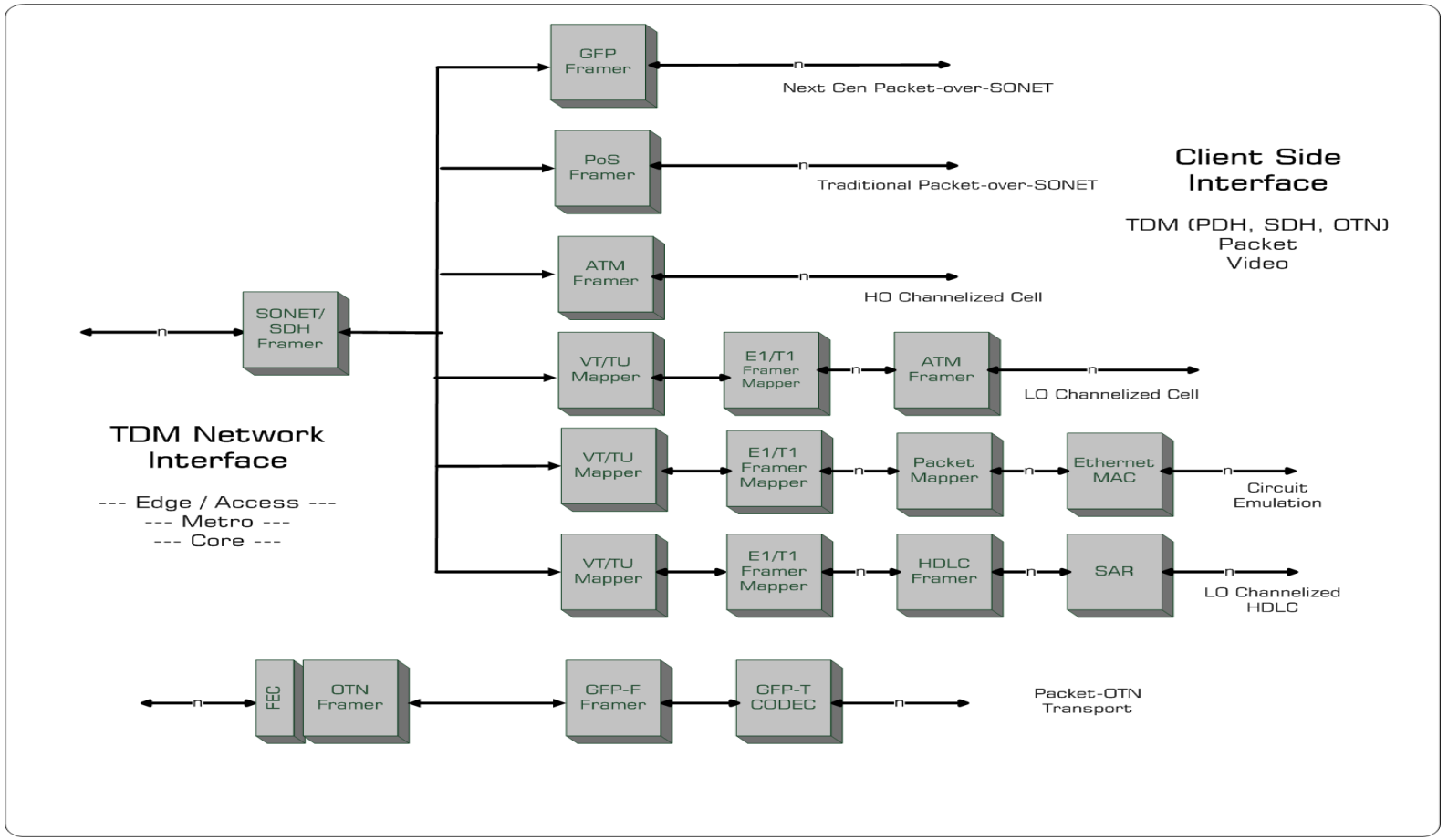
E1/T1 LIU/Framer

•Conforms to ITU G.704/ANSI T1.403.
•Performs frame synchronization and generation for T1, J1 and E1 PDH signals.
•Serial clk+data line interface support for connecting to standard E1/T1 LIUs.
•Jitter attenuation for up to 504/672 E1/T1 channels (2xOC12/STM4 links).
•Designed to provide G.832 and G.824 Output Jitter Compliance, for 2.048 kHz +/-50 ppm (E1), 1.544 kHz +/-32 ppm (T1).

E3/T3 LIU/Framer

•Conforms to ITU G.704/ANSI T1.403.
•Generates and performs frame synchronization for T3, J3 and E3 PDH signals.
•Supports up to 24 serial clk+data E3/T3 line interfaces
•M13 (DS3->DS2-DS1) and E3->E2->E1 support.

Products: Packet / Cell



Products: Packet / Cell

POS Framer
- Supports OC3/STM1 through to OC192/STM192.
- Designed to process concatenated SONET/SDH payloads.
- Inserts and detects CRC-16 and CRC-32.

ATM Framer
- Conforms to ITU I.432.1.
- Processes data for multiple independent TDM ATM streams.
- Configurable IDLE and Unassigned Cell insertion, detection and deletion.
- Optional HEC insertion; HEC error detection and correction.

HDLC Framer
- Multi-channel HDLC support (>8k channels)
- Supports bit-synchronous and byte-synchronous HDLC.
- Configuration may be applied to each stream independently, and changed dynamically.
- Full Overhead and Defect processing per channel.

Products: Packet / Cell

GFP-F (Framer)

- Compliant with ITU-T G.7041 specification.
- Generates/Synchronises to GFP data stream including IDLE frames.
- Provides GFP scrambling/descrambling.
- Full Overhead and Defect processing

Ethernet MAC

- Tri-rate (10/100/1000) & 10Gb Ethernet support. Compliant to IEEE-1588
- CRC-32 checking & generation
- Programmable frame length to support proprietary and standard frame lengths.
- Network statistics.

Our Partnerships

Partnerships

ALTERA®
AMPP℠
ALTERA MEGAFUNCTION PARTNERS PROGRAM

XILINX®
ALLIANCE PROGRAM

Mentor Graphics®