Solid State TECHNOLOGY
Insights for Electronics Manufacturing

Vertical through-wafer insulation: Enabling integration and innovation

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Through-wafer insulation has been used to develop technologies such as Sil-Via TSV and Zero-Crosstalk.

TSI, or through-silicon insulation, is the processing of silicon wafers by MEMS techniques to create dielectrically isolated areas of the silicon. By taking advantage of the high aspect ratio and vertical sidewall capabilities of deep reactive ion etching (DRIE), trenches can be formed in silicon which extend all the way through the silicon wafer (**FIGURE 1**).

The final wafer after TSI processing exhibits islands of single crystal silicon separated by high quality isolation. This structure is the basis of TSI, and forms the building block of many of Silex's offered technologies.

TSI has been compared to either a dielectric isolation (DI) or silicon-on-insulator (SOI) process, and the comparisons are fairly close. TSI has, in fact, been called a "vertical SOI" process because of its similarity to SOI in creating an insulator-based separation between sections of single-crystal silicon. Unlike SOI, of course, TSI goes vertically through the wafer to create islands of silicon joined by insulating bands. In this second way, it is similar to a DI process where dielectrically isolated islands are created on a SOI device layer, which are then used in device manufacture like diode arrays. Unlike DI, though, TSI extends completely through the wafer: the standard thickness for a TSI processed wafer is 430μm, thick enough to be processed through all MEMS or CMOS steps without the need for special carriers or handling. It is this mechanical strength which makes TSI so useful as a wafer level feature.

MEMS is, of course, a mechanical structure and MEMS structures can use the entire bulk of the silicon as elements in its construction. This is unlike ICs which are primarily concerned with the surface 10 or 20μm of silicon area where the circuit elements are formed. And yet MEMS wafers undergo wafer processing which has all the requirements of IC processing (in terms of implants, diffusions, thermal or deposited films, thermal budgets, etc.) plus additional challenges of deep etching, forming complex 3D structures, wafer to wafer bonding, debonding, oxide or silicon release, and noble metal processing. Any TSI process, then, would have to hold up to the full range of processing challenges.

FIGURE 1. SEM image of TSI DRIE etch through silicon.

Sil-Via TSV

TSI was developed in the 2003-4 timeframe when a working through-silicon via (TSV) approach was

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needed for a major customer. This customer needed a TSV solution which was via-first (the TSV patterned and formed prior to any other wafer processing), high density (small footprint of the device was critical), and high reliability (the end application was a smartphone.)

Traditional approaches to TSVs at the time were poly-fill (which didn't offer the low resistance or reliability that the customer needed) or metal-filled (which suffer from reliability concerns due to TCE mismatch with the silicon), but our engineers recognized that a new approach was needed. Their solution was to take a highly doped substrate, typically phosphorous doped down to 1-3 mΩ-cm or less, and use the TSI approach to form a via out of the single crystal silicon (**FIGURES 2 and 3**).

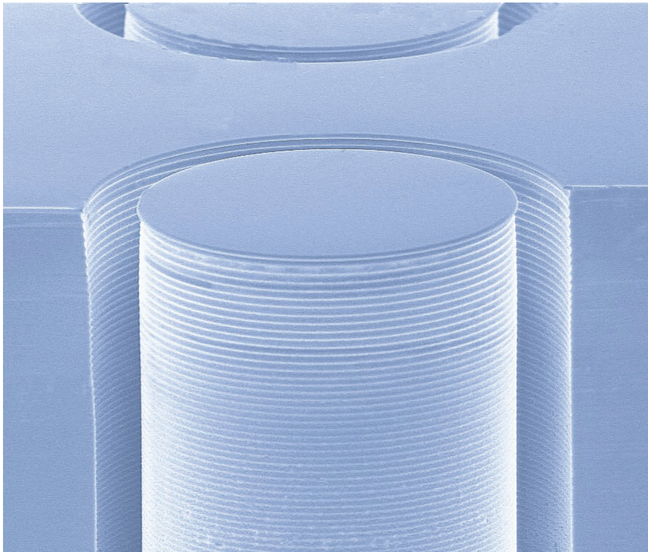

FIGURE 2. SEM of the TSI etch to form the Sil-Via TSV.

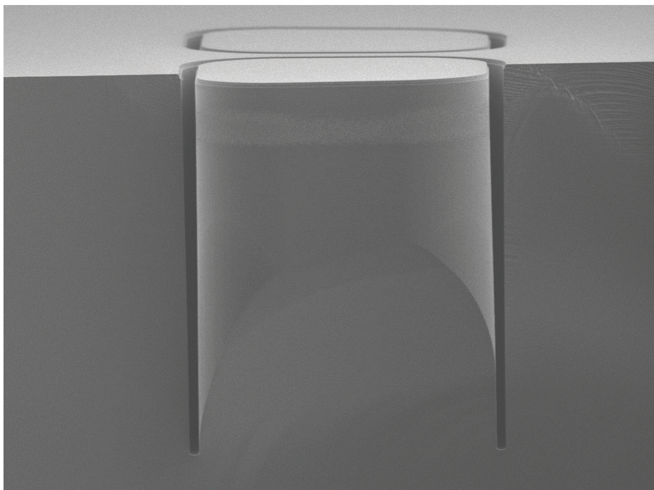

FIGURE 3. Example of two Sil-Via TSVs with oblong shape. Note the tight via pitch possible with TSI processing.

The resulting structure is a single crystal, full wafer thickness TSV exhibiting typical resistances of 0.5-1Ω for a 100µm diameter x 430µm thick via. The single crystal construction (formed out of the native wafer material) is perfectly matched thermally to the wafer, eliminating any TCE concerns or reliability issues. The gap formed by the TSI etch is filled by a proprietary insulating material, and gives TeraOhm level DC isolation of the via post to the surrounding substrate.

The Sil-Via TSV went into production in 2005 and eventually ramped up to a peak of 2000 wafers per month. Since then, the Sil-Via has been in continuous production and implemented on over 50 different products on both 6" and 8" wafers. With over 50,000 wafers shipped across all products, we have seen zero field failures for the TSV making it one of the most widely recognized and reliable TSV technologies on the market.

Sil-Via TSVs have been used in bulk MEMS applications, wafer capping, and advanced silicon interposers for 2.5D and 3D packaging, as will be discussed below. They can support via pitches down to 50µm and continuous via formation across the entire wafer. As we shall discuss later as well, Sil-Via provides an intriguing platform for higher functional integration, such as ESD protection diodes and functional interposer solutions.

Met-Via TSV

While Sil-Via addressed the production, cost, and reliability needs of the market when it was released, TSI has been adapted to support metal through-silicon vias since then. Using the vertical isolation for sidewall protection of the TSV, Silex has brought to market an all-metal TSV that meets the low resistance and high frequency needs of our customers. Licensing the XiVia™ technology from ÅAC Microtec, another Swedish company creating packaging solutions for space-level reliability applications, the Met-Via utilizes two connected DRIE TSVs and double sided copper RDL plating with hermetically sealed vias to create a high reliability metal TSV. The XiVia approach creates a 'locking pin' which protects against thermal cycling concerns, and the hollow-plated TSV gives additional flexion for the TCE mismatch (**FIGURE 4).**

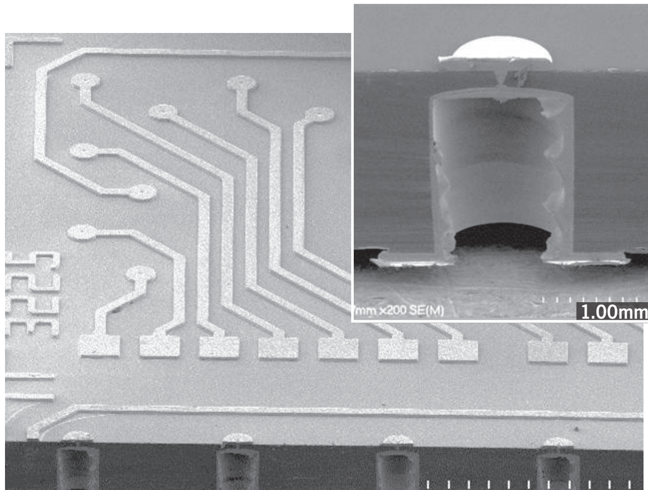

FIGURE 4. Microphotograph of Met-Via interposer test structure with close-up of Met-Via cross-section showing the XiVia feature. (some metal smearing evident due to wafer saw).

Zero-Crosstalk substrate isolation

The Sil-Via TSV is in essence a round post through the silicon wafer, but the beauty of TSI's flexibility is that it doesn't have to be like that. TSI is patterned by lithography, so any geometry or shape can be formed as a TSI structure (There is a practical limit to this: first there are processing challenges relating to the percent of silicon being etched away across the entire wafer, and second the trench width has to be consistent in order to have a complete and reliable fill).

Taking a clue from the "Vertical SOI" image of TSI, Silex developed and also offers a substrate isolation platform called Zero-Crosstalk™. This uses either chains of Sil-Via type structures, or continuous trench rings to define the isolated areas of the silicon. Each silicon island then is completely DC isolated from its neighbors, making them act as physically distinct pieces of silicon. A common application for Zero-Crosstalk is to create separate analog and digital grounds for mixed-signal applications (**FIGURES 5 and 6**).

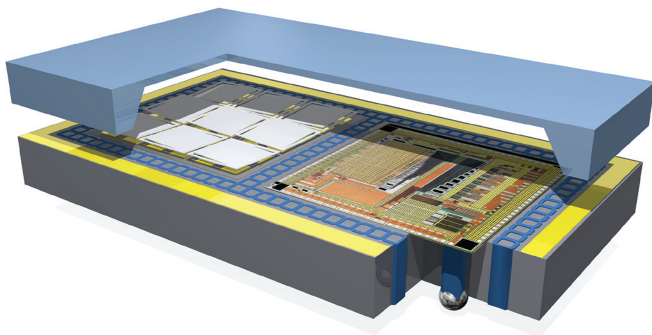

FIGURE 5. Zero-Crosstalk™ concept CAD drawing.

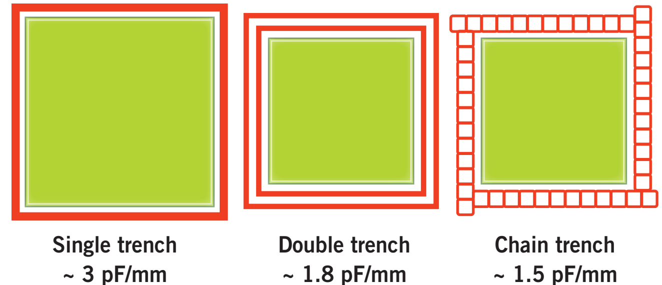

FIGURE 6. Three different options for Zero-Crosstalk showing typical capacitance figures for a 20μm trench – 350μm wafer thickness implementation.

Zero-Crosstalk can be implemented on low resistivity or high resistivity substrates, making it a viable technology for IC substrate isolation as well (**FIGURE 7**).

In the MEMS area, Zero-Crosstalk has among other applications been used for LED interposers to provide isolated substrates for diode arrays, X-Ray detectors to isolate individual detection elements, and in the following example.

In this product example of a microbattery array from mPhase Technologies, TSI is used to create electrically isolated microbattery cells which also act as electrical interconnects through the cell layers. This is an example of the flexibility of TSI, where arbitrary geometries can be defined which can act both as Zero-Crosstalk areas and Sil-Via TSVs (**FIGURES 8-10**):

The rigid interposer approach

The application which drove the development of TSI and the Sil-Via TSV was for a 2.5D interposer with Zero-Crosstalk for cellphone microphones, with the CMOS ASIC mounted side-by-side. MEMS has, in fact, always been involved with advanced packaging requirements because of the need to package the MEMS and IC in the same package.

Interposers for package-level integration of multichip ICs is an emerging hot topic and an area that most major OSATs, one where packaging houses are looking to provide complete solutions. MEMS foundries like Silex have a critical role to play in this

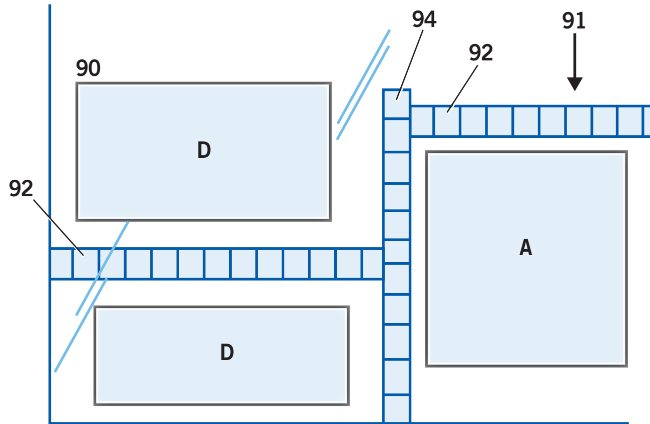

FIGURE 7. CAD drawing showing separate analog/digital substrate areas defined by Zero-Crosstalk.

emerging supply chain, as the interposer foundry for either the IC company or the OSAT directly, as neither entity nor the traditional IC foundry has the infrastructure or expertise to build these 3D structures

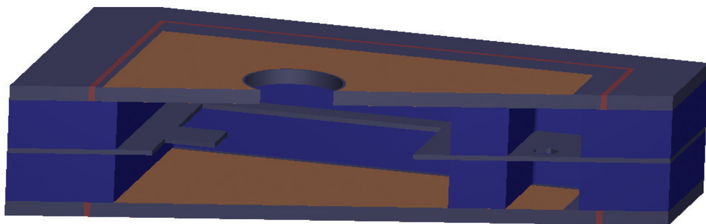

FIGURE 8. Cross section diagram of the 5-layer bonded mPhase microbattery structure.

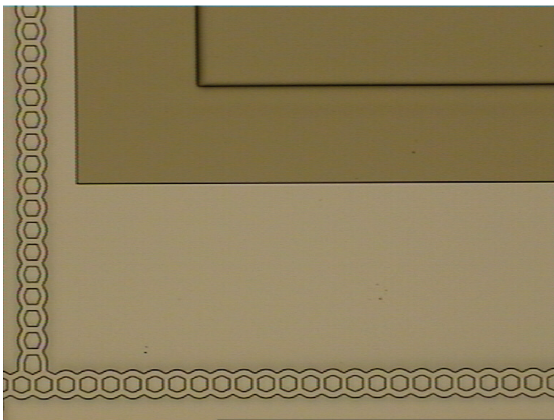

FIGURE 9. Photomicrograph of the TSI chain structure defining the Zero-Crosstalk TSV structures for the mPhase microbattery.

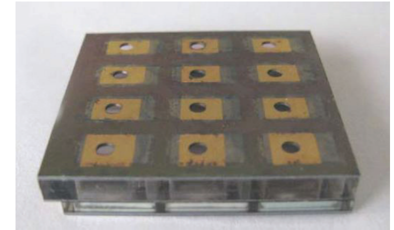

FIGURE 10. Photomicrograph of the final mPhase microbattery (image courtesy mPhase Technologies, Inc.).

reliably and in high volume. Yole Developpement refers to this emerging supply chain element as the "Mid-End Foundry," and predicts it will service a $1.7B market by 2017 as interposer packaging hits the mainstream.

And yet, despite all the press about 3D integration, the engineering challenges of 3D packaging have presented a substantial barrier to companies pursuing this packaging path. This is because each element of the package presents engineering challenges, and the current focus of the 3D industry (ultra thin wafers, specialty wafer handling, organic substrates, chip to chip signal routing, thermal and electrical optimization, and yield loss ownership by the supply chain) make the challenges to adoption more daunting. This focus is also concentrating on the very bleeding edge of technology (like the highest cost FPGAs), technologies which are overkill for the majority of ICs being produced in the market.

Our approach is to leverage our full wafer thickness TSI technology to provide rigid interposers to the marketplace, simplifying the engineering and supply chain challenges. "Rigid Interposers" means interposers from 300 to 430μm thick, with enough mechanical strength to support the microbump, mounting and molding steps of the assembly process. By eliminating the ultrathin wafer requirements and

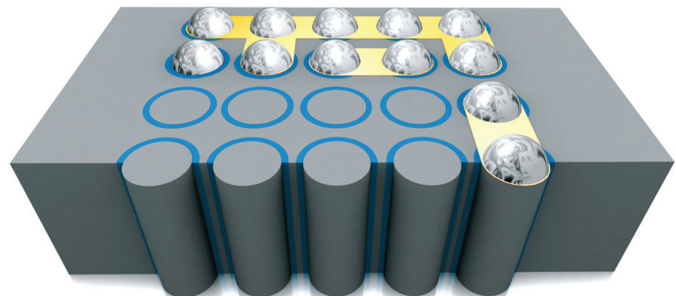

FIGURE 11. Graphic of a Sil-Via based interposer.

associated bonding, debonding, and carrier handling steps, not only is the assembly process simplified but the organic substrate used in the 2.5D package can be eliminated. What results is an all-silicon package which is reliable, mechanically strong, and thermally stable for advanced IC use (**FIGURE 11**).

2.5D packaging technologies offer integration and footprint reduction advantages to a wide range of IC uses, yet the extreme costs and engineering challenges of the mainstream approach effectively removes it from consideration for the majority of the market. We believe that rigid interposers not only simplifies the engineering challenges, but makes 2.5D a viable option for a much broader IC market.

Future TSI-enabled markets

Even though it was created to solve a specific need, TSI remains a platform for innovation in bringing new customer-integratable features to the market. Among the technologies being worked on by Silex or with customers today are:

- Full DI substrates for IC processing – the application of Zero-Crosstalk for IC applications, taking the concept of full dielectric isolation all the way to the IC fab.
- CMOS TSVs – TSVs as interconnects which allow stackable components has long made technological and economical sense for MEMS components. Extending this to the IC world as a via-first or via-middle technology which can support full IC processing is the natural progression of this capability.
- Metal IC TSVs – Many ICs require the performance of an all-metal TSV, and foundries want to avoid the cost and expense of thin wafer handling. Integrating the Met-Via TSV as a via-middle process into the customer's design and IC flow affords the advantages of all metal TSVs without the limitations of thin wafer handling (which are only available at the highest and most costly technology nodes)
- TSVs with Integrated Diodes – since Sil-Via is a doped substrate silicon TSV, the via can be constructed to incorporate blocking or steering diodes directly into the via, thereby giving active component capability integrated directly into the via.
- TSVs with ESD protection – a variant of the integrated diodes, especially for interposers where multiple chips can be interconnected and protected at the same time
- Through-silicon 3D inductors – making use of the copper TSV technology of Met-Via to create a true wound inductor, using the silicon wafer itself as the inductor spool. A mag core element can be integrated to boost Q value, as well.

Summary

The TSI platform has proven to be a very reliable and production worthy technology. In continuous production for over six years, it has been integrated in one form or another in over two dozen different projects. Customers, working with Silex engineers, continue to find innovative ways to take what's available in TSI and re-purpose it for another use. By providing higher value customer-integratable features, both Silex and the customers stay ahead in the MEMS and packaging games. TSI truly allows all true semiconductor integration options to be "more than Moore." ◆

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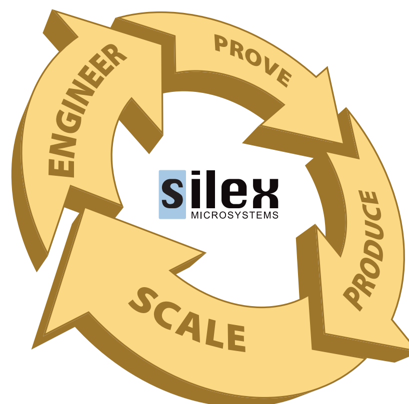

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