

From Medical and Wearables to Big Data: Differentiated IP for the IoT Spectrum

Whether it's a tiny always-on medical device or a secure cloud network processing Big Data, the Internet of Things is bringing new challenges to IC design. This white paper provides techniques and IP examples for managing IoT's power and bandwidth demands

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March 2015

Ultra-Low-Voltage SRAM and TCAM Enable IoT Markets

Today, we are seeing the world around us becoming increasingly smarter. Almost any manufactured good now includes an embedded processor (typically a microcontroller, or MCU), along with user interfaces, that can add programmability to enable "command and control" functionality. The electrification of the world and the pervasiveness of embedded processing are the keys to making objects "smart."

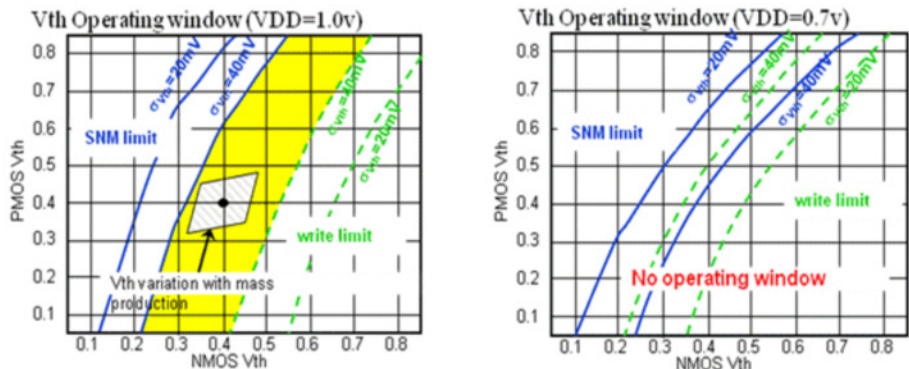
After a device becomes smart through the integration of embedded processing, the next logical step is remote communication with the smart device to help make life easier. We see several emerging IoT markets that will generate lots of data, which will have to be digested and analyzed in order to become useful for non-technology companies. Some of these markets include medical devices, utilities, insurance, mining, agriculture, retail, transport, airlines and automobiles.

Medical and Wearables

When looking at medical devices we see that the device is mostly "on" and listening for incoming data. What types of IP are most useful for this market? Both active power and static power are critical for maintaining long battery life. Therefore optimizing for very low voltage as well as very low leakage is important. These devices typically operate significantly below 100MHz.

Most available memory IP is not optimized for these criteria. Most semiconductor foundries prefer to develop and manage the SRAM bitcells. Because SRAM cells are limited by stability (or static noise margin) and write ability (or write margin) the lowest operating voltage (VDDMIN) is carefully specified. The random threshold variations in subnanometer technologies have resulted in serious yield issues for realizing low VDD READ/WRITE operations with a 6T SRAM cell. The use of different cell topologies may improve the SRAM stability at low operating voltages.

Figure 1: SRAM Bitcell Static Noise Margin

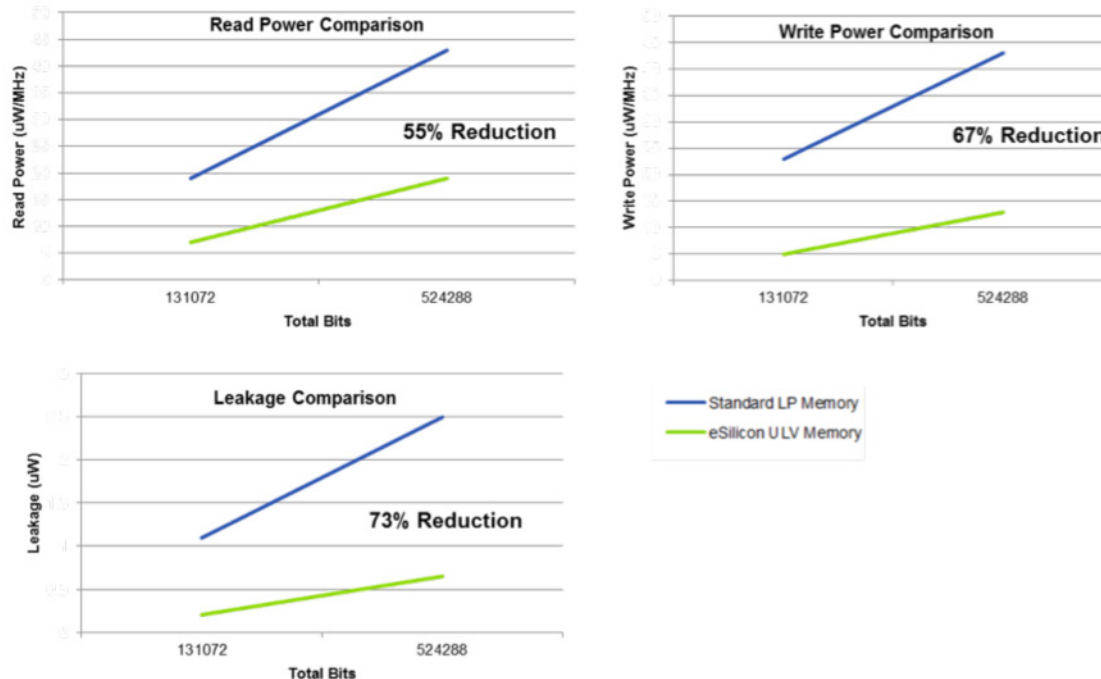


Circuit techniques such as NMOS and PMOS biasing, periphery shutdown, and use of high transistor threshold implants can manage and reduce the static power component of embedded SRAM. The combination of some or all of these techniques with new bitcell topologies offers a highly differentiated SRAM solution for embedded medical devices.

We see that Bluetooth-enabled devices have similar criteria, however the device is often in standby and listening for an activation signal to turn the device to functional mode. The circuitry that is always “on” listening and activating the device into functional mode is a small component and doesn’t draw much current. However, this contribution may become significant if the device is operating more in standby mode. These devices also have slower clock cycles up to a maximum of 100MHz.

eSilicon has developed statistical simulation techniques to determine statistical failure probability distributions for low-voltage failure modes for various bitcell topologies. Bitcell read current, read-disturb margin, write margin, minimum data-retention voltage (MDRV), and leakage current are all thoroughly analyzed. These techniques enable quantification of actual failure rates as a function of critical process parameters, temperature, voltage, and design parameters. Effective design optimization for optimum VDDMIN, power, performance, and yield is enabled by these efficient simulation techniques. The result is a series of optimized SRAM architectures that operate below 100MHz, below 0.7V, and at one-fourth the leakage power of other available SRAM compilers at 65nm, 55nm, 40nm and 28nm technologies.

Figure 2: eSilicon 40nm Single-Port SRAM



Networking and Big Data Analytics

For the network, sophisticated cloud-based processing requires a new generation of communications processors that can keep track of all of those connected devices, communicate with them and translate their functionality into useful services, all with non-linear improvement to their performance and efficiency. The challenge will be to build secure networks that keep up with demand, while simultaneously reducing energy consumption and cost of equipment. This will require all kinds of innovations, well beyond the improvements that Moore’s law can deliver.

What IP is needed to support these networking applications? Networking processors have multiple CPUs that require large amounts of data access and storage. According to the ITRS the market drivers for networking and communications are:

1. Bandwidth
2. Reliability
3. Time-to-market
4. Power

Network processors are designed to address the performance problems resulting from exploding Internet traffic. The development efforts of these network processors concentrate almost exclusively on streamlining their data paths to speed up network packet processing, which mainly constitute routing and data movement. Rather than blindly pushing the performance of packet processing hardware, an alternative approach is to avoid

repeated computation by applying the time-tested architectural idea of caching to network packet processing.

Many of the table lookup tasks at different network layers that were originally implemented in software are now being replaced by hardware solutions to meet performance requirements. An efficient hardware solution to perform table lookup is the content addressable memory (CAM). A CAM can be used as a co-processor for the network processing unit (NPU) to offload the table lookup tasks.

CAMs are hardware search engines that are much faster than algorithmic approaches for search-intensive applications. CAMs are composed of conventional semiconductor memory (usually SRAM) with added comparison circuitry that enables a search operation to complete in a single clock cycle. The two most common search-intensive tasks that use CAMs are packet forwarding and packet classification in Internet routers. CAMs are also beneficial in a variety of other applications that require high-speed table lookup such as processor caches, translation lookaside buffers (TLB), data compression applications, database accelerators, and neural networks.

Associative lookup structures lie at the heart of many computing problems. CAMs provide fast constant time lookups over a large array of data (content keys) using dedicated parallel match circuitry. The most widespread exploitation of this technology occurs in high-performance routers, for route lookup, access control and packet classification.

What makes the ternary CAM (TCAM) abstraction such a powerful primitive for many of these applications is the ability to simultaneously search through a large number of subspaces of a higher dimensional space in one shot. For example, each

subspace can be compactly represented as one (or a few) TCAM entries using the “don’t care” bits to cover ranges that constitute it.

De-duplication techniques for cache, memory, I/O and storage data all exploit some form of content lookup or comparison schemes. Ternary bloom filters can be used to achieve an order of magnitude throughput improvement over current techniques in high-speed multiple-string-matching (MSM) problems, a key component in data de-duplication, sequence alignment and intrusion detection techniques.

Additional tasks have arisen from the expansion of multiple types of bridging, network routing, and transport being combined with merged protocols such as PBB-TE and MPLS-T. In attempting to address new requirements from support of IP/MPLS or hybrid IPv4/IPv6 networks, some OEMs have turned to broader use of search-centric processors, often based on the use of special content-addressable memory such as TCAM. In some cases, the TCAM search engine can be combined with other centralized control-plane or data-plane functions, but in other cases it deserves its own specialized role near the route engine.

Available today, eSilicon’s 14/16nm TCAM compiler offers 1 gigasearch per second under worst-case conditions with low-power search features. The TCAM is available in multi-port and variable byte search configurations. The multi-port architecture is 1 gigasearch per second per port.

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