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Spin-Coating Defect Theory and Experiments

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This paper presents a theory to explain how detectable defects are generated during a material's transition from a liquid state into a solid film. The hypothesis of defect formation is that it occurs as a result of an imbalance of molecular forces and molecular motion during the material phase transition. Experimental validation was done using a model spin-on silicon hardmask. Spin time and bake temperature were studied as process parameters to control defect counts. Wide variations in the resulting defect counts show strong statistical significance. The experimental results fit very well with the hypothesis. This preliminary study on defect mechanisms gives a direction to develop next-generation defect-free materials.

Introduction

Defects are fatal to integrated circuit (IC) manufacturing because they cause open or short circuits. Foundries must battle defects throughout the entire development cycle, from early prototypes of individual transistors to current large-scale ICs, which makes up most of the cost of IC products. The industry has put forth tremendous effort to reduce defects by investing in expensive clean room equipment, implementing complicated processing procedures such as iterate filtration and dummy dispense, and developing sophisticated materials with inherently fewer defects. While defects are being controlled, the resolution and efficiency of defect-scanning tools are improving, allowing even more defect details to be identified and characterized.

In addition to environmental contamination that contributes foreign defects, defects intrinsic to a material are extremely critical for material selection. A process-of-record (POR) material could be replaced simply due to an unsolvable defect issue. Intrinsic defects can be considered a basic property of the material, even though filtration and contamination are tightly controlled. Silicon- or metal-containing hardmasks (Si-HMs) are known to have typically high intrinsic defects.[1~3] Some foundries have worked hard to eliminate defects for these Si-HMs, and, as a result of the difficulties in doing so, have finally conceded to a reduced silicon content to alleviate defect issues. Therefore, to further explore defect issues, the research presented here will focus on a model spin-on Si-HM and how to mitigate the intrinsic defects.

To investigate intrinsic material defects, we should first learn how to generate and classify the defects and then how to control the defect counts. In the case of low defect counts, environmental contamination and wafer pre-count defects can have a significant effect on test results. Therefore, to reduce the contribution from these sources, a method of forcing higher defect counts is proposed. This method is also capable of giving stronger statistical significance, resulting in more precise defect characterization, and will also help reduce the cost of routine investigations. This approach is a very efficient way to develop low-defect materials.

Assumption of defect formation

The fundamental assumption in this paper is that intrinsic defects are formed during the transition from liquid material to solid film and from the imbalanced molecular forces that occur during this process. ***Figure 1*** shows a representative viscosity curve during the wafer spin-coating process. The spin-coating process is represented by the thin black curve, and the hot plate baking process is represented by the thick red curve. The dark green areas, D1, D2, and D3, are the regions where viscosity is less than a certain level (below light orange area of high viscosity) and the areas where molecular imbalance and motion would be most likely to result in defect formation. When the material is dispensed onto a wafer, it is still in a pure liquid state, and the molecules' Brownian motion is in an equilibrium condition. In this case, the molecular motion does not change molecular statistical distribution, and, hence, there is very little chance of defect formation. After spinning to a point where solvent evaporation makes the material more

viscous and the temperature decreases (viscosity in ***Figure 1*** reaches the blue dashed "Saturated soluble" line), the material may start to precipitate. In the precipitation process, the equilibrium state is disturbed because multiple phases of material are mixed together. In this state, the precipitated molecules may serve as a nucleation site for further particle growth and aggregate to build a defect. The aggregation continues until material viscosity is high enough to prevent further molecular motion, as indicated by the dark green areas of D1 and D2 in the figure. This process is very fast, and the material dries before it reaches another new equilibrium condition. The imbalanced molecular forces of a non-equilibrium condition are set and become a potential tension in the film. The tension could be released by molecular motion during hot plate baking reflow, giving rise to another set of conditions for possible defect formation, as shown in region D3 in ***Figure 1***.

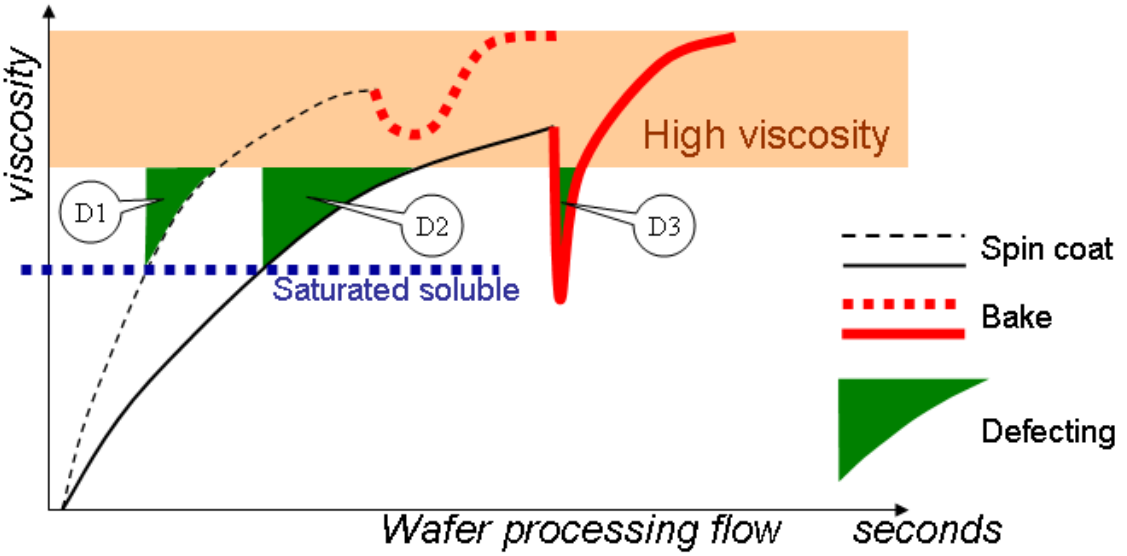


Figure 1. *Viscosity curve during wafer process flow, where the spin-coating section is represented by the thin black curves and hot plate baking is represented by the thick red curves. The dark green areas indicate the time windows of defect formation. The solid curves represent a conventional a wafer process, and the dashed curves are an improved process proposed for lower defect counts.*

According to this theory, retaining material solubility at high viscosity is very critical to defect performance. Wafer processing design is important to controlling defect counts. Based on this theory, the defect generation time window can be reduced by using rapidly evaporating solvents or by using high spin speeds and exhaust rates. Slow temperature ramp-up could eliminate defect formation during hot plate baking reflow.

Experiment I

This experiment was done with a model spin-on Si-HM. Spin time and bake temperature were the only two variables in the test matrix. ***Table 1*** details the test plan and the defect count results. The material was coated onto 8-inch bare silicon wafers using a TEL Clean Track Mark VIII wafer processing tool. The spin speed was fixed at 1500 rpm with 5000 rpm/s acceleration under the default exhaust. Before and after coating, the wafers underwent scanning using a KLA-Tencor Candela CS20 defect detection tool. The resolution is claimed as 80-nm particle size. The pre-count and post-count defect values are recorded in the "preC" and "postC" columns. The "net defects" are the differences between post- and pre-count values, which are much larger than pre-count values and the standard deviations in the last column. Such large differences indicate that the experimental results have strong statistical confidence.

Table 1. *Test plan and results*

run order	spin time	bake	preC	postC	net defects	std
#1	***5 s***	**205℃, 60 s**	**66**	**10996**	**10930**	105
#2	***40 s***	**205℃, 60 s**	**69**	**8141**	**8072**	90
#3	***70 s***	**205℃, 60 s**	**148**	**7396**	**7248**	85
#4	***90 s***	**205℃, 60 s**	**26**	**6032**	**6006**	77
#5	***120 s***	**205℃, 60 s**	**26**	**2955**	**2929**	54
#6	***300 s***	**205℃, 60 s**	**449**	**3396**	**2947**	54
#7	**300 s**	***20℃ (no bake)***	**7**	**3016**	**3009**	55
#8	**60 s**	***40℃, 120 s + 205℃, 60 s***	**3**	**3810**	**3807**	62
#9	**60 s**	***60℃, 120 s + 205℃, 60 s***	**43**	**3572**	**3529**	59
#10	**60 s**	***160℃, 60 s***	**34**	**3136**	**3102**	56
#11	**60 s**	***175℃, 60 s***	**104**	**3772**	**3668**	61
#12	**60 s**	***190℃, 60 s***	**143**	**5397**	**5254**	72
#13	**60 s**	***205℃, 60 s***	**95**	**8620**	**8525**	92
#14	**60 s**	***220℃, 60 s***	**1**	**2389**	**2388**	49

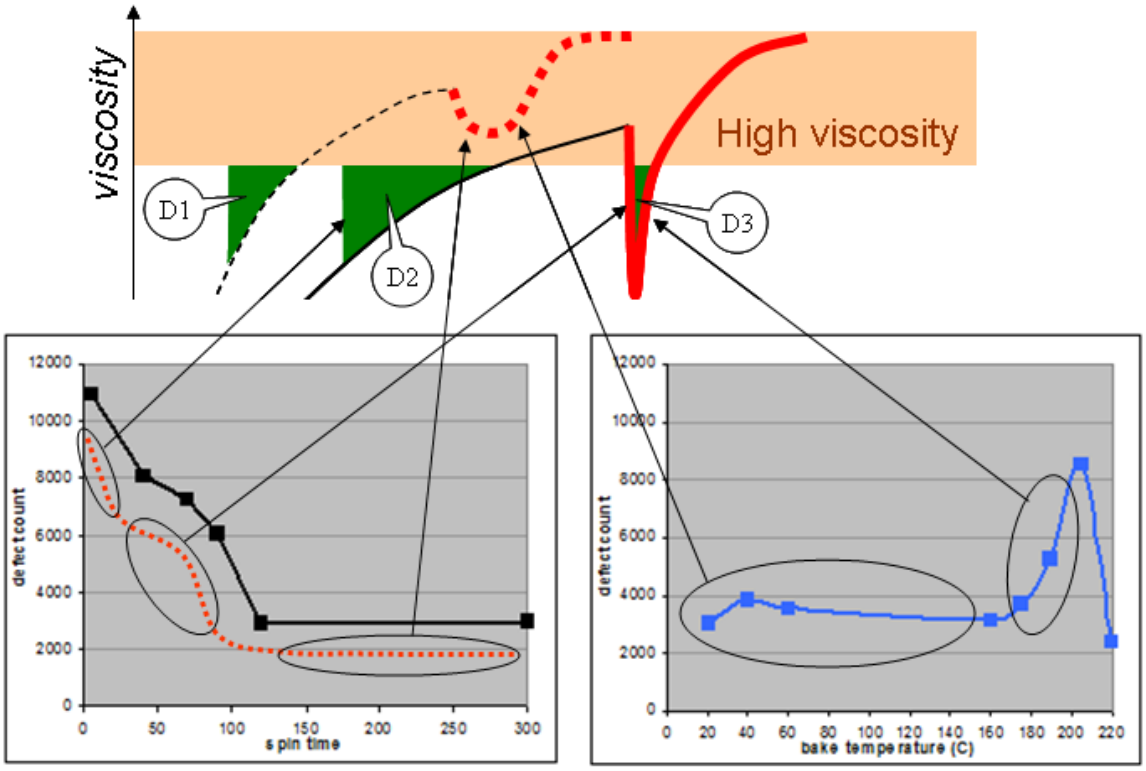


Figure 2. *Defect count plots from* ***Table 1****. Spin time test data (wafers 1~6) are plotted on the left; the red dashed line is a theoretical curve. Bake temperature test data (wafers 7~14) are on the right.*

The bottom left chart of ***Figure 2*** shows the defect count with respect to spin time. The red dot is a theoretical curve fit to the experimental data. When spin time is very short, before the first inflection point, the material is not completely dry and is still at low viscosity. This leads to a wide time window available for potential defect formation. In this section, high defect counts are expected as both precipitation and bake reflow are contributing to the defect formation. In the second section of the curve, between the first and second inflection points, the baking reflow (D3) is the main contributor of defects. The longer the spin time, the dryer the film will be before hot plate baking, and defects will be reduced because of the shorter time window available for defect generation. Therefore the defect count drops sharply with the spin time. When spin time is longer than the second inflection point, the film is dry enough to prevent baking reflow. The defect count converges or saturates to a baseline value, as indicated for wafers 6 and 7 in ***Table 1***, where the net defect count is the same when spin time is increased from 120 to 300 seconds. The spin speed effect is further demonstrated in **Experiment II**, as the baseline is shifted to lower defects due to an increase in spin speed.

The bottom right plot of ***Figure 2*** is the defect count with respect to bake temperature. Lower bake temperatures ranging from 20°C to 160°C give slightly higher defect count, which may be due to the longer reflow time window at low bake temperature. However, the first temperature point is an exception, as it was spun for a much longer time, thus making that film drier than the other wafers on the curve before hot plate bake. At a high

temperature range, 160°C to 200°C, defects increase with temperature, which could be caused by the deeper reflow at higher temperature. The last data point, a 220°C bake, indicates a significant drop in defect count, which means alternate phenomena may be occurring once the material reaches a certain temperature. The drop in defect count may due to a chemical reaction that reduces or mitigates some gel defects after formation.

Experiment II

The same Si-HM material was coated on top of a spin-on carbon (SOC) film 300 nm thick. The coated wafers were scanned with a Hitachi LS Series surface scanning inspection system (SSIS), and the reported defects were reviewed by an RS5500 defect review scanning electron microscope (DRSEM). The defect size and sensitivity was calibrated with a set of polystyrene latex (PSL) spheres (33, 40, 46, 60, 73, 81, 97, 151, 199, 299, and 499 nm in size). The haze level of such a dual-layer stack has a reported defect resolution of about 55 nm.[4]

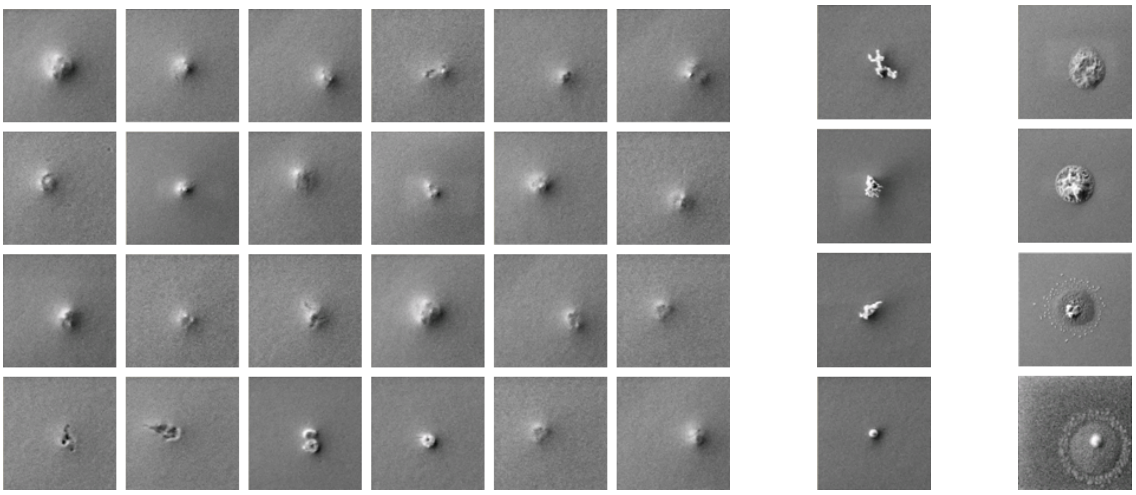
Table 2 details the test plan and the results. The trend of the total defect count agrees with the theory, that is, a longer spin time gives a lower defect count. It is even more significant to reduce defect count by increasing spin speed to make material dry faster, which reduces defect formation time window D1 or D2 in ***Figure 1***. Faster spinning produces a thinner film, which may further reduce defect count due to less material participating in defect formation. However, the dry fast is the major contribution to the defect reduction, as high spin speed reduces the intrinsic defect count by 68% while the thickness shrinkage is only 27% calculated from ***Table 2***. For each wafer, about 5% of the total defect counts were reviewed by the RS5500, with the defect types classified in the table.

Table 2. *Test plan and results*

rpm	film thickness	spin time	total defects	intrinsic defects	foreign defects	
			x1000	embedded	particle	SOC
1500	30 nm	8 s	**20.8**	93.7%	5.6%	0.7%
1500	30 nm	8 s	**21.8**	94.2%	5.3%	0.5%
1500	30 nm	60 s	**19.5**	94.4%	4.9%	0.8%
1500	30 nm	60 s	**18.2**	95.0%	3.4%	1.7%
2500	22 nm	8 s	**12.2**	90.0%	9.0%	1.0%
2500	22 nm	8 s	**10.7**	90.4%	8.6%	1.0%
2500	22 nm	60 s	**7.9**	83.6%	14.9%	1.5%
2500	22 nm	60 s	**7.8**	80.5%	17.0%	2.5%
			average:	**90.21%**	**8.59%**	**1.20%**

The SEM pictures are shown in ***Figure 3***. Embedded defects are the most common Si-HM defect. To simplify the discussion, embedded defects are assumed to be the intrinsic defects in Si-HMs. "Foreign defects" are the defect types that are not generated from the Si-HM. ***Table 3*** summarizes the intrinsic and foreign defect counts. From these data, we can see that the process of long spin time and high spin speed improve the

intrinsic defect count rather than the foreign defect count. High spin speed reduces the defect count baseline in the bottom right plot of ***Figure 2***.



(a) embedded (b) particles (c) SOC

Figure 3. *Defect patterns of different types from classification: (a) embedded defects from Si-HM – the size is distributed within 70~200 nm; (b) particles considered as foreign defects; (c) larger defects found on SOC coating.*

Table 3. *Summary of intrinsic and foreign defects*

rpm	film thickness	spin time	intrinsic defects	foreign defects
1500	30 nm	8 s	19480	1320
1500	30 nm	8 s	20527	1273
1500	30 nm	60 s	18402	1098
1500	30 nm	60 s	17285	915
2500	22 nm	8 s	10982	1218
2500	22 nm	8 s	9675	1025
2500	22 nm	60 s	6604	1296
2500	22 nm	60 s	6279	1521

Experiment III

Pit defects are another intrinsic defect of a Si-HM material. They are generated during hot plate baking, where bubbles are generated under high temperature and are broken by reflow. A pit defect appears as a smooth circular dent, as shown in ***Figure 4***. In most cases, the sizes of such defects are too small to be detected with a defect scanner. They can be found in SEM pictures when the defect counts are over tens of billions per wafer.

The viscosity curve during the baking process indicates what determines pit defect formation. ***Figure 4*** is SEM pictures of four wafers that underwent different processing conditions. The first one had a shorter spin time of 15 s, and baking while wet produced larger pit defects. From these four pictures, we can see the longer the spin time, or the drier the film before bake, the smaller the defect size. The pit defects had almost disappeared in the third picture, where an extremely high spin speed of 4500 rpm for 300 s was applied. The last wafer was soft baked at 130°C for 1 minute before a 205°C bake. The pit defects were completely eliminated.

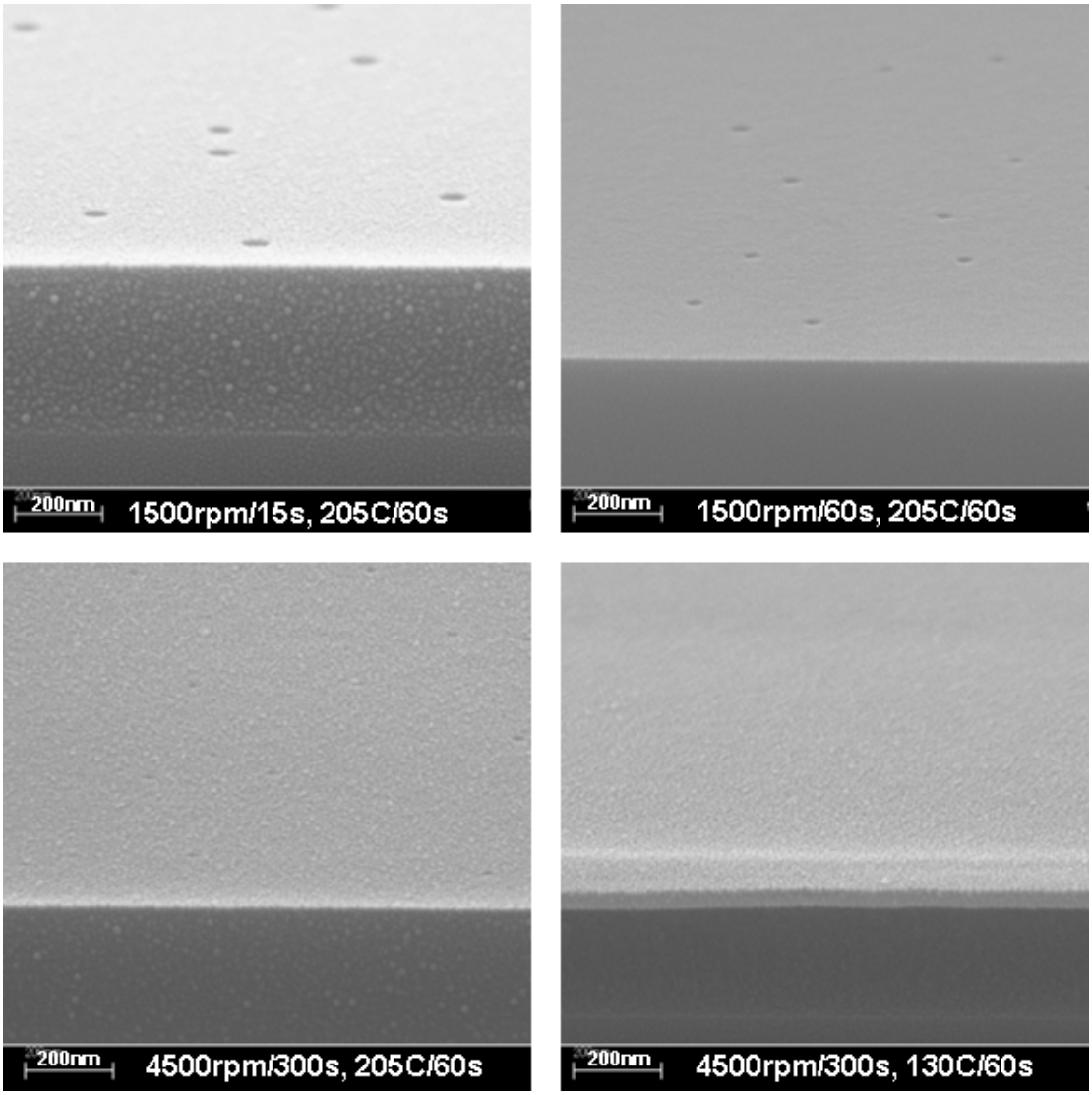


Figure 4. *Pit defect SEM pictures, with different wafer processing conditions. The drier the material after spinning, and the less reflow upon baking, the smaller the defect size. Pit defects can be completely eliminated when a film is dry enough to prevent reflow.*

Discussion

In the context of this theory, material solubility is the basis of material defect performance. We would like materials that retain good solubility at high viscosity. In other words, the precipitation could happen only when the viscosity is high enough to prevent the molecules from migrating to make defects.

Intrinsic defects have been shown to be controlled by spin-coating and baking processes. Material defect characterization and development could be done under conditions that force high intrinsic defect counts for high sensitivity. Higher intrinsic defect counts would allow us to ignore the effects of environmental contamination and give more statistical confidence. This theory could also be used as a guideline to design material processing procedures that produce low defects. ***Figure 4*** shows the best performance of Si-HM with a low defect count ~10 over an 8-inch wafer scanned by SP2 with a resolution of ~70 nm.

According to the assumptions in this paper, intrinsic defects are generated due to multiple phases during precipitation. The impurity in the material would be the defect seeds that first start precipitation. It could also be possible to remove these impurities by precipitation before the final filter.

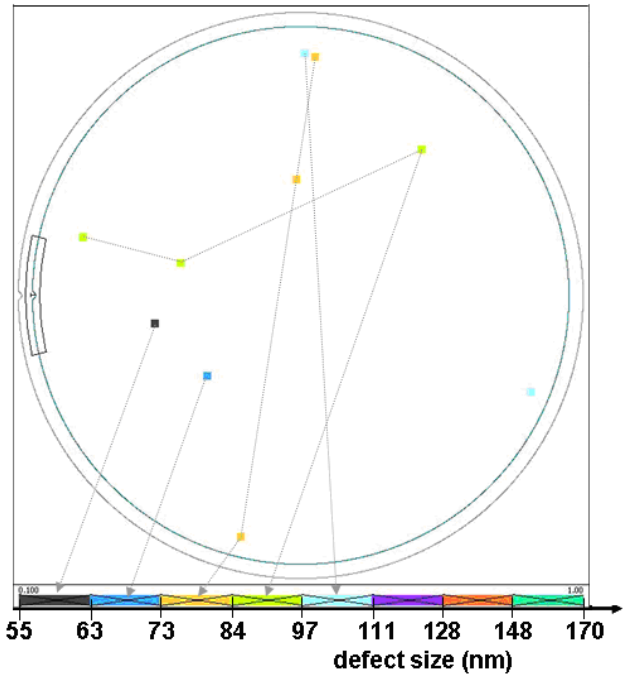


Figure 4. *Defect map of 8-inch wafer, scanned by SP2 in a class 100 clean room. The coated film is Si-HM material.*

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