QuickLogic PolarPro 3 Versus Lattice iCE40 Logic Cell Utilization

Introduction

With the immergence of low-power programmable devices, designers have grappled with how to save power and silicon space while still maximizing logic cell utilization. Complicating the issue is that logic cells from different vendors have different components and configurations. Additionally, naming conventions can differ as some vendors refer to each set of components as a logic cell, slice, or logic element. Essentially, a set of components, referred to as a logic cell, consist of a look up table, flip-flops and muxes. In the case of QuickLogic's PolarPro 3 and 3E solution platforms (where the logic cells are identical) and Lattice's iCE40 family of devices, the logic cells each consist of a 4-input Look-Up Table (LUT), a flip-flop, and a few muxes. However, they perform differently with respect to how much logic can be implemented within each cell. While the logic cell architectures from the QuickLogic PolarPro 3 & PolarPro 3E families of devices and the Lattice iCE40 family have similar configurations, and both have what can be considered 4-LUTs, their effective utilization of resources differ.

Logic Cell Configuration

Before looking at the results, it is important to understand why the PolarPro 3 and 3E logic cell is more efficiently designed than the Lattice iCE40 logic cell. **Figure 1** shows the architecture of the two logic cell types.

Figure 1: Logic Cell Architectures

QuickLogic PolarPro 3/3E Logic Cell

Lattice iCE40 Logic Cell
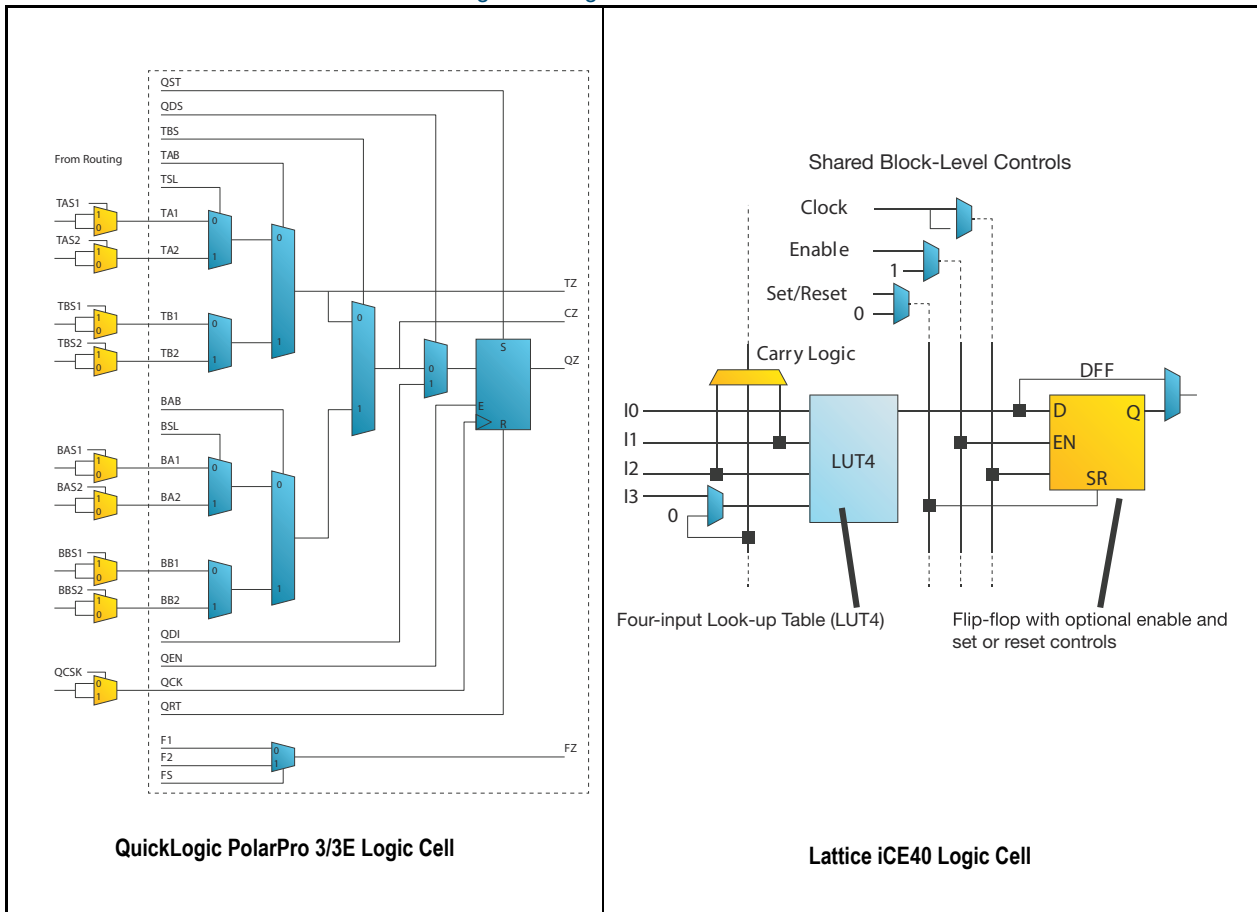
QuickLogic's PolarPro 3 and 3E families feature the unique ability to implement two independent 3-input LUTs or a single 4-input LUT from a single logic cell. Typical programmable fabric logic cells only contain a single 4-input LUT. **Figure 2** shows how a single logic cell in the PolarPro 3 or 3E device can actually perform multiple LUT functions and in multiple configurations, whereas a Lattice iCE40 logic cell can only perform a single LUT function.

Figure 2: Logic Cell LUT Configurations
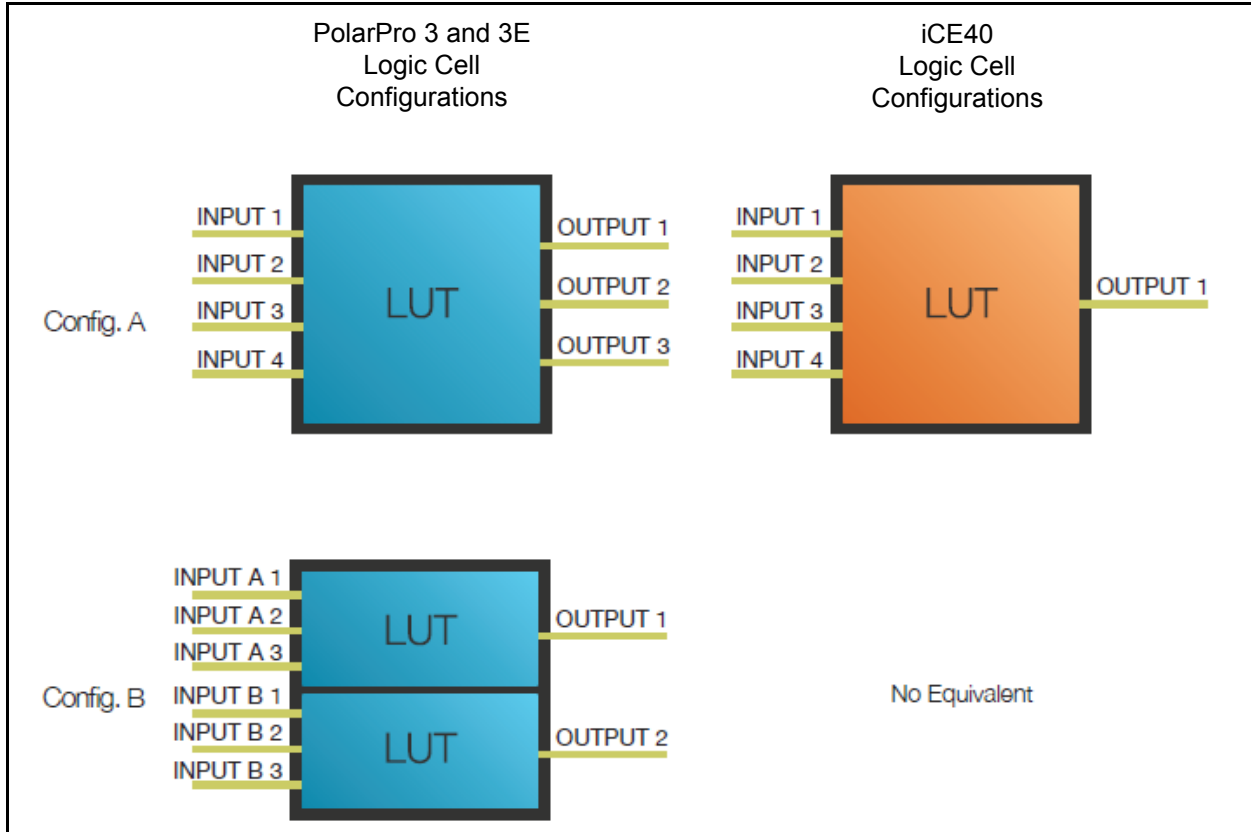
QuickLogic PolarPro 3 & 3E Logic Cell Flexibility

The PolarPro 3 and 3E families also add the flexibility for the flip-flop input signal to be routed from the logic cell or general routing. The iCE40 logic cell flip-flop input can only be routed from the output of the 4-input LUT block. This means that resources are taken up within the LUT just to route a signal to the data input of a flip-flop. In the case of the PolarPro 3 and 3E, the majority of the logic cell resources are still available even if the flip-flop is used. The advantage can clearly be seen in **Figure 3**, which shows the utilized paths in red, and the available resources circled in green.

Figure 3: Available Logic When Flip-Flop is Used

QuickLogic PolarPro 3/3E Logic Cell

Lattice iCE40 Logic Cell
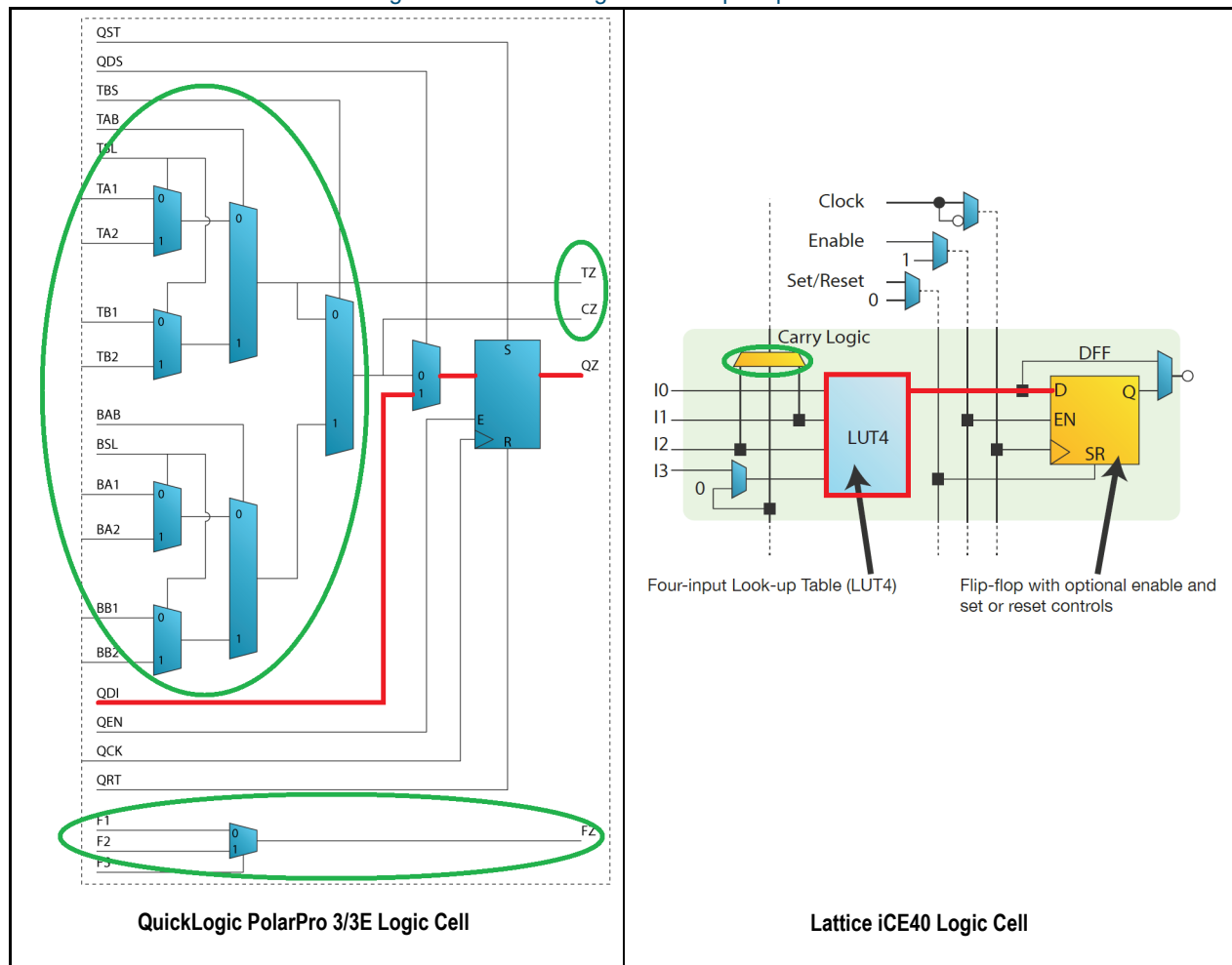
The PolarPro 3 and 3E also allows the combinatorial and registered logic outputs to be used separately. Conversely, the iCE40 logic cell flip-flops can only output the registered or non-registered LUT output, since both are not available at the same time.

Additionally, PolarPro 3 and 3E have the option to output many different levels of the combinatorial logic to the logic cell outputs. **Figure 4** highlights the various output paths within the PolarPro 3/3E logic cell, which are available to general purpose routing. In an iCE40 logic cell, only the carry logic and LUT output are available for routing to other logic cells.

Figure 4: Output Options

QuickLogic PolarPro /3E Logic Cell

Lattice iCE40 Logic Cell
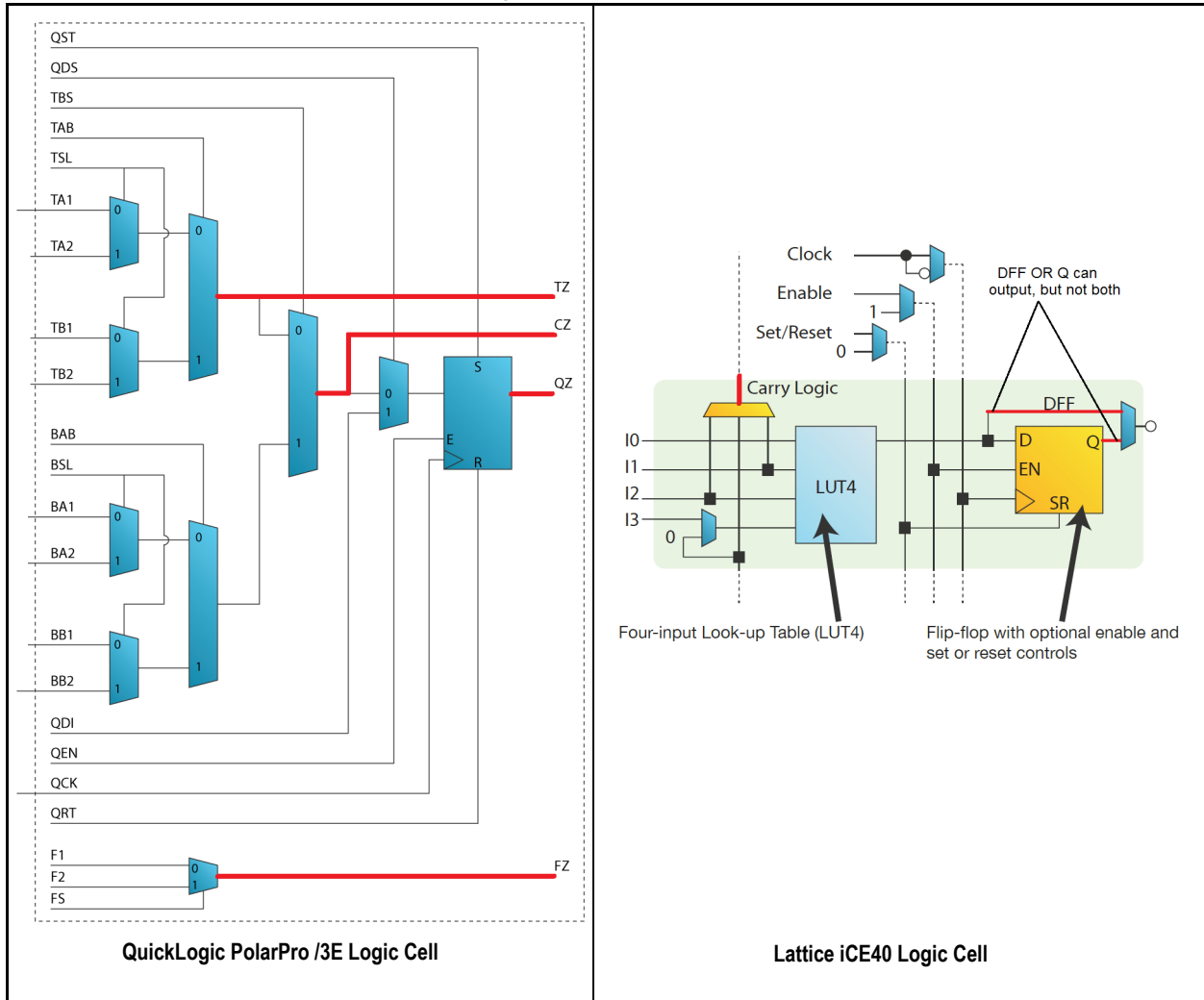
Consequently, because QuickLogic's logic cells are more flexible, designers can fit more functionality into a smaller amount of logic cells, or implement the same functions in a lot fewer logic cells. In fact, in typical implementations, the PolarPro 3 and 3E families have been benchmarked to use available resources twice as efficiently as competing logic cell architectures.

Example Designs Testing Logic Cell Utilization

In general, a PolarPro 3 or 3E device can achieve almost twice as much functionality in the same number of logic cells as an iCE40 device. To fairly compare the utilization performance equally between the two different logic cell architectures, generically written HDL code was chosen. This means that no macros that were specifically made for either family of devices were chosen. Likewise, with the exception of RAM block instantiations, the HDL code is the exactly the same for the PolarPro 3 and the corresponding iCE40 designs. Using the same HDL code with no device-specific macros ensures that neither architecture is favored.

Additionally, an assortment of design sizes and complexities were chosen to give a wider sample set of design types. The following designs were tested:

- Clock Divider — Digital clock divider, with control registers for configurable frequency division.

- Multipler — Basic 11-bit x 11-bit multipler (see appendix for source code)

- Integrated Interchip Sound/Pulse-code modulation (I2S/PCM) Bridge — High performance, low power design connecting a Qualcomm modem processor via I2S for digital audio to a SiliconLab subscriber line interface circuit (SLIC) for telephone communication via a PCM interface.

- 16550 Universal Asynchronous Receiver/Transmitter (UART) — Standard serial communications interface for multifunction I/O solutions. Serial to parallel, and parallel to serial conversion, Baud rate generator, interrupt controller, and internal buffering.

- Managed NAND Flash Controller — Memory interface controller for nonvolatile storage and communication. Programmable block size, interrupt generation, applications processor interface, and error-correcting code.

The QuickLogic PolarPro 3 designs were generated using QuickLogic's SpDE tool version 2013.1.2 as shown in **Figure 5**. The Lattice iCE40 designs were generated using Lattice's iCECube2, release 2013.3.23358 as shown in **Figure 6**. PolarPro 3 designs were targeted to the CSSP-CDPDN64. iCE40 designs were targeted to the iCE40LP1K-CM121.

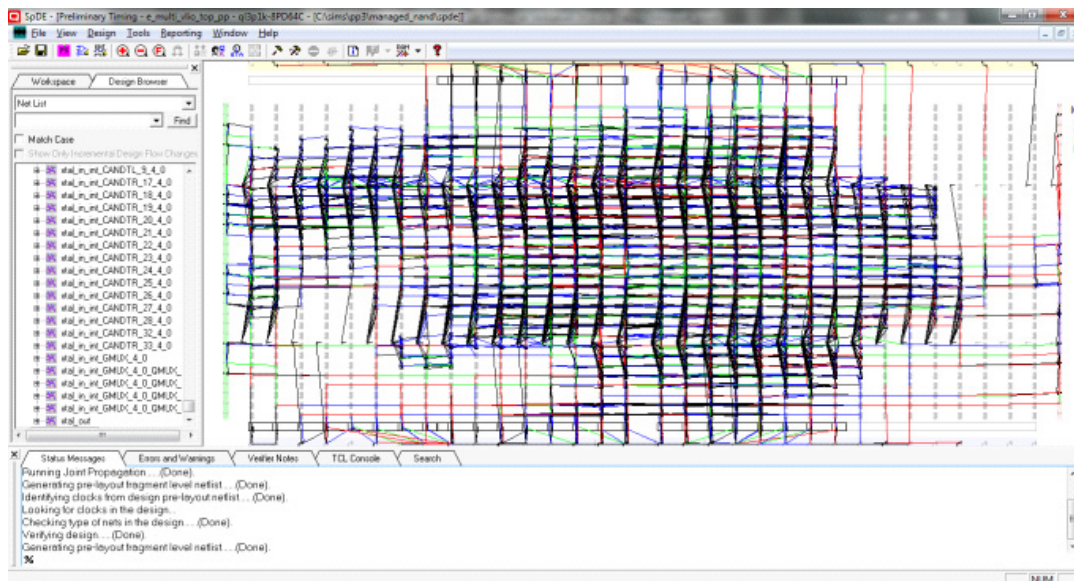Figure 5: SpDE 2013.1.2 Design Software Screen Capture

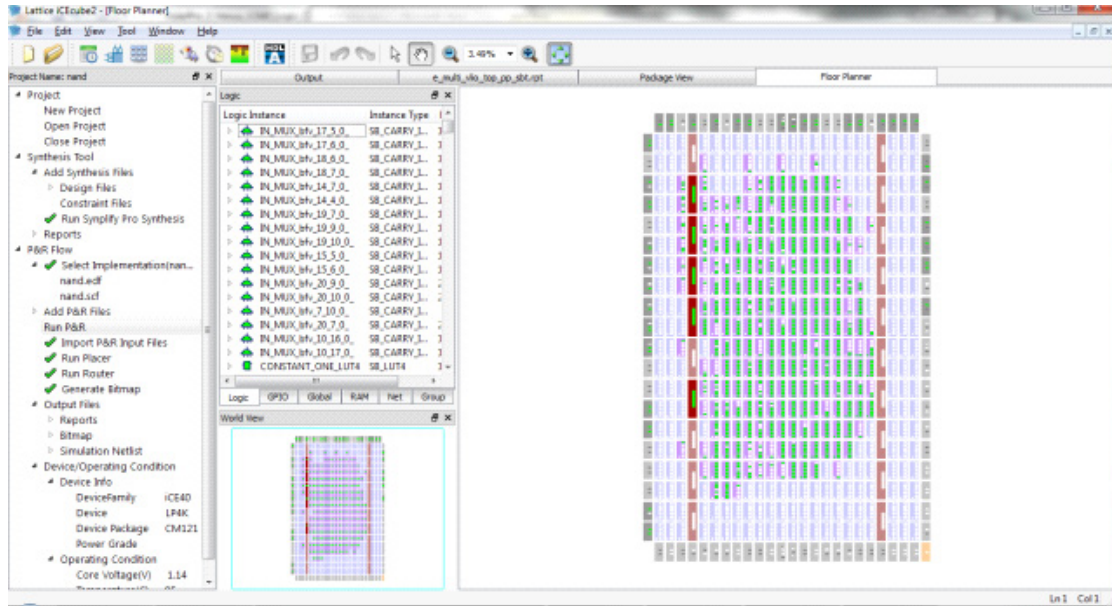Figure 6: iCE40 2013.3.23358 Design Software Screen Capture

Table 1 shows the resulting logic cell utilization for each design.

Table 1: Utilization Testing Results

Design	iCE40 Logic Cells Utilized	PolarPro 3 Logic Cells Utilized	PolarPro 3 Effective Logic Cells
Clock Divider	77	31	56.9% fewer logic cells
I2S/PCM Bridge	104	57	45.2% fewer logic cells
Multiplier 11-bit x 11-bit	280	127	54.6% fewer logic cells
16550 UART	542	233	57.0% fewer logic cells
Managed NAND Flash Controller	1370[a]	570	58.4% fewer logic cells

a. Since the iCE40 design required more than 1280 logic cells, it did not fit in an iCE40 LP1K. Therefore, the design needed to be targeted to the larger iCE40 LP4K.

Conclusion

As can be seen from the test results between the QuickLogic PolarPro 3 and the Lattice iCE40 family of devices, the PolarPro 3 outperforms the iCE40 in efficient use of logic by nearly twice as much over a diverse range of design sizes and complexities. In the case of the Managed NAND Flash Controller design, the required logic could not fit in the iCE40 LP1K, so the design had to be ported to a larger device to fit.

While not shown, the PolarPro 3E expands on this advantage through the use of embedded system blocks. The following embedded system blocks are present in the PolarPro 3E:

• SRAM and FIFO controllers

- I2C and SPI Interfaces

- Dual 32 x 32 multipliers

These embedded system blocks are commonly found in mobile programmable logic designs, taking up valuable fabric space. By implementing these commonly used blocks in hard logic rather than programmable fabric, additional space is freed up for design, increasingly the logic cell efficiency.

Appendix

Verilog source code for the Multipler design:

```
module mult_11x11 (a, b, mult_out);

    input  [10:0] a;
    input  [10:0] b;
    output [21:0] mult_out;

    assign mult_out = a * b;

endmodule
```

Contact Information

Phone: (408) 990-4000 (US)
        +(44) 1932-21-3160 (Europe)
        +(886) 26-603-8948 (Taiwan)
        +(86) 21-2116-0532 (China)
        +(81) 3-5875-0547 (Japan)
        +(82) 31-601-4225 (Korea)
E-mail: info@quicklogic.com
Sales: America-sales@quicklogic.com
         Europe-sales@quicklogic.com
         Asia-sales@quicklogic.com
         Korea-sales@quicklogic.com
         Japan-sales@quicklogic.com
Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
A	January 2014	Jason Lew and Kathleen Bylsma
B	February 2015	Paul Karazuba -- Update for PolarPro 3E

Notice of Disclaimer

QuickLogic is providing this design, product or intellectual property "as is." By providing the design, product or intellectual property as one possible implementation of your desired system-level feature, application, or standard, QuickLogic makes no representation that this implementation is free from any claims of infringement and any implied warranties of merchantability or fitness for a particular purpose. You are responsible for obtaining any rights you may require for your system implementation. QuickLogic shall not be liable for any damages arising out of or in connection with the use of the design, product or intellectual property including liability for lost profit, business interruption, or any other damages whatsoever. QuickLogic products are not designed for use in life-support equipment or applications that would cause a life-threatening situation if any such products failed. Do not use QuickLogic products in these types of equipment or applications.

QuickLogic does not assume any liability for errors which may appear in this document. However, QuickLogic attempts to notify customers of such errors. QuickLogic retains the right to make changes to either the documentation, specification, or product without notice. Verify with QuickLogic that you have the latest specifications before finalizing a product design.

Copyright and Trademark Information