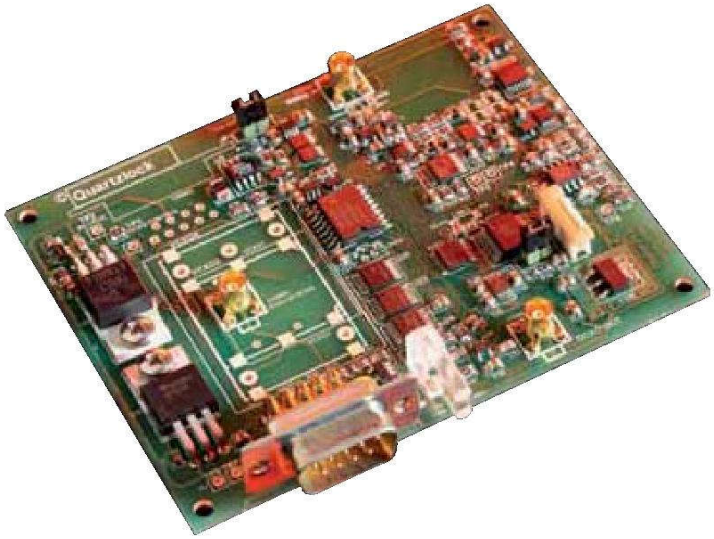
Quartzlock A6-CPS

DPLL, DDS Active Noise Filter

- 1MHz to 40MHz output frequency
- 4mHz to 500mHz PLL bandwidths
- Compact OEM board for a wide range of applications



The A6-CPS digital phase locked loop (PLL) provides an low noise, very high short term stability filtered output which can be customised to a specific application.
The A6-CPS digital PLL may be fitted into the Quartzlock A6 frequency convertor with BVA OCXO, rubidium, GPS or other options.

Features

- RS232 MONITOR AND CONTROL
- Pre-defined user bandwidths
- Wide range of OCXO supported

Benefits

- Improved phase noise
- Improved short term stability
- Low cost solution to upgrade existing designs and reference
- Quick and simple to use and install

Applications

- Time and frequency reference for satellite communication ground solution, CDMA, LTE, DTV
- Frequency referencing of interception and monitoring receivers
- Wired and Wireless network synchronization
- Secure communication, C4, defence and R&D
- Radar & navigation systems
- Higher definition in MRI imagining systems

Tel **+44 (0)1444 232 967**

Email **sales@quartzlock.com**
www.quartzlock.com

Technical Description

This module is designed to overcome the disadvantages of narrow band width analog phase lock loops used to lock relatively stable oscillators together, or to generate arbitrary frequencies from a 10MHz reference with good phase noise, freedom from non harmonically related spurii, and good short term stability.

When locking a low noise OCXO to a rubidium reference, for example, the ideal PLL bandwidth will be very much less than 1Hz, probably in the region of 10 to 100mHz.

An analog loop will have a very long time constant integrator, leading to thermal drift, capacitor dielectric absorption, and operational amplifier offset drift. In addition, acquisition time of the loop will be very long, and if there is any frequency error, acquisition may not occur at all. There is also a problem of providing an effective “in lock” indicator to the user, or for use with associated equipment.

The digital loop overcomes all these problems. The long time constant integrator is replaced by a digital integrator that does not drift at all. A combination of an analog phase detector for low noise, and an extended range phase/frequency detector for certain acquisition can be used. The loop bandwidth can be set to maximum for acquisition, followed by glitch free reduction to the working bandwidth when the phase error becomes small. In addition performance measures related to the phase error in the loop, and the frequency error can easily be derived and used to indicate lock and bandwidth control.
As an additional benefit a hold over mode that keeps the controlled oscillator tuning voltage constant if there should be a reference failure can be easily provided.

In order to generate arbitrary frequencies from a 10MHz reference, a DDS synthesiser is used. This has 36 bit resolution and is clocked at 10MHz from the reference. Output frequencies of 1.8MHz to 3.6MHz are available

as the reference input to the digital PLL. This enables the controlled oscillator (OCXO) to have a frequency range of 1.8MHz to 28.8MHz. The resolution at 10MHz output will be 1.45x10-11.

Technical details of design

The design uses mixer type phase detectors operating at frequencies between 1.8MHz and 10MHz. A dual phase detector is used with quadrature square wave inputs from the controlled oscillator. The main input , which is split between the quadrature phase detectors, is a sine wave input at a level between 0 and 13dBm, and is link selected to either come from the 10MHz reference input, or the output of the DDS synthesiser.

The sine wave signal from the controlled oscillator is converted to a square wave using a fast comparator. It is then divided by 2, 4 or 8 using digital dividers. A link selects direct, 2,4, or 8 divided signals.

The output from the dividers forms the “Q” reference signal to the Q phase detector. A quadrature “I” reference is generated by passing the Q signal through a programmable delay line, which may be set to delays from 10ns to 137ns, in steps of 0.5ns. This enables quadrature references to be generated for phase detector frequencies between 1.8MHz and 25MHz.

The outputs from the phase detectors are filtered and amplified by DC amplifiers with gain control using digital potentiometers. The gain is controlled by a software AGC system which tries to keep the input to the ADCs at optimum levels. The phase detector outputs are sampled by two channels of the 10bit AtoD convertor internal to the PIC 16F689 microcontroller. All other functions of the PLL are carried out by software.

The control of the OCXO or other controlled oscillator uses a precision tuning voltage derived from DtoA convertors . Two 16 bit DACs are used, with the output of the fine tune DAC divided by 256 and added to the output of the coarse tune DAC. This gives effectively 24 bit resolution with an overlap between the coarse and fine tune DACs. A software normalisation process ensures that the fine tune DAC is used for tuning most of the time. Only when the controlled oscillator has drifted out of range of the fine tune DAC would the coarse tune DAC need adjusting, with the chance of a very small glitch in the tuning voltage. A precision, low noise, voltage reference is used to supply the DACs.

The microcontroller is provided with an RS232 interface. A simple set of control codes enable monitoring and set up of the digital PLL parameters to accomodate a wide range of controlled oscillators. A Windows front end program will use the control codes to enable the operation of the PLL to be monitored with real time graphs of performance measures.

Software design

The input to the software is the sampled I and Q signals from the phase detectors. These are sampled at a 1kHz rate. As the final bandwidth of the PLL will be less than 1Hz, this oversampling enables prefiltering to be used which extends the resolution and reduces noise in the 10bit AtoD convertor internal to the microcontroller. Single pole digital filters are used on both the I and Q channels. These are implemented as exponential filters which have a 3dB band width which is a function of the “order” of the filter. Filter orders between 0 (no filter) and 15 are provided. This gives bandwidths between 114Hz for order 1, and 4.8mHz for order 15. The filter order is varied as the user selected PLL bandwidth is varied.

After prefiltering, the I and Q channels, now at 16 bit resolution, are subsampled at a rate between 15.625 s/s, and 1.953 s/s depending on the user bandwidth and lock state of the PLL. The “Q” sample is now divided by the ”I” sample (after checking that I>Q) to give a binary fraction. This is used to look up the phase value in a TAN-1 look up table. The look up table is used to synthesise two types of phase detector:

a) A phase detector with 16 bit resolution between Pi/2 and -Pi/2.

b) A phase/ frequency detector with 16 bit resolution between 2Pi and -2Pi. This phase detector is equivalent to the well known digital phase/frequency detector. This rolls over between 2Pi and 0 for positive cycle slips, and between -2Pi and 0 for negative cycle slips, and will always provide reliable lock if there is a initial frequency error.

The output of the selected phase detector now has digital gain applied, selectable between 1/256 and 128. After digital gain, the phase value is added into the integrator, which is 32 bits wide.

In order to make the loop stable, by providing a phase lead, the phase value has proportional term gain applied, also selectable between 1/256 and 128. This value is added to the upper 3 bytes of the integrator to give the tuning voltage (24 bits)

The tuning voltage is divided between the coarse and fine tune DACs as follows: When normalisation is performed, the fine tune DAC most significant 8 bits are set to mid point (80h). The least significant 8 bits of the fine tune DAC are set to the least significant 8 bits of the tuning word. The coarse tune DAC is then set to provide the final tuning voltage. During all subsequent tuning, only the fine tune DAC is used over its 16 bit range. If the range is exceeded, the normalisation procedure is repeated. A state machine provides control of locking. After reset the last value of the integrator, which has been stored in EEPROM on a regular basis, is restored. This will retune the controlled oscillator to very nearly the correct frequency. The loop is then opened and the software waits for the following all to occur (state 0):

a) Rubidium reference warm up input to go high.

b) OCXO supply current to drop below a threshold showing the OCXO has warmed up

c) A measure |I|+|Q| which is an approximate measure of the signal level at the phase detector to rise above a threshold.

When these conditions are fulfilled, the software attempts to lock the loop (state 1) by selecting the phase frequency detector, maximum bandwidth, and maximum subsample rate. It then closes the loop and waits for another measure, which is |phaseresult|, to drop below a threshold. The measure |phaseresult| is the modulus of each phase calculation filtered in an 8th order exponential filter, the bandwidth of which, for the 15.625 s/s subsample rate, equals 9.7mHz.

Once the lock threshold for |phaseresult| is reached, the lock state (state 2) is entered. The bandwidth is switched to the users selected bandwidth, which has been maintained in EEPROM, and the phase detector is switched over to the narrow band phase detector (Pi/2 to -Pi/2). All the time during normal operation , |phaseresult| is being compared to a lower threshold than the lock threshold. If it exceeds this threshold, state 3 is entered which provides a brief flash of the lock LED to warn the user that the selected bandwidth may be too narrow for the PLL to track the drift of the controlled oscillator fast enough. This low threshold is currently set at 480ps maximum phase error.

In extreme cases the lock threshold (4.8ns phase error) may be exceeded, in which case the software assumes lock is lost and re-enters state 1. A further performance measure is calculated, which is available over the interface. This is the first difference of the phase error, filtered in an 8th order exponential filter. It is corrected for subsample rate, and has a constant sensitivity of 5.8x10-15 per bit. (at 10MHz phase detector frequency)

This performance measure gives the mean fractional frequency difference between the controlled oscillator and the reference, and is useful for setting up the optimum bandwidth of the PLL.

The band width and damping of the PLL is controlled by 4 parameters, integrator digital gain, proportional digital gain, prefilter order, and subsample rate. These are preset for 8 values of user selected bandwidth, and can only be changed by modifying the software. It is possible to temporarily adjust the four individual parameters as part of a test procedure carried out over the RS232 interface. The selection of the 4 parameters has been optimised using a mathematical model of the PLL modelled as a MATHCAD spreadsheet. This could be made available to customers who wished to readjust the PLL parameters.

Specification

Reference Input		
Frequency	10MHz	(DDS used)
	1MHz to 10 MHz	(no DDS)
Level	100mVPP to 5VPP	(DDS used)
	1VPP to 5VPP	(no DDS)
Input Impediance	1000 OHMs	
Controlled Oscillator		
Frequency	1MHz to 40MHz	(no DDS)
	1.8MHz to 28.8MHz	(DDS used)
Level (external oscillator)	100mVPP to 5VPP	
	High end options	Typical option
Phase Noise	-130dBc/Hz @ 1Hz offset	-110dBc/Hz
	-178dBc/Hz @ 10kHz offset	-160dBc/Hz
Stability Allan Variance	$8x10^{-14}$/s	$x10^{-13}$/s
Input Impediance	500 Ohms	
External Tune Voltage	0 to SPAN, where SPAN is software adjustable between 5.8V and 10V	
	Notes: a) If DDS is not used, controlled oscillator must be k times higher frequency than refeence, where k is link adjusted to 1,2,4,8 b) Either reference or controlled oscillator must be 10MHz to provide microcontroller clock	
Power Supply	14 to 30V	on board OCXO is used
	12 to 30V	no on board OCXO
Current Consumption	150mA typical	on board OCXO
	50mA	typical (no on board OCXO)
PLL Bandwidths	4mHz to 500mHz typical in 8 binary increments	
Frequency Pull in	Up to 7Hz initial frequency error	
Lock Indicator	On	Not locked
	Off	Locked, low phase error
	Short flash every second	Locked, high phase error
	Long flash, short flash	No processor clock
Interface	9.6kbaud, RS232, PC compatible, Windows front end program or USB	
Interface Codes	Ask Quartzlock for separate document	
PCB Size	94 x 75mm (may be substantially reduced in customised version). OCXO may mount off PCB.	