SWTEST ASIA

PROBE TODAY, FOR TOMORROW

2019 CONFERENCE

Friday, October 18
Proceedings

Welcome to SWTest Asia 2019

2nd Annual SWTest Asia Conference

On behalf of the SWTest Asia Team it is our great pleasure to welcome you to the Second Annual SWTest Asia EXPO at the Sheraton in Hsinchu, Taiwan. We would like to thank all our sponsors (8-platinum, 8-gold, and 8-silver), the 42 exhibitors, and the committee members as well as the volunteers for their support to make SWTest Asia a valuable event for the Asian wafer test industry.

Last year, the inaugural SWTest Asia Conference drew over 450 attendees with more that 45% of attendees from outside of Taiwan. More than 35% of the registered attendees were key engineers, managers, and decision makers from IDM, Foundry, and OSAT companies.

For 2019, we are pleased to have expanded the conference schedule into a two-day Technical Program with six themed sessions as well as a sold-out EXPO with 42 booths. The top probe card, probe equipment, and related service suppliers will have an opportunity to showcase their latest product offerings and technical services. Our goal with the focused EXPO is to provide our attendees with unprecedented access to the premier suppliers of technologies and services for the wafer test industry.

The popular “Tech Showcase” track will be held during the EXPO hours but will not conflict with the technical session schedule of the conference. SWTest Asia Conference and EXPO is rapidly becoming a must-attend event for the Asia wafer test industry.

New for SWTest Asia 2019, we started the “1st Annual Sponsors and Exhibitors Golf Tournament” to facilitate relaxed technical discussions, networking, and support our student travel grant awards.

Once again, thank you for being a part of the 2nd Annual SWTest Asia Conference and EXPO; and we hope that you enjoy your time in Taiwan and the Hsinchu area.

Jerry Broz, Ph.D.
General Chair
SWTest Asia

Clark Liu
Program Chair
SWTest Asia

Rey Rincon
Technical Program Co-Chair
SWTest Asia

Maddie Harwood
Finance Chair &
Conference Management
SWTest Asia

2019
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Conference

SWTEST ASIA
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PROGRAM SCHEDULE

SWTest Asia 2019 - Platinum Sponsors

MPI

international TEST SOLUTIONS

FormFactor™

STAr Technologies

TERADYNE

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PROGRAM SCHEDULE

SWTest Asia 2019 - Gold Sponsors

RUDOLPH TECHNOLOGIES

SEMICS

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HTSi Hermes Testing Solutions Inc.

TECHNOPROBE Wafer Probing Technologies

GLOBAL INNOVATION ISC

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SWTest Asia 2019 - Silver Sponsors

ADVANTEST

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WinWay Technology

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2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

"Program Overview At A Glance"

Day One	Thursday, October 17th, 2019
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Chair's Opening Remarks*** ***Thursday Keynote Presentation in General Session Room*** Prof. Chen-Fu Chien, Ph.D. *Tsinghua Chair Professor & Micron Chair Professor at National Tsing Hua University*
10:15 – 10:45	Tea Break in the Registration Lobby
10:45 – 12:15	**"*Challenges for Next-Gen of Wafer Test*" in General Session Room** Full Conference Only
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions
14:00 – 15:30	**"*Big Data, Big Future*" in General Session Room** Full Conference Only – Expo Open
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall
16:00 – 17:30	**"*Challenges in Process Control Monitoring*" in General Session Room** Full Conference Only – Expo Open
17:30 – 18:30	Welcome Reception in Expo Hall

Day Two	Friday, October 18th, 2019
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Chair's Opening Remarks*** ***Friday Keynote Presentation in General Session Room*** Masahide Ozawa *Technical Consultant* at *Tokyo Electron Technology Solutions*
10:15 – 10:45	Expo Open & Tea Break in the Registration Lobby and Expo Hall
10:45 – 12:15	**"*Full Speed Ahead with 5G Solutions*" in General Session Room** Full Conference Only – Expo Open
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions
14:00 – 15:30	**"*Temperature Handling & Space Transformation*" in General Session Room** Full Conference Only – Expo Open
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall
16:00 – 17:30	**"*Advanced Probing Interface Solutions*" in General Session Room** Full Conference Only – Expo Open
17:30 – 17:45	Presentation Awards Ceremony
17:45 – 18:45	Closing Reception in Expo Hall

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

SWTest Team is proud to announce the 2nd Annual SWTest Asia conference to be held in Hsinchu, Taiwan, October 17-18, 2019. This two-day conference is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas. SWTest Asia promotes a friendly atmosphere with Technical Sessions, an EXPO, and a Tech Showcase, as well as our signature relaxed environment for "informal discussion and networking".

This event attracts attendees from the local and regional semiconductor industry that include ASE, TSMC, Ardentec, KYEC, SPIL, Micron, ChipMOS, UMC, Winbond, PTI, and more. Visitors to the conference will come from Japan, Korea, China, Singapore, India, Philippines, and Malaysia. Conference registration includes all meals, refreshments, social activities, and technical program and exhibit attendance, as well as the eProceedings.

Thursday, October 17th, 2019	
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Welcome to SWTest Asia 2019 – Day 1*** Dr. Jerry Broz, SWTest Asia General Chair Clark Liu, SWTest Asia Technical Program Chair
	Thursday Keynote Presentation ***"Industry 3.5" to Empower Intelligent Manufacturing and Empirical Studies in Taiwan***  **Prof. Chen-Fu Chien, Ph.D.** **Tsinghua Chair Professor & Micron Chair Professor** Department of Industrial Engineering & Engineering Management National Tsing Hua University, Taiwan
10:15 – 10:45	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Thursday Program Overview

Technical Session 1 **10:45 – 12:15**	**Challenges for Next-Gen of Wafer Test** **Session Chair**: Dr. Jerry Broz, General Chair (International Test Solutions)
10:45 – 11:15	**Advanced Packaging — It's Changing The World Of Wafer Test** Amy Leong (FormFactor Inc. – USA)
11:15 – 11:45	**Methodology of VCSEL Probing and Testing** Hector Lin, Douglas Tsai, and Gary Liu (MPI Corporation – Taiwan)
11:45 – 12:15	**Probing Technology Challenge: Now and Future** Clark Liu, Henry Tseng, and Jason Sung (PTI – Taiwan)
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions

Technical Session 2 **14:00 – 15:30**	**Big Data, Big Future** **Session Chair:** Joey Wu (SWTest Member at Large)
14:00 – 14:30	**Wafer Defect Diagnosis With Test Big Data Driven Techniques** Prof. Katherine Shu-Min Li (National Sun Yat-Sen University – Taiwan) Andrew Huang, Chau Cheung Cheng, Chengyen Tsai, Leon Chou, Yi Yu Liao, and Chen Hsun Lee (NXP Semiconductors - Taiwan)
14:30 – 15:00	**Probe Card Electrical Quality Enhancement Using Big Data Analytics** Kenny Huang, Fred Chou, Alex Wei, Steven Wu (MPI Corporation – Taiwan) Ying-Jen Chen (DALab Solutions x Associates Co., Ltd., Taiwan – Taiwan) Yu-Mei Ling, Yi-Yu Chen and Prof. Chen-Fu Chien (National Tsing Hua University – Taiwan)
15:00 – 15:30	**Testing the Spatial Pattern Randomness on Wafer Maps** Prof. Jwu E Chen, Prof. Hsing-Chung Liang, and Tung Ying Lu (National Central University – Taiwan)
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall

Technical Session 3 **16:00 – 17:30**	**Challenges in Process Control Monitoring** **Session Chair:** Nobuhiro Kawamata (FormFactor KK – Japan)
16:00 – 16:30	**Reducing Wafer Parametric Test Costs By High Speed Test Solution** Yu Cheng Su (National Instruments – Taiwan) Mark Lu (Semitronix – China)
16:30 – 17:00	**Advances In Position Measurement And Analysis For Guide Plate Microholes** Michael Cullimore and Dr. Alan Ferguson (Oxford Lasers – United Kingdom)
17:00 – 17:30	**Takumi CL – New 2D-MEMS Spring Introduction to Formfactor Parametric Probe Card and Comparison with 3D MEMS Spring** Takao Saeki (Formfactor KK – Japan)
17:30 – 18:30	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Friday, October 18th, 2019	
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Welcome to SWTest Asia 2019 – Day 2*** Dr. Jerry Broz, SWTest Asia General Chair Clark Liu, SWTest Asia Technical Program Chair
	Friday Keynote Presentation ***Wafer Test Value and Future***  **Masahide Ozawa** **Technical Consultant** Tokyo Electron Technology Solutions - Japan
10:15 – 10:45	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Friday Program Overview	
Technical Session 4 **10:45 – 12:15**	**Full Speed Ahead with 5G Solutions** **Session Chair**: Dr. Jerry Broz, General Chair (International Test Solutions)
10:45 – 11:15	**Getting Ready For The Next Wave Of Growth** John West (VLSI Research Europe – United Kingdom)
11:15 – 11:45	**5G Enhanced Micro-Cantilever Membrane Probing Solutions** Jed Hsu and Jordan Smalls (Translarity, Inc. – USA)
11:45 – 12:15	**How To Successfully Embrace The Era Of 5g Mmwave Test** Yu Cheng Su (National Instruments – Taiwan)
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions

Technical Session 5 **14:00 – 15:30**	**Advanced Thermal Handling & Space Transformation** **Session Chair:** Dr. Alan Ferguson (Oxford Lasers – United Kingdom)
14:00 – 14:30	**Ultra High Temperature Production Probe Card Solution for Automotive IC Testing** Alan Liao (FormFactor – USA) and Hirofumi Nagata (FormFactor – Japan)
14:30 – 15:00	**Space Transforming Probes** Gary Grube and Dominik Schmidt (Translarity Inc. – USA)
15:00 – 15:30	**Temperature Accuracy At High Wattage Wafer Test – A Novel Method To Control Device Temperature** Klemens Reitinger (ERS electronic GmbH – Germany)
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall

Technical Session 6 **16:00 – 17:30**	**Advanced Probing Interface Solutions** **Session Chair:** Clark Liu (PTI – Hsinchu, Taiwan))
16:00 – 16:30	**Overview Of Specialized Testing For Mems Sensors; Wafer Probe & Final Test** Michael Ricci (Rika Denshi Group, LTD – Japan)
16:30 – 17:00	**Innovative Probe Card Analyzer Solutions For Next Generation Probe Cards** John Strom (Rudolph Technologies – USA)
17:00 – 17:30	**A New Framework to Manage Device Interface Complexity For The Next Decade** Steve Ledford (Teradyne – USA)
17:30 – 18:30	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

2019 EXHIBITORS

Advantest
ATT Systems GmbH
Celadon Systems Inc.
Chain-Logic International Corp.
CHPT
Dynamic Test Solutions Asia Pte Ltd.
ERS electronic GmbH
Feinmetall GmbH
Ferrotec Ceramics Corporation
FormFactor
Hermes Testing Solutions Inc.
Hitachi Chemical Co., Ltd.
Integrated Technology Corporation
International Test Solutions
inTEST EMS
ISC Co., Ltd.
IWIN Co., Ltd.
JEM Taiwan Probe Corp.
Laser Job, Inc.
MJC Taiwan
MPI Corporation
Nagase (Taiwan) Co., Ltd.
National Instruments
NHK Spring Co., Ltd.
Nidec SV TCL
Oxford Lasers
PLI Co., Ltd.
Posalux SA
Rudolph Technologies, Inc.
Saehan Microtech
SEMICS Inc.
Shyan Sheng Hitech
Specialty Coating Systems
STAr Technologies, Inc.
T.I.P.S. Messtechnik GmbH
Tanaka Precious Metals
Technoprobe America Inc.
Teradyne, Incorporated
Veco Precision
Wentworth Laboratories Ltd.
WinWay Technology Co., Ltd.
WONIK QnC Corporation

2019

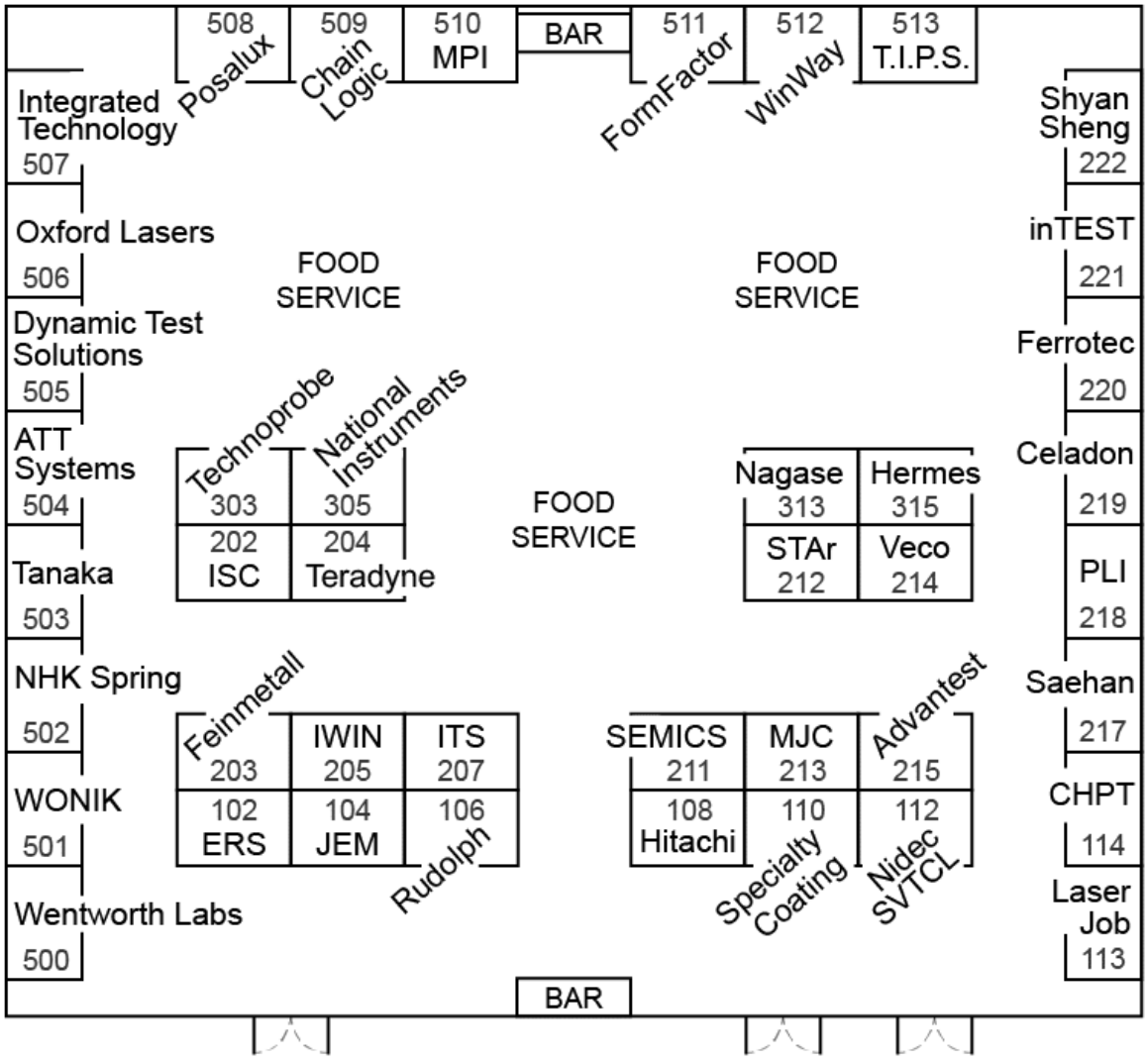
SWTest Asia Conference

SWTEST ASIA

PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

EXPO HALL



2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

3nd Annual SWTest Asia

Coming in October, 2020
(dates will be announced soon!)

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

30th Anniverary SWTest

June 7 to 10, 2020

Rancho Bernardo Inn

San Diego, California

Technical Program
SWTest Asia 2019

Friday, October 18, 2019

Hsinchu, Taiwan, October 17-18, 2019

Friday, October 18, 2019

9:00 to 9:15 – Welcome to SWTest Asia

Dr. Jerry Broz (SWTest Asia General Chair) and Clark Liu (SWTest Program Chair)

9:15 to 10:15 – Keynote Speaker

Wafer Test Value and Future

Masahide Ozawa

Technical Consultant
Tokyo Electron Technology Solutions - Japan

Friday, October 18, 2019

10:45 to 12:15 – Full Speed Ahead with 5G Solutions

Getting Ready For The Next Wave Of Growth

John West (VLSI Research Europe – United Kingdom)

5G Enhanced Micro-Cantilever Membrane Probing Solutions

Jed Hsu and Jordan Smalls (Translarity, Inc. – USA)

How To Successfully Embrace The Era Of 5g Mmwave Test

Yu Cheng Su (National Instruments – Taiwan)

Friday, October 18, 2019

14:00 to 15:30 – Advanced Thermal Handling & Space Transformation

Ultra High Temperature Production Probe Card Solution for Automotive IC Testing

Alan Liao (FormFactor – USA) and Hirofumi Nagata (FormFactor – Japan)

Space Transforming Probes

Gary Grube and Dominik Schmidt (Translarity Inc. – USA)

Temperature Accuracy At High Wattage Wafer Test – A Novel Method To Control Device Temperature

Klemens Reitinger (ERS electronic GmbH – Germany)

Friday, October 18, 2019

16:00 to 17:30 – Advanced Probing Interface Solutions

Overview Of Specialized Testing For Mems Sensors Wafer Probe & Final Test

Michael Ricci (Rika Denshi Group, LTD – Japan)

A New Framework to Manage Device Interface Complexity For The Next Decade

Steve Ledford (Teradyne – USA)

Intelligent Method for Retesting a Wafer

YC Wang and YK Huang (Teslence Technology Co., Ltd)

Technical Program
SWTest Asia 2019

Friday, October 18, 2019

Hsinchu, Taiwan, October 17-18, 2019

Welcome to the 2st Annual SWTest Asia in Taiwan

Jerry Broz, Ph.D.
General Chair, SWTest Asia
International Test Solutions

Clark Liu
Technical Program Chair, SWTest Asia
Powertech Technology, Inc.

Hsinchu, Taiwan, October 17-18, 2019

Welcome to the Sheraton, Hsinchu !

SWTest Asia and SWTest San Diego

- **SWTest Conferences are Probe Technology Forums …**
  - Premier Conferences for Wafer Test Professionals and Probing Technologists.
  - Balanced mixture of manufacturers and suppliers as well as collaborative presentations
  - Practical solutions to real problems that are faced by test engineers

- **Thirty-Two Combined Years of Probe Technology …**
  - 2nd SWTest Asia in Taiwan brings a "workshop style" conference to Asia Semiconductor community.
  - SWTest in San Diego has more than 9500 worldwide attendees to discuss probe technology.

- **Informal and Networking Conferences …**
  - Focused technical exchange
  - Great social activities and informal discussions
  - Meet new people and have a little fun !

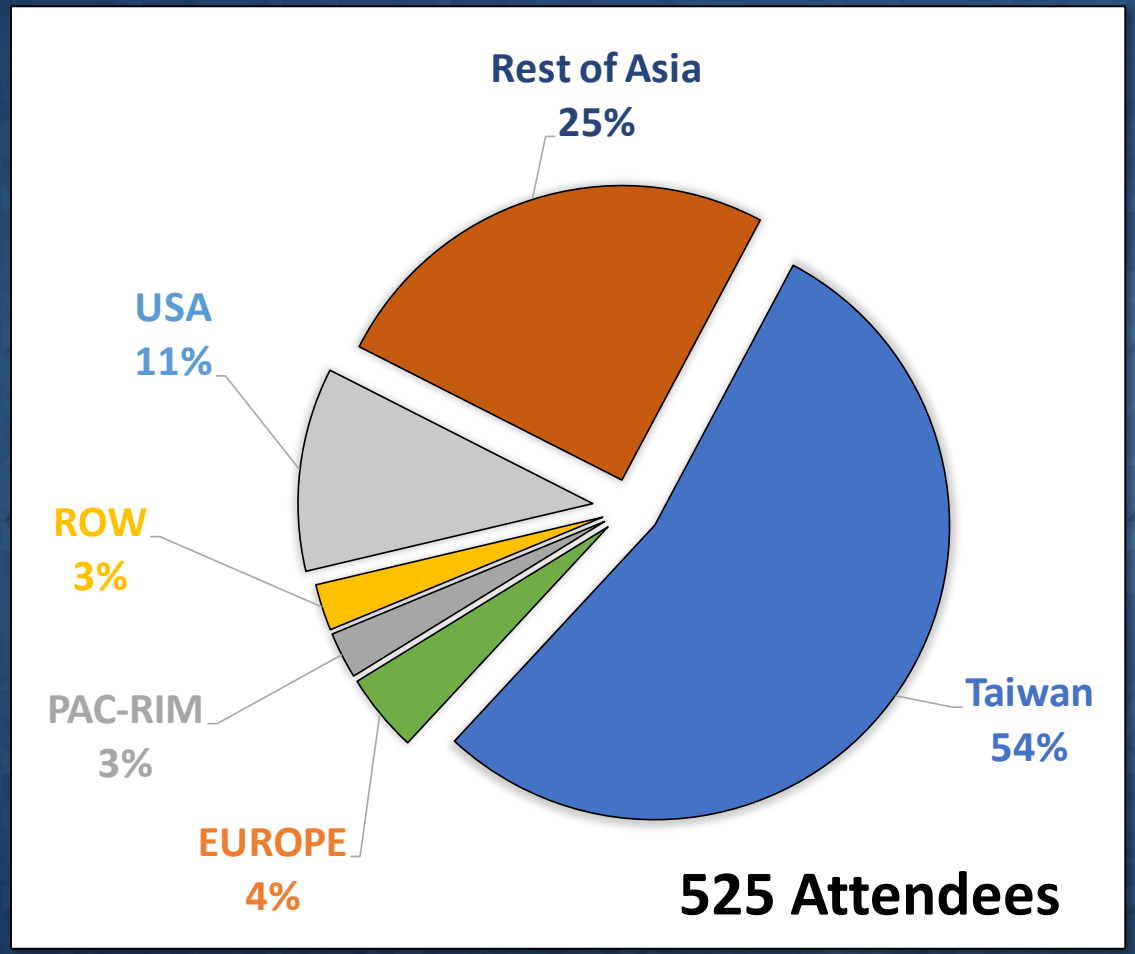
SWTEST ASIA

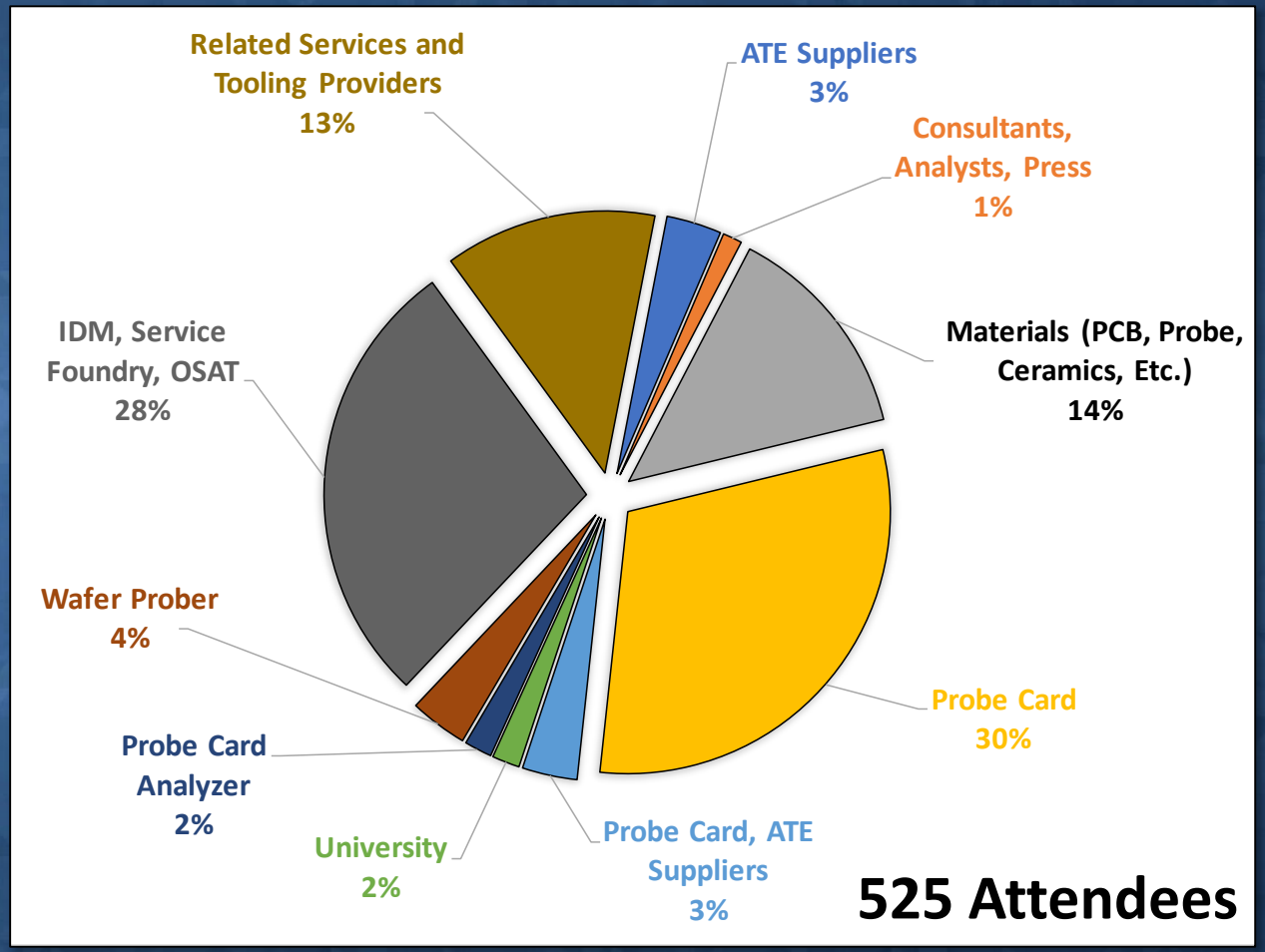
Held During
October
In Asia Region

SWTEST
PROBE TODAY, FOR TOMORROW

Held During
June
In San Diego, CA

SWTest Asia 2019 Demographics





SWTest Asia Chairs and Committee

- **SWTest Asia Chairs**
  - Dr. Jerry Broz, General Chair (International Test Solutions – USA)
  - Clark Liu, SWTest Asia Technical Program Chair (Powertech Technology, Inc. – Taiwan)
  - Rey Rincon, Technical Program Co-Chair (Translarity, Inc. – USA)
  - Maddie Harwood, Finance and Conference Management Chair (SWTest Conferences)

- **SWTest Asia Steering Committee**
  - Nobuhiro Kawamata (Formfactor, K.K. – Japan)
  - Alex Yang (MPI Corporation – Taiwan)
  - Alan Ferguson, Ph.D. (Oxford Lasers, Inc., United Kingdom)
  - Joey Wu (SWTest Member at Large – Taiwan)
  - Haruko Yoshii (Formfactor, K.K. – Japan)

SWTest Asia 1st Annual Benefit Tournament

老爺關西高爾夫球場
Royal Kuan-Hsi Golf Club

Wednesday, October 16, 2019

SWTest Asia 2019 on October 17 to 18, 2019

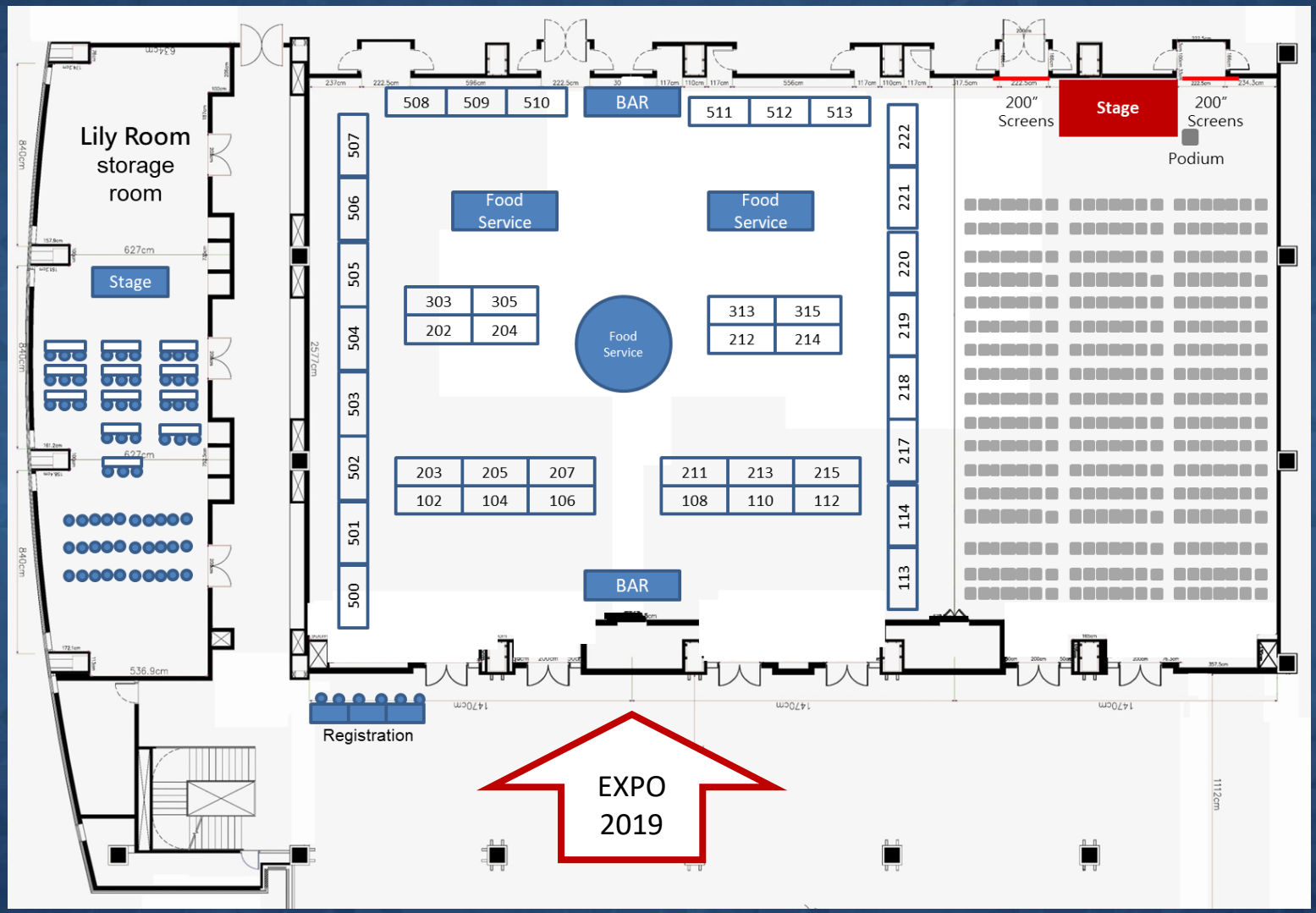
Thursday, October 17

- Keynote from Prof. Chen-Fu Chien, Ph.D., Tsinghua Chair Professor & Micron Chair Professor at National Tsing Hua University
- Technical Program with 3-podium sessions
  - 1045 – 1215: Challenges for Next-Gen of Wafer Test
  - 1400 – 1530: Big Data, Big Future
  - 1600 – 1730: Challenges in Process Control Monitoring
- SWTest Asia EXPO 2019 with 42-key suppliers
- Technology Showcase Presentations by Platinum Sponsors
- Welcome Reception in Expo Hall

Friday, October 18

- Keynote from Masahide Ozawa, Technical Consultant at Tokyo Electron Technology Solutions
- Technical Program with 3-podium sessions
  - 1045 – 1215: Full Speed Ahead with 5G Solutions
  - 1400 – 1530: Advanced Thermal Handling & Space Transformation
  - 1600 – 1730: Advanced Probing Interface Solutions
  - Awards for “Best Presentations” selected by committee.
- SWTest Asia EXPO 2019 with 42-key suppliers
- Technology Showcase Presentations by Platinum Sponsors
- Closing Reception in Expo Hall

Map of the Area

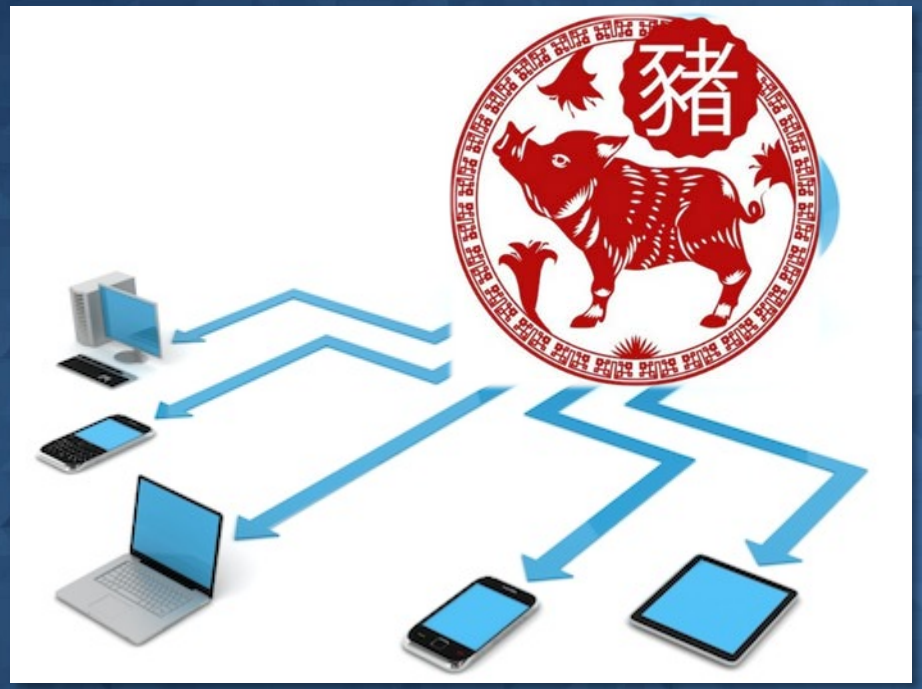


Sponsors
Tech Showcase

Technical
Program

EXPO
2019

SWTest Asia 2019 eProceedings



ePROCEEDINGS Password:

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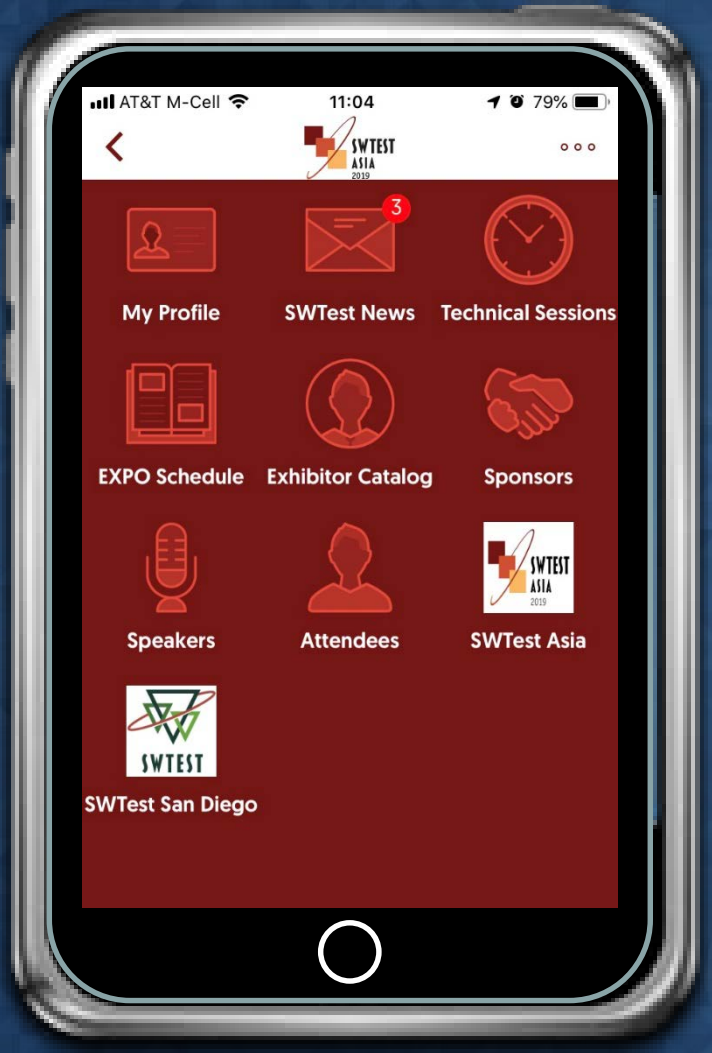
- **Conference e-Version is available for download in a password protected file.**
  - **Ballroom WiFi = SAP03**
  - **Go to … http://www.swtestasia.org … to download the daily eProceedings.**
- **Free WiFi access will be available during the entire conference to allow attendee access to the downloads.**
- **Password for the download files will be announced throughout each day and at the registration desk.**
- **Non-password locked files (including the Keynote presentations) will be made available in the SWTest Asia Archives after the conference adjourns.**

SWTest Asia App – “In the Palm of Your Hand”



- Up-to-the-minute updates in “SWTest News”
- Schedules of the “Technical Sessions”
- Meet with the “Exhibitors” and “Sponsors”
- Connect with the “Speakers”
- Attend the “Tech Showcase”
- Get oriented on the “Floorplan”
- Network with the “Attendees”
- Learn about “SWTest in San Diego”

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Platinum Sponsors

Gold Sponsors

Silver Sponsors

Friday Keynote Speaker

Wafer Test Value and Future

Masahide Ozawa

Technical Consultant

Tokyo Electron Technology Solutions - Japan

TEL™ TOKYO ELECTRON

Technical Program
SWTest Asia 2019

Friday, October 18, 2019

Hsinchu, Taiwan, October 17-18, 2019

Recognition & Awards

SWTEST ASIA
PROBE TODAY, FOR TOMORROW
2019 CONFERENCE

- **Best Overall Presentation**
- **Best Data Presentation**
- **“Most Inspirational” Presentation**

3rd Annual SWTest Asia
Coming in October, 2019
(dates will be announced soon !)

Thanks for Attending SWTest Asia !

We Hope to See you at SWTest San Diego

June 7 – 10, 2020
Rancho Bernardo Inn San Diego, California

SWTEST
PROBE TODAY, FOR TOMORROW
2020 CONFERENCE

Join us in celebrating our 30th Anniversary

30 YEAR ANNIVERSARY

Thanks for your Support !

- **Contact the SWTest Asia Team with any questions**

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“Getting ready for the next wave of growth”

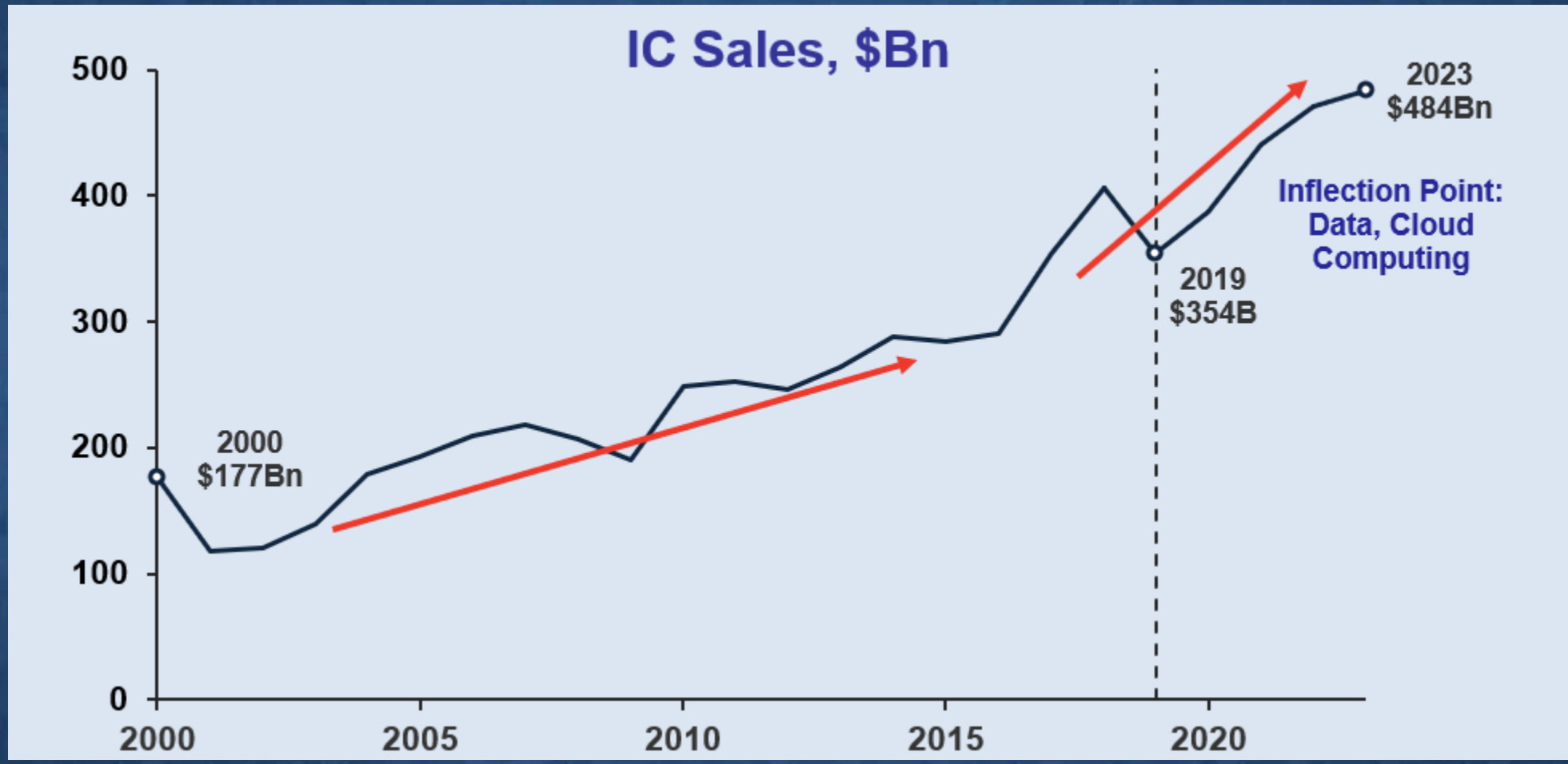
VLSIresearch

John West
VLSI Research Europe

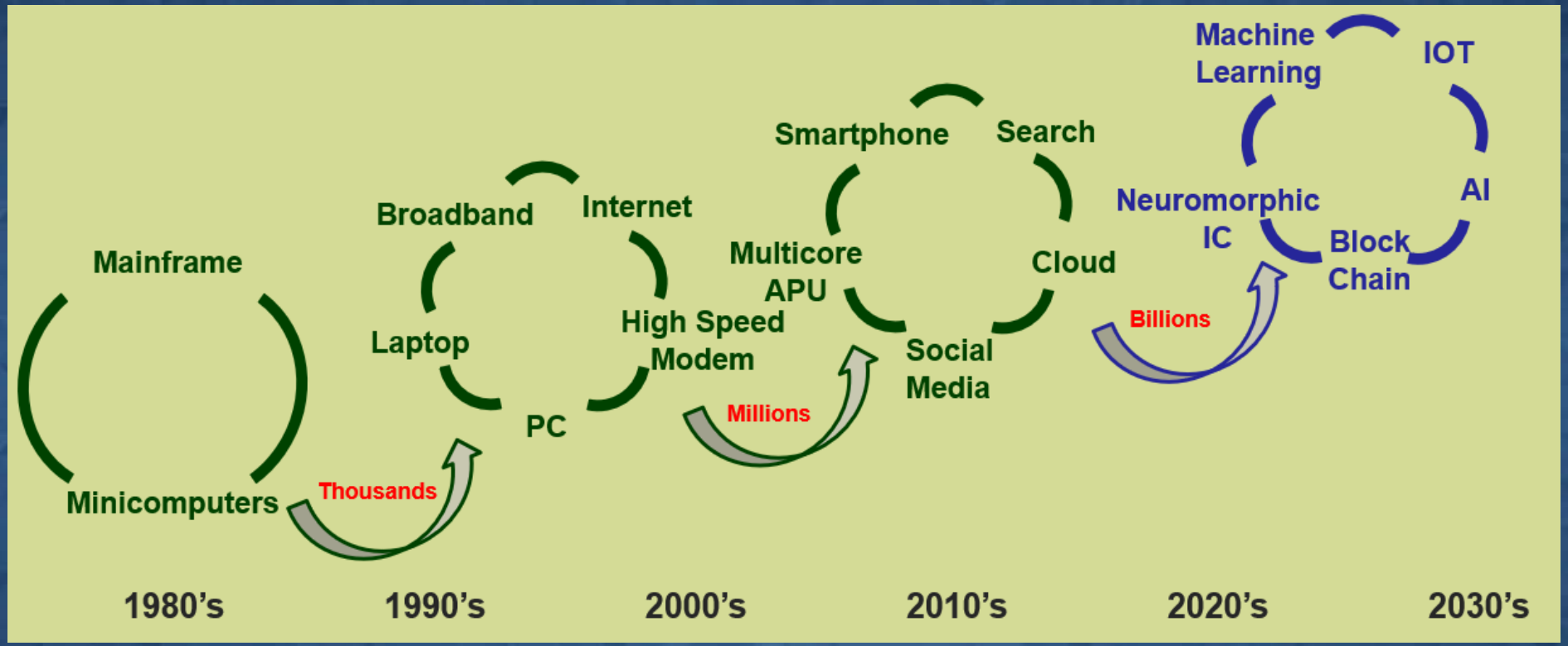
Hsinchu, Taiwan, October 17-18, 2019

The next wave of growth has already started…

Here is the data to back it up

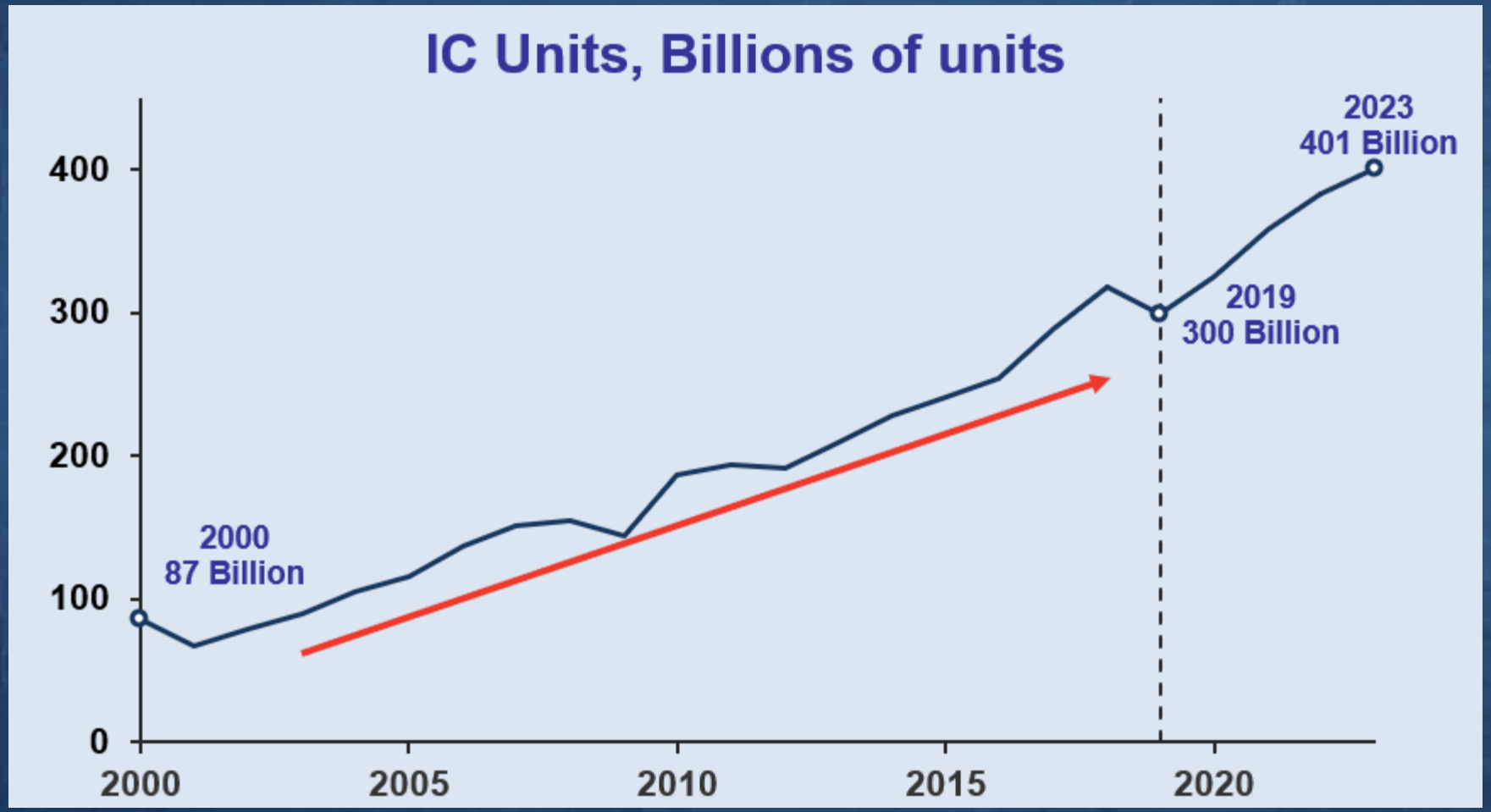


But this new wave is different to the previous three



From thousands to billions…

Units growing faster than revenues but the difference is narrowing



Average Selling Prices Trending Upwards

Are you ready?

The Main Problem for the industry

Moore's Law is slowing which means…

- 2D shrinks more difficult
- New architectures and devices required
- New materials
- Advanced packaging technology

This is driving structural change within the industry so the industry has to innovate

What this means for you…

This breaks down into three fundamental areas

Product
Capacity
Sales Strategies

Product

In the future there will be more of all probe card types, but the trend will be for…

Probe heads with more needles / higher needle density

High performance needles: higher frequencies, higher power, wider temperature ranges, durability, etc

Capacity

Are you going to run out of capacity?

Some segments are growing rapidly

Do you have the right technology roadmap?

Manufacturing technologies will change

A bit of inside information about capacity and capability

Chipmakers are concerned there is a gap emerging between what they need and what the industry can deliver

Sales Strategy:

If you don’t align your sales strategies with the changing environment, you will lose customers

Customers:

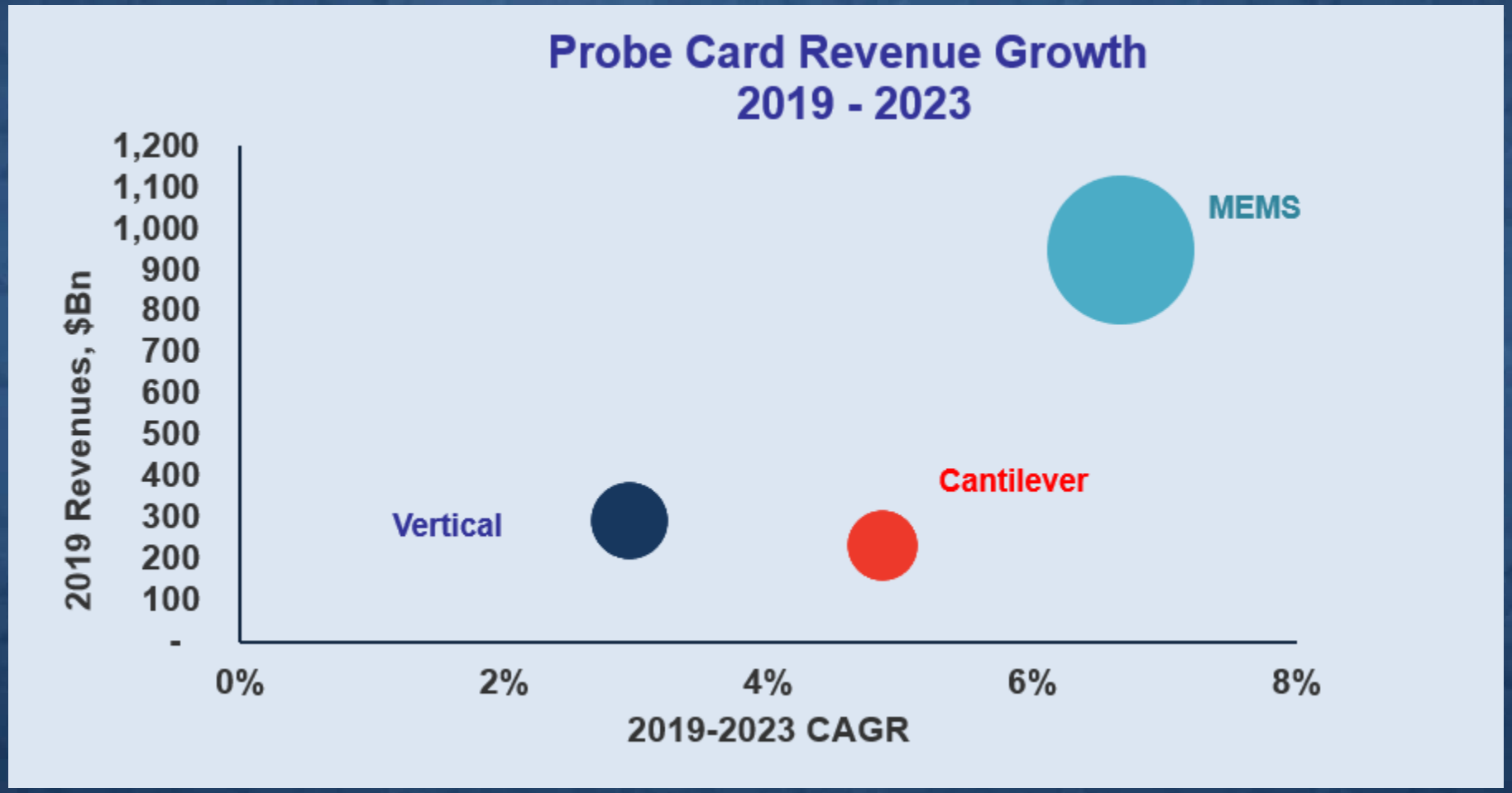
- are on the move
- priorities are changing

Competitive landscape:

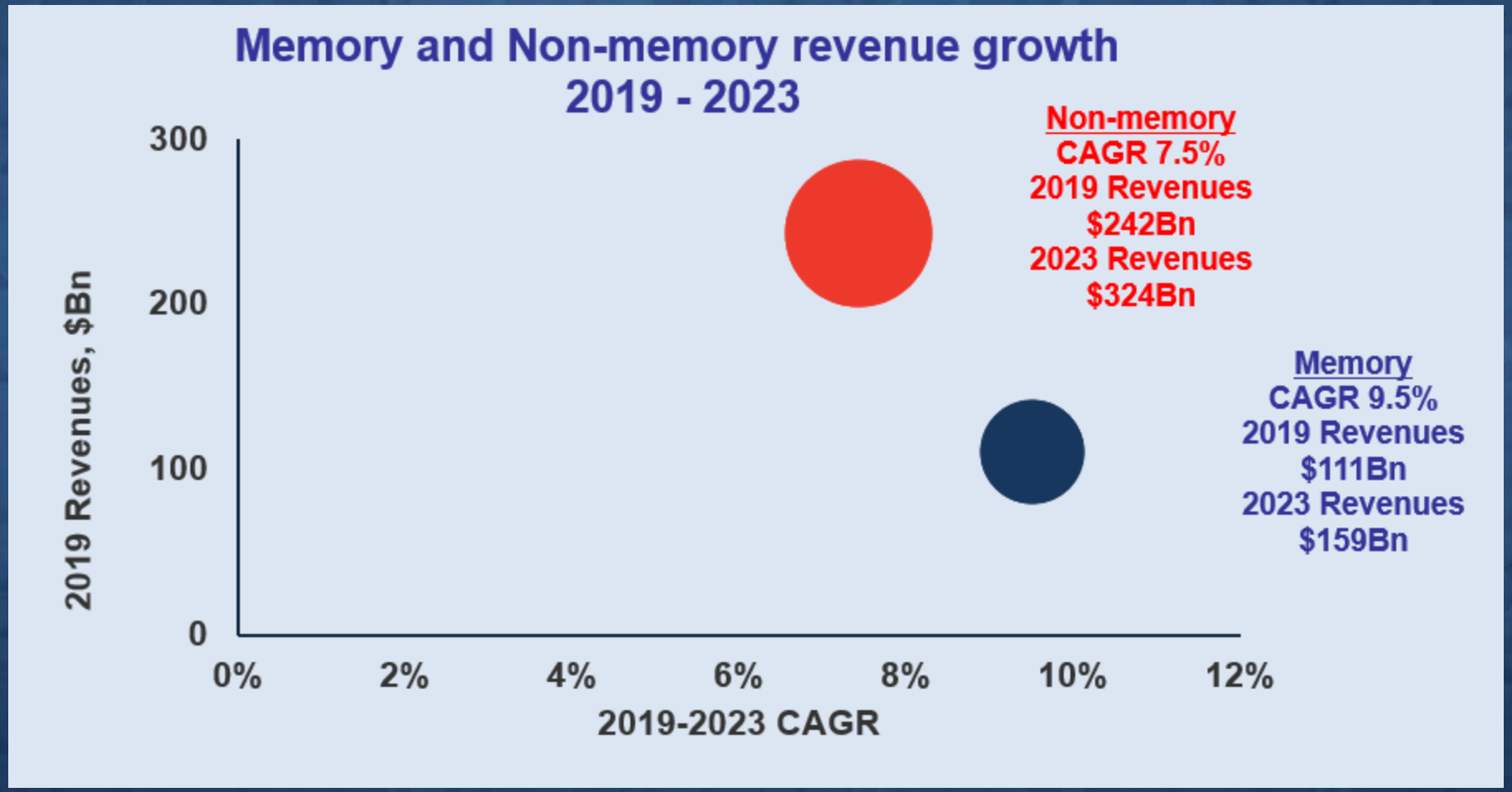
- It’s changing
- Suppliers are getting smarter

Solutions: How to use data to plan future growth

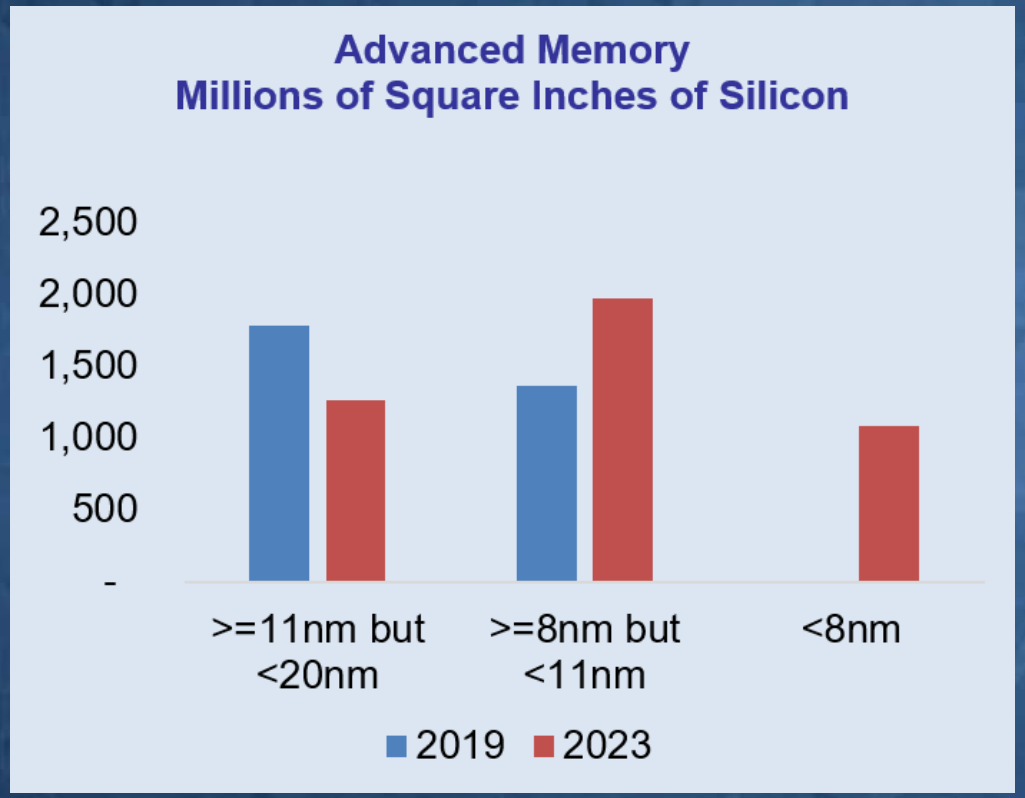
Product Solutions:
All probe card technologies growing

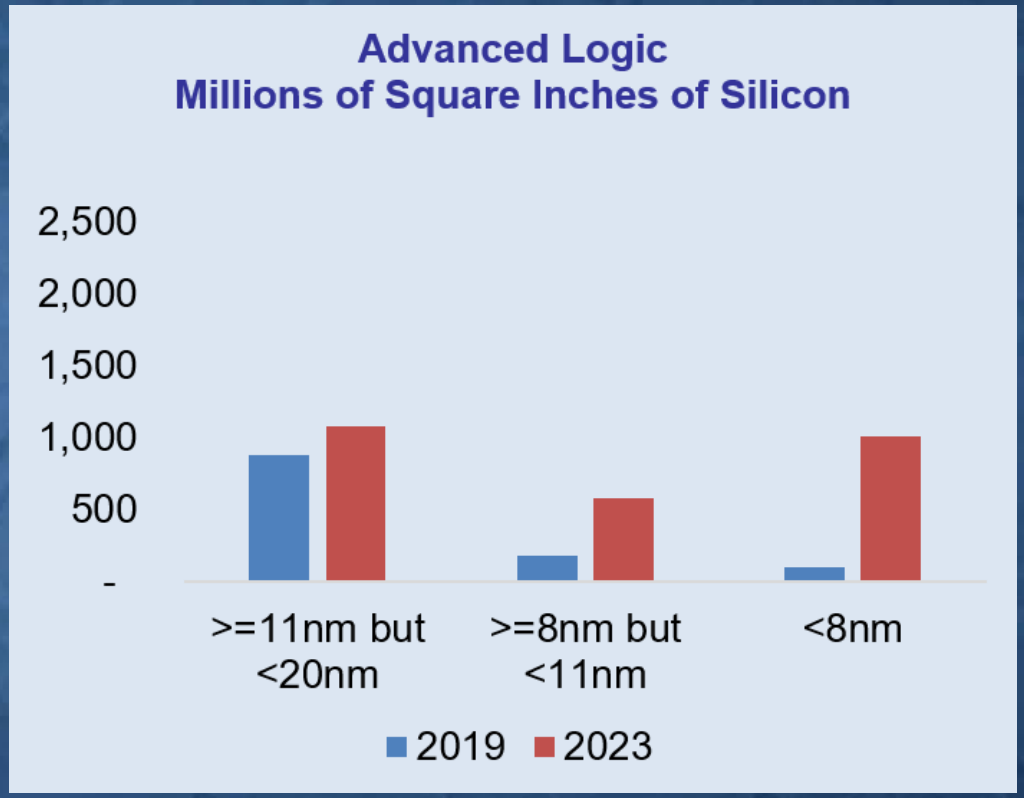


Product Solutions:
Opportunities in both memory and non-memory



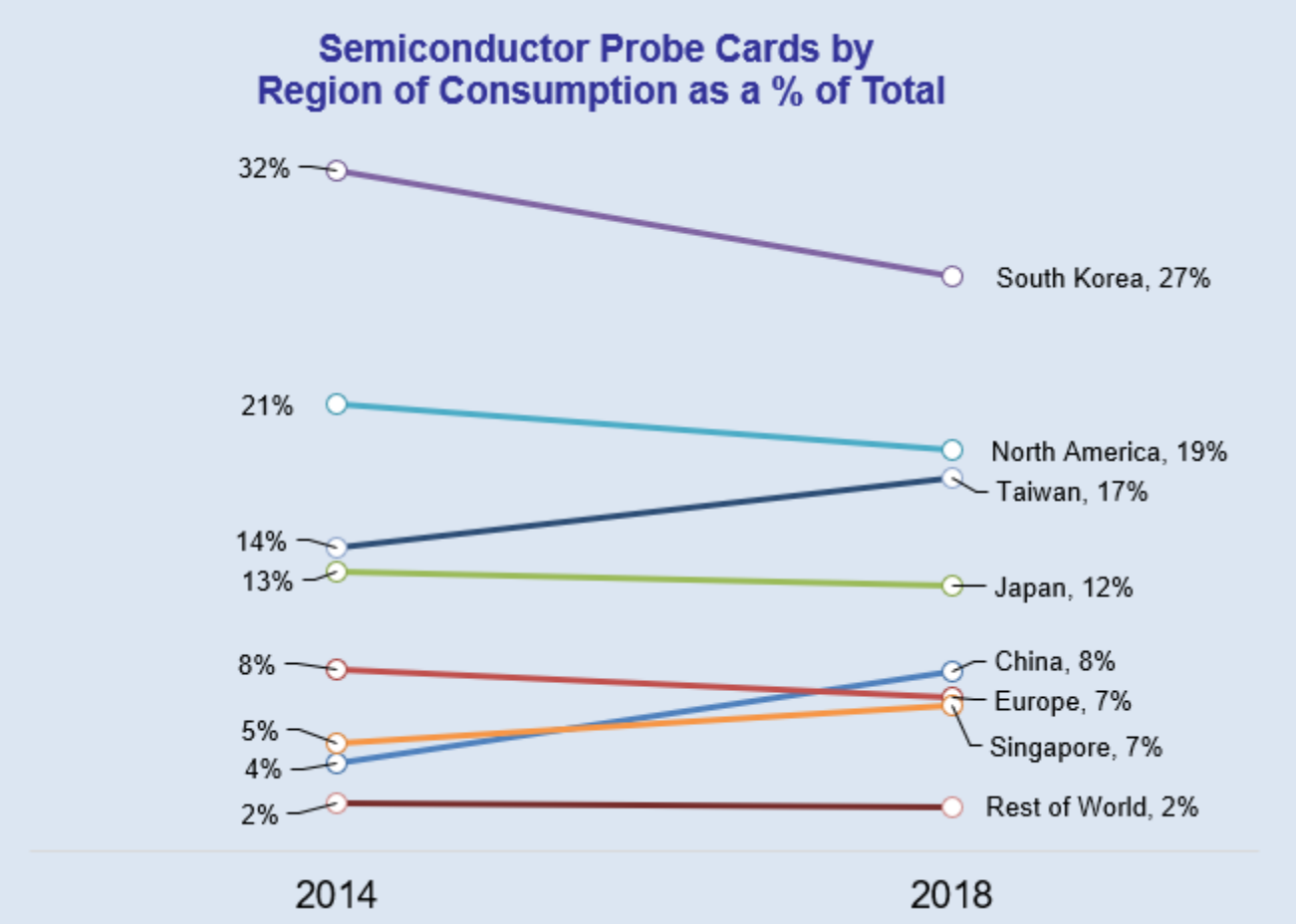
Capacity Solutions:
You need to invest now for leading edge applications



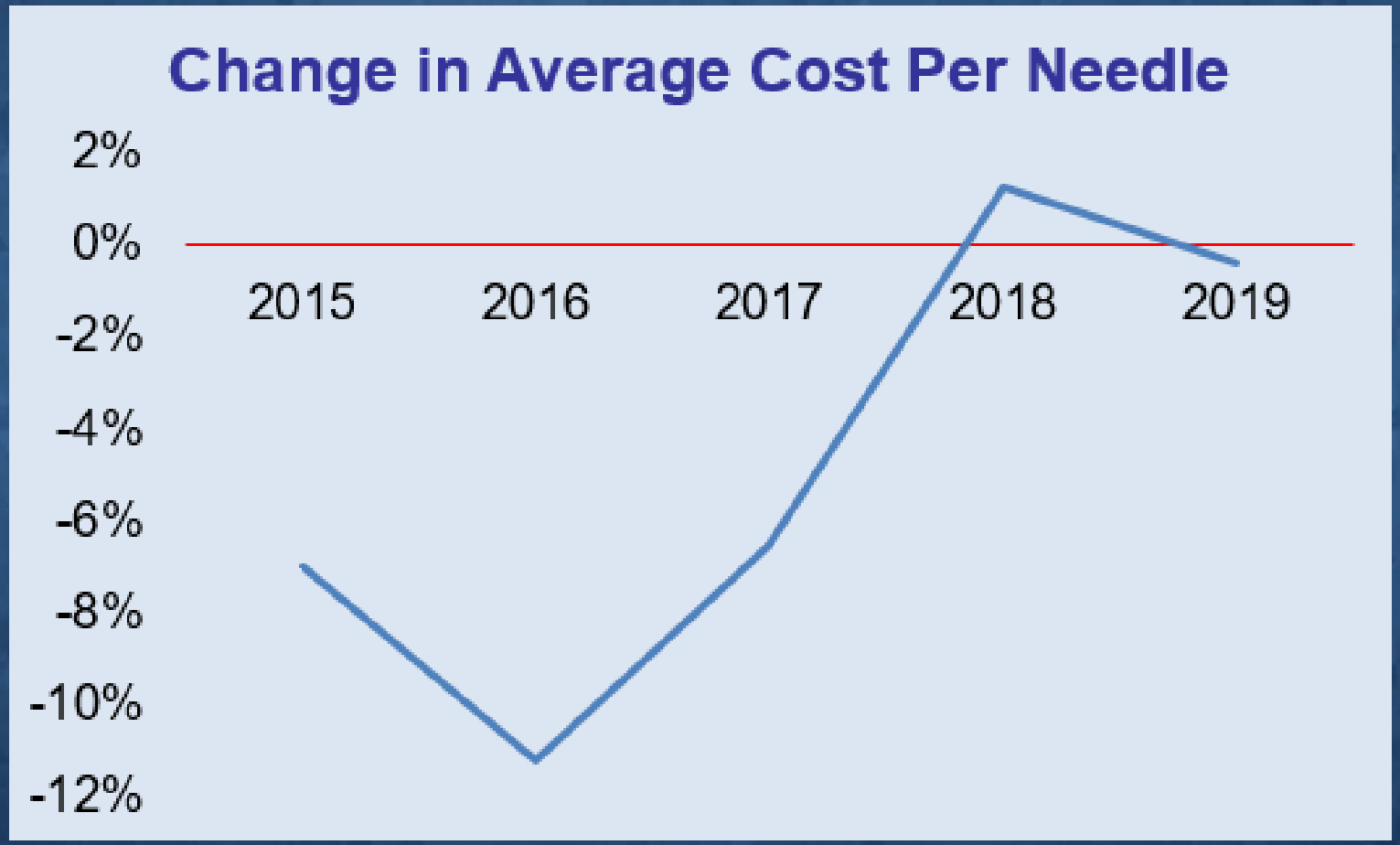


Sales Strategies Solution:

know where your customers are going to be in the future



Sales Strategies Solution: gain a deep understanding of customers' pain… it's not always the price of a probe card



So What Happens Next?

To succeed you need to understand:

- What products are required
- Which manufacturing technologies to invest in
- How your customers priorities are changing

And to do this effectively you need data and the stories behind the data so that you can be more solid in the discussions that are sure to come in this new wave of growth

SWTEST ASIA 2019

5G Enhanced Micro-Cantilever Membrane Probing Solutions

Jed Hsu
Jordan Smalls
Translarity, Inc.

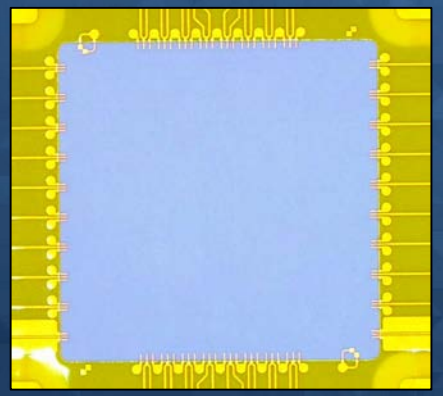
Hsinchu, Taiwan, October 17-18, 2019

Introduction

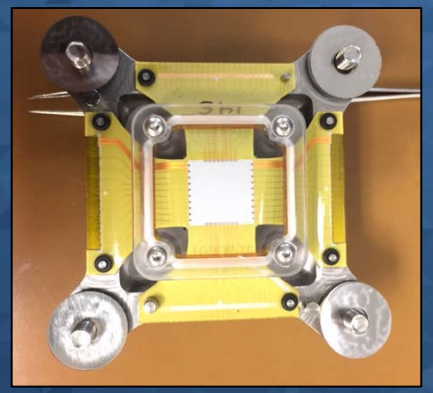
- **Market is pushing toward high frequency RF testing**
- **Translarity's solutions bring testing improvements to address:**
  - Foreign material with tall microcantilever probes
  - CRES/lateral scrub
  - Durability and lifetime
- **Objective: Create a product to test high frequency, high density devices up to 70 GHz with a focus on repeatability and durability for production stability**

Probe Card Construction

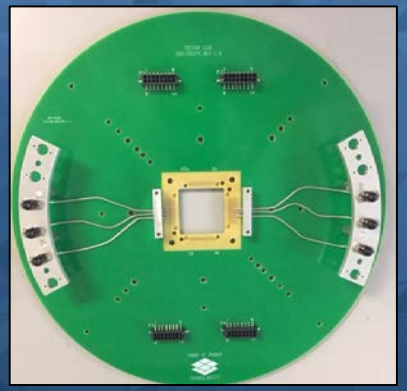
- **FPC (flexible printed circuit) design architecture**
  - Low loss materials
  - For use with microcantilever and vertical probes
- **Designed for max overtravel of 100 µm**
  - Recommended 75 µm overtravel
  - Custom design spring set for precise compliance
- **Proprietary low loss coaxial attach process**



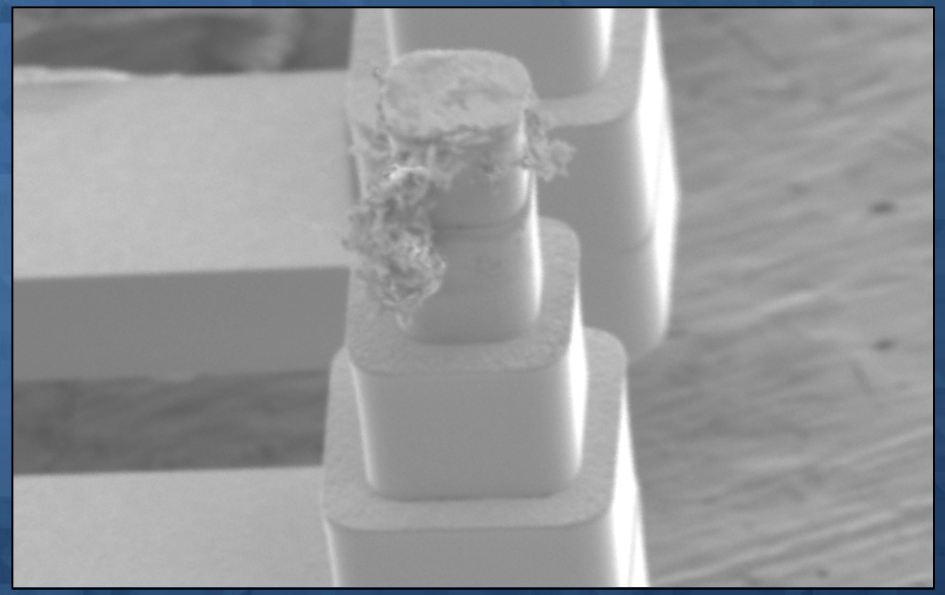
Microscope image of center design of FPC with pads



Modular Probe head



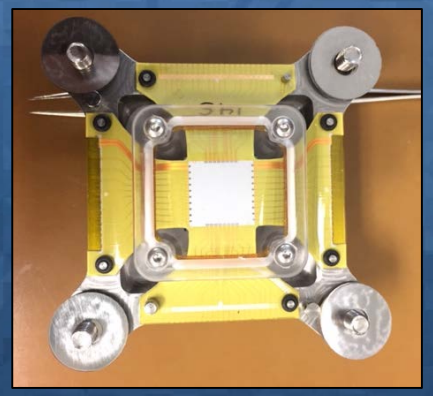
Tester side of PCB with 6 coaxial cables attached



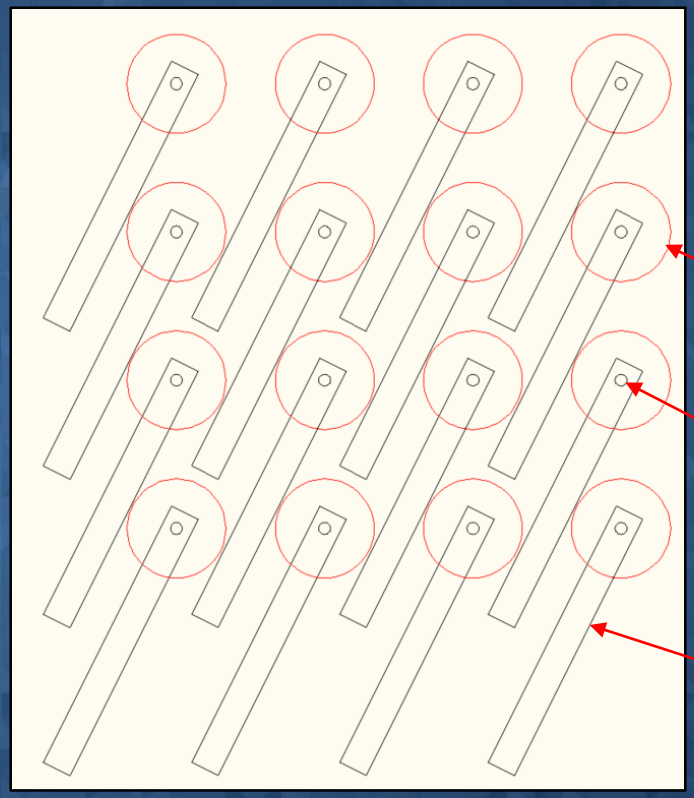
SEM image of a probe tip with foreign material.
40µm particle is not a hindrance
Probe tip is 88µm tall

Probe Card Construction

- **Probe card construction is capable for a minimum 150µm pitch array**
  - Microcantilever's tip prevents heel strike issues with tall tip design
- **Repairability**
  - Single probe repairable
  - Modular probe head enables quick probe card replacement



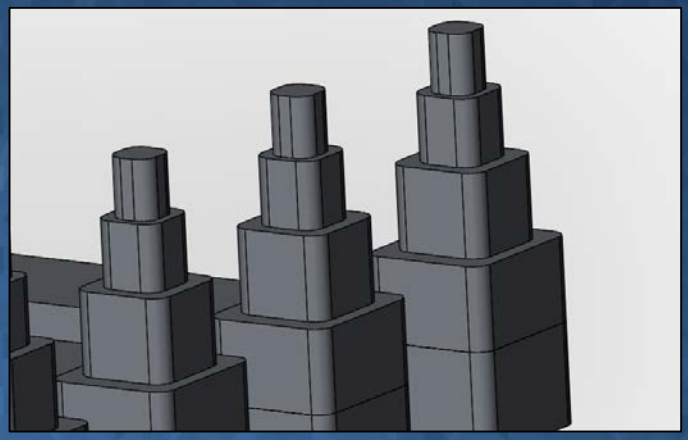
Modular Probe head



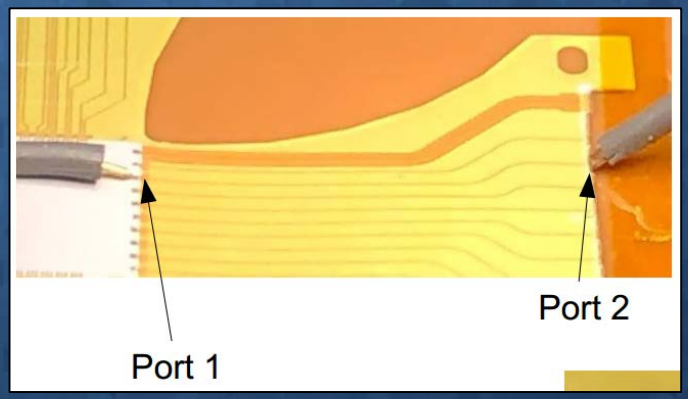
Microcantilever probe design for contacting 150µm pitch array

Simulation & Testing Data Summary

- **RF simulations**
  - Cantilever probes
  - Cantilever probes + FPC
- **RF measurements of complete assembly**
- **Cantilever probe characterization**
  - Force
  - CCC
  - Durability



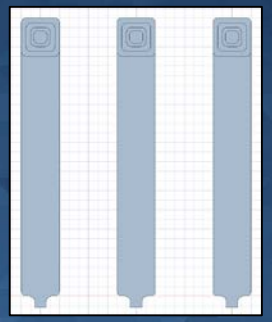
Microcantilever model



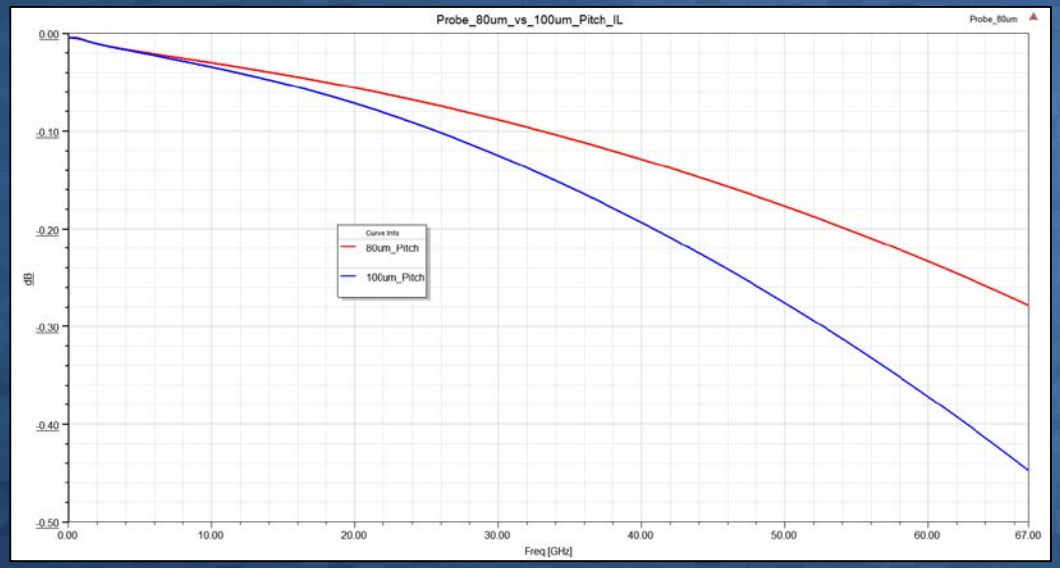
Test Setup

HFSS Simulation Results: Cantilever Probes

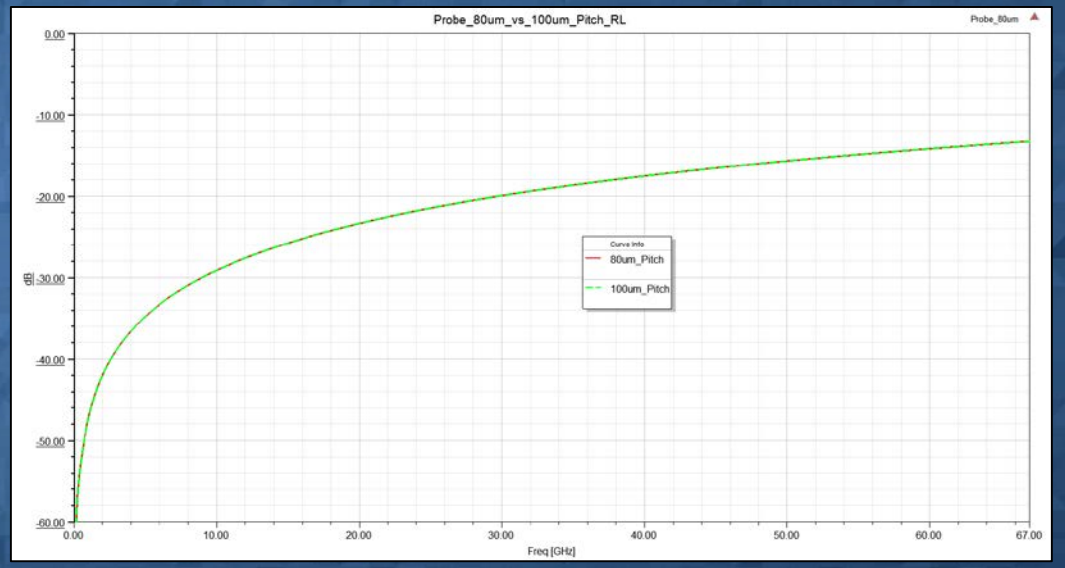
- **Microcantilever designs simulated in isolation, suspended in air**
- **Frequency range: DC to 67 GHz.**
- **Simulated with microcantilever at 80µm and 100µm pitch**



Microcantilever probes, top view



S21, insertion loss

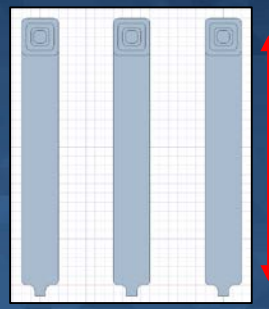


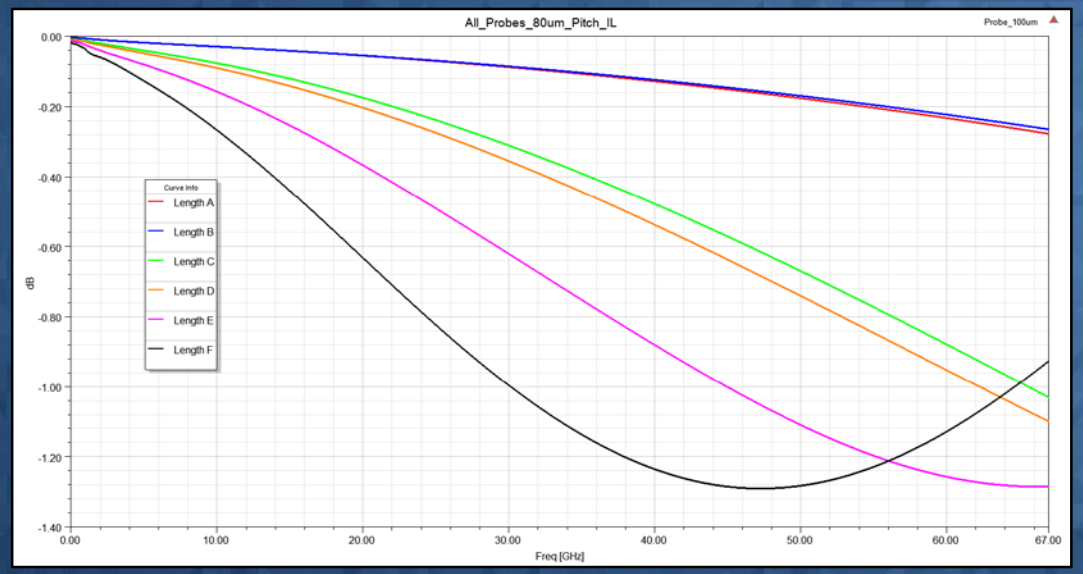
S11, return loss

Probe design has very low signal loss

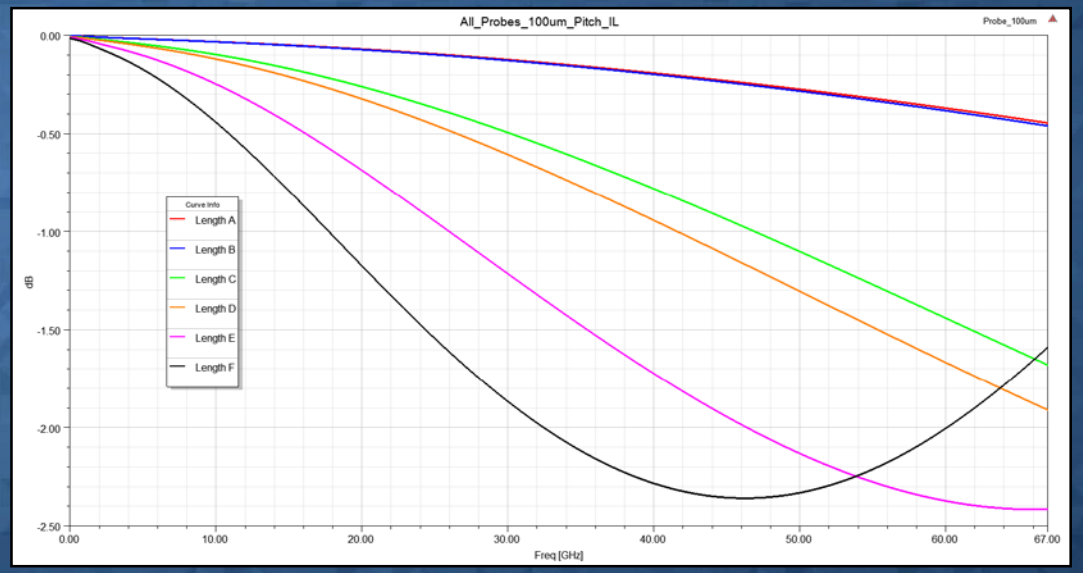
HFSS Simulation Results: Cantilever Probes

- **Microcantilever designs with various cantilever lengths simulated at 80µm and 100µm pitch for insertion loss**





S21, Insertion Loss at 80µm pitch

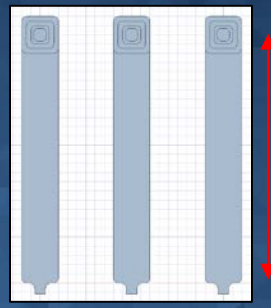


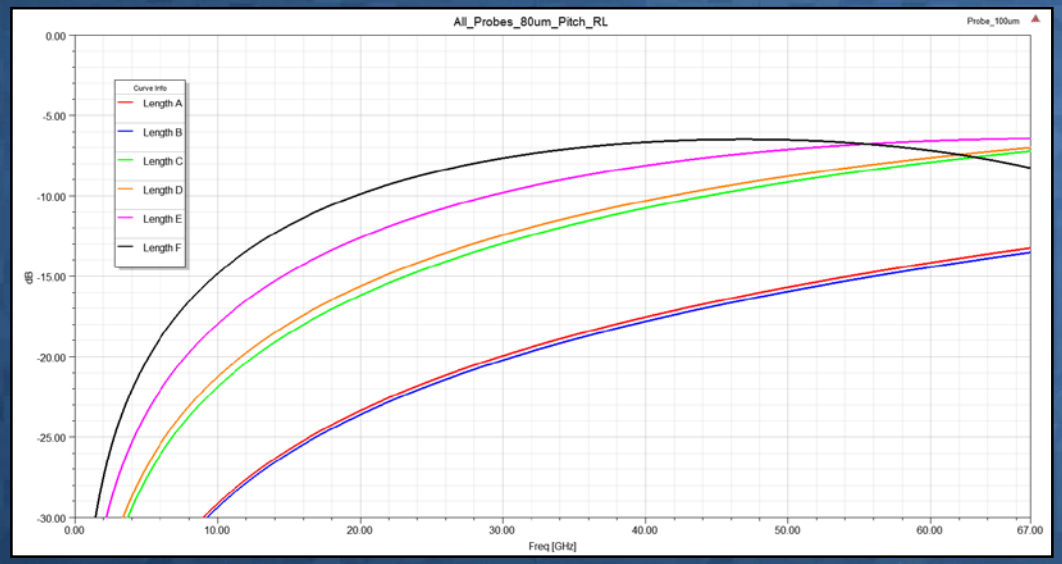
S21, Insertion Loss at 100µm pitch

Probe design can support various cantilever lengths and pitches

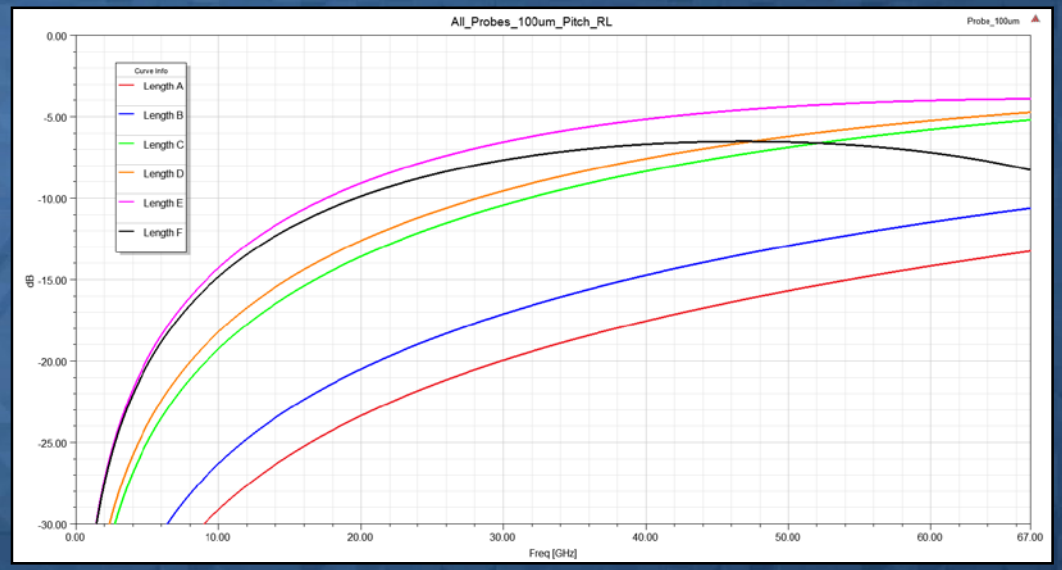
HFSS Simulation Results: Cantilever Probes

- **Microcantilever designs with various cantilever lengths simulated at 80µm and 100µm pitch for return loss**





Return Loss at 80µm pitch

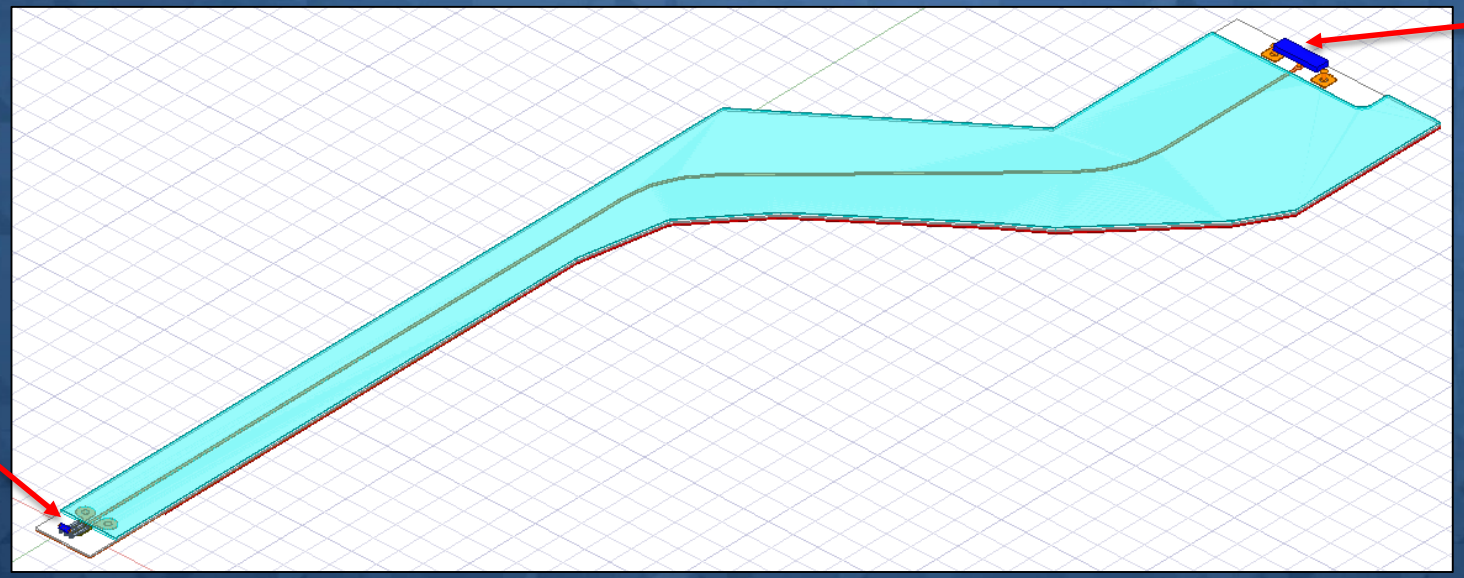


Return Loss at 100µm pitch

Probe design can support various cantilever lengths and pitches

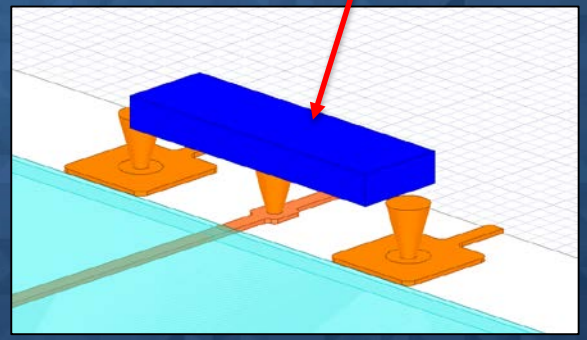
Simulation Model: Probes and FPC

- **Simulation model in GSG configuration**
  - Includes microcantilever probes and FPC
  - Simulated microstrip transmission line



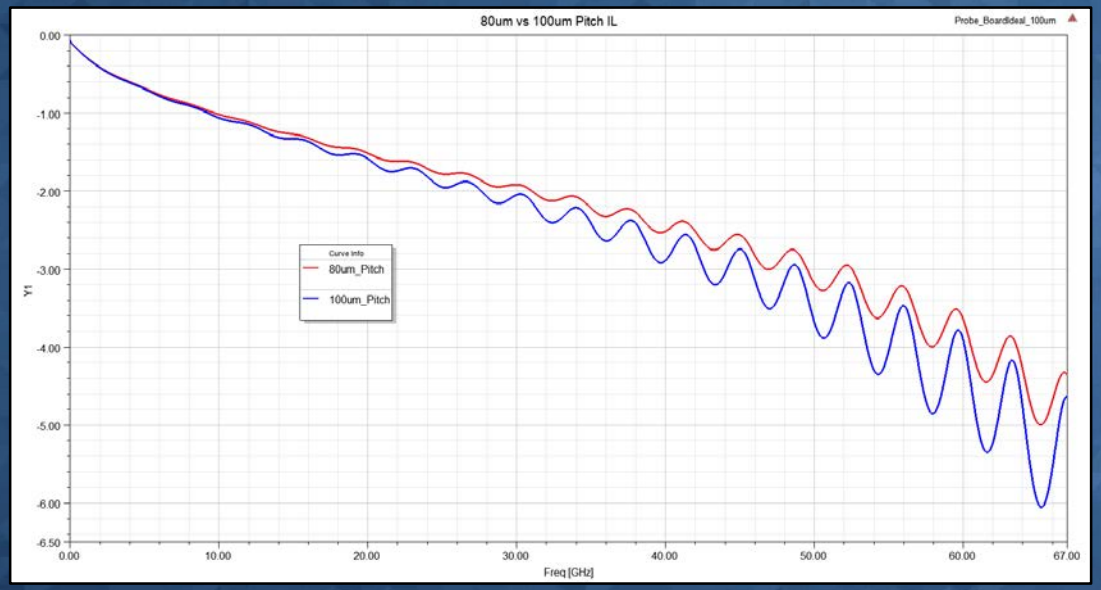
Simulation microstrip

GSG Tester
Probe, Port 1

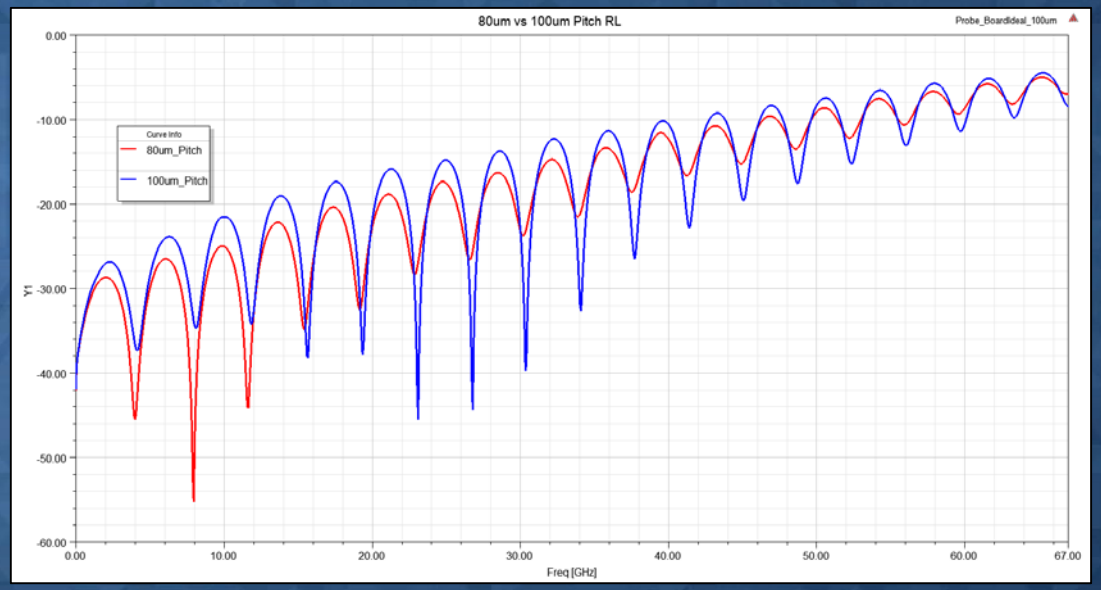


Simulation Results: Probes + FPC

- Simulation results for probes and FPC
- Target insertion loss < 5dB, return loss > 10dB



S21, Insertion Loss

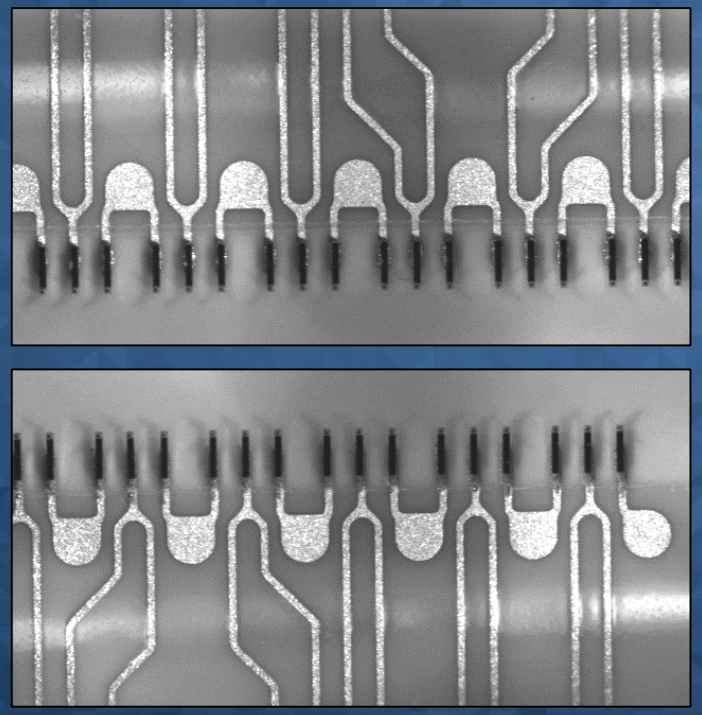


S11, Return Loss

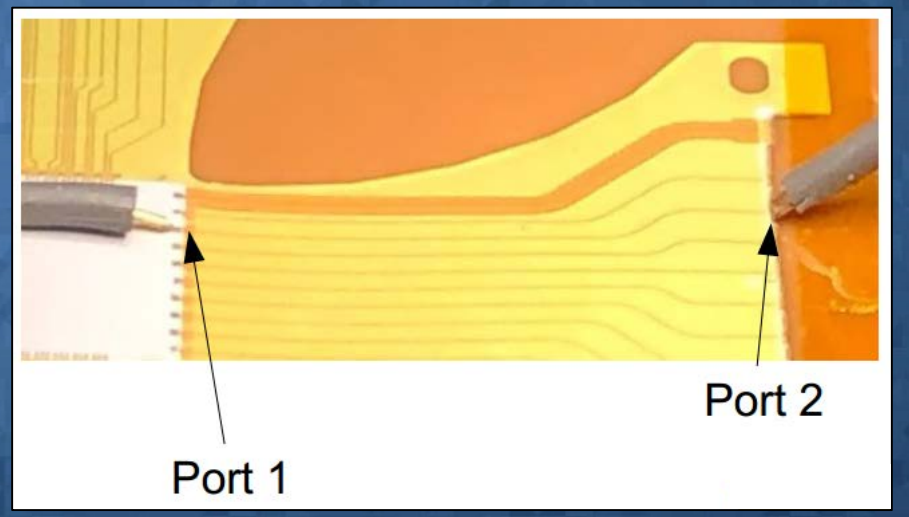
Probes + FPC perform well to about 40GHz

Measurement Results

- **Completed probe head assembly tested by outside independent lab**
- **First prototype demonstrated to >20 GHz**



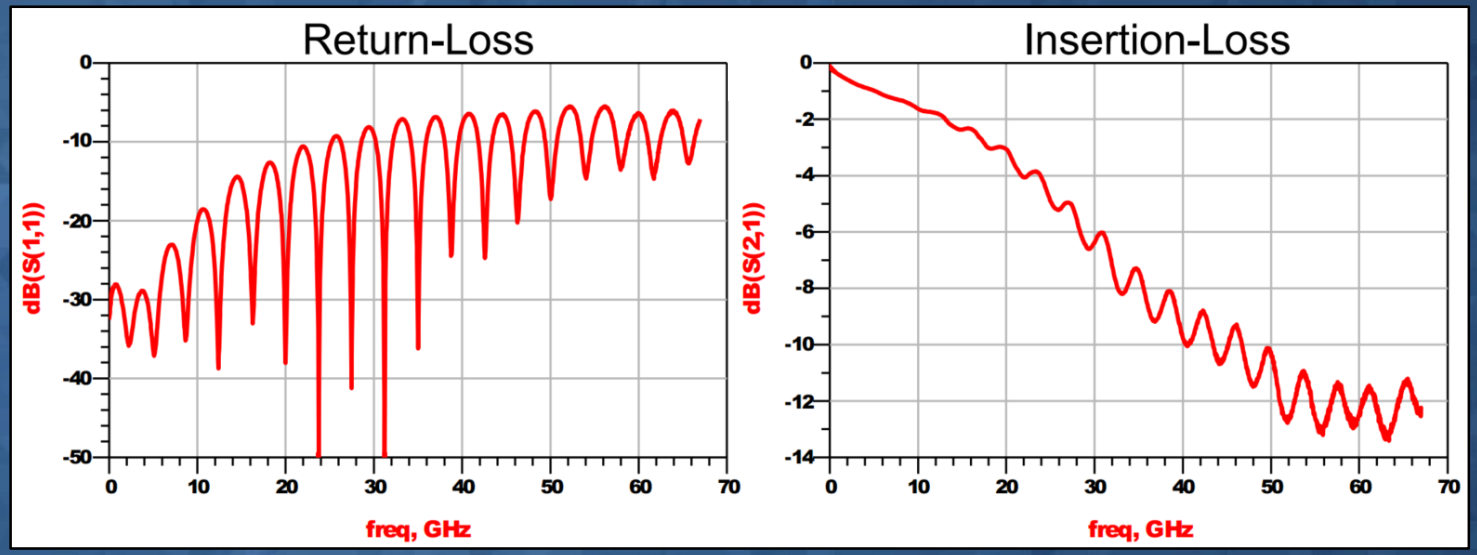
Microscope images of cantilever probes



Test Setup

Probe + FPC Measurements, Rev 1 Build

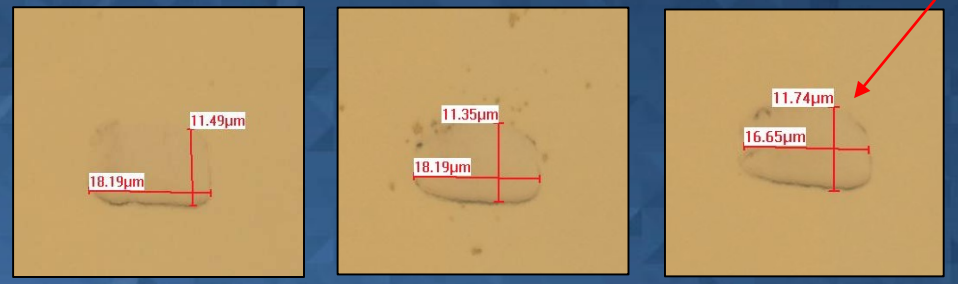
- **Industry:**
  - 5 dB @ 20 GHz insertion loss
  - 10 dB @ 20 GHz return loss
- **Measurements:**
  - 3 dB @ 20 GHz insertion loss
  - 12 dB @ 20 GHz return loss



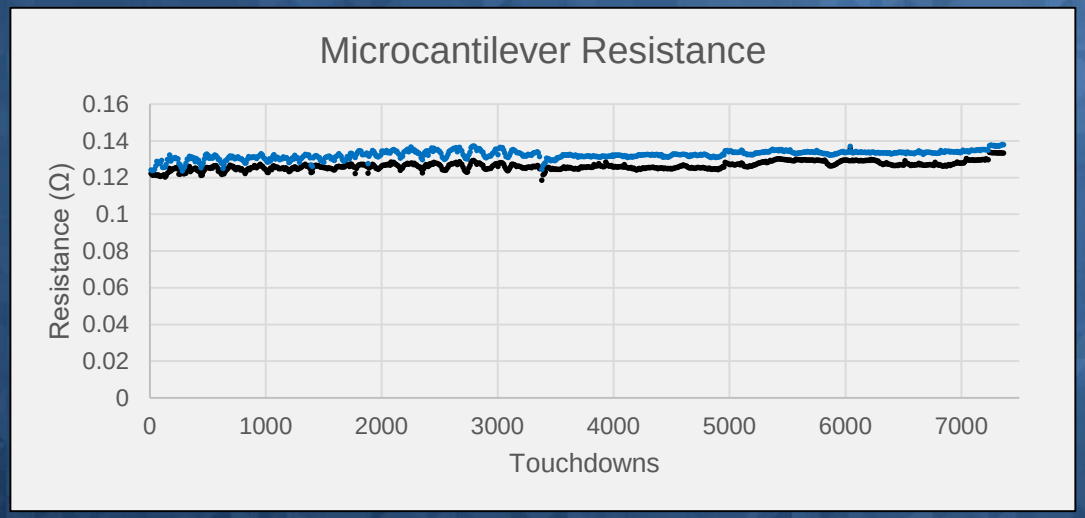
Graphs above show as measured data

Mechanical Data: Scrub marks

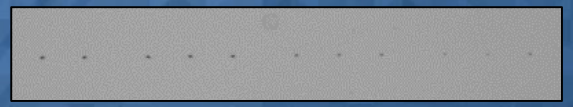
- **Microcantilever probes' mechanical design allows for 2-4 µm of lateral scrub**
- **Allows probes to self-wipe during testing and keep resistance low**



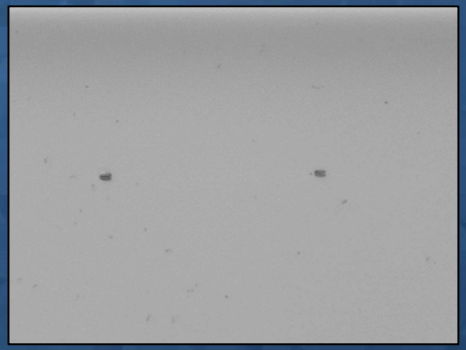
Sample measurements of scrub marks



Resistance includes microcantilever probe and flex microstrip



Low magnification image of scrub marks on Accretech tester on a blank Al/Cu wafer

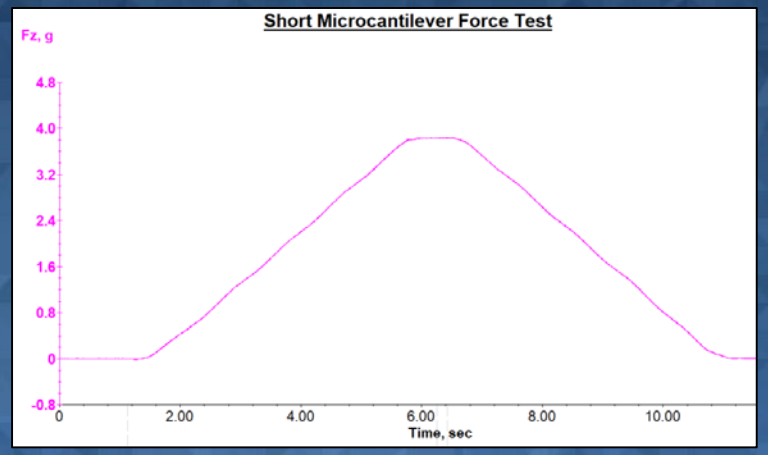


High magnification image

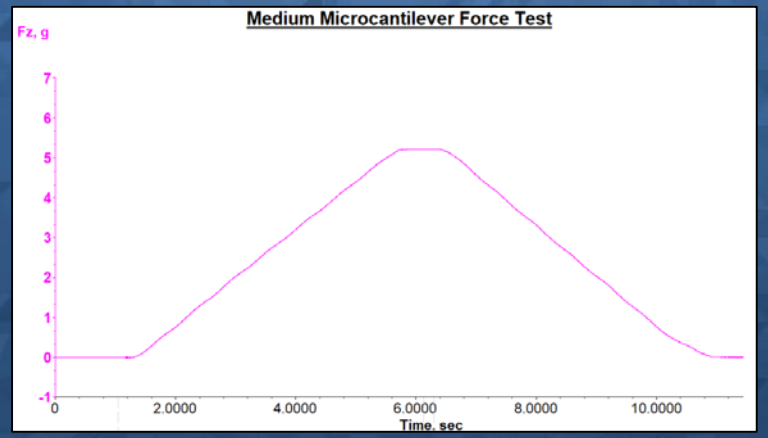
Lateral scrub ensures good electrical contact

Force and CCC

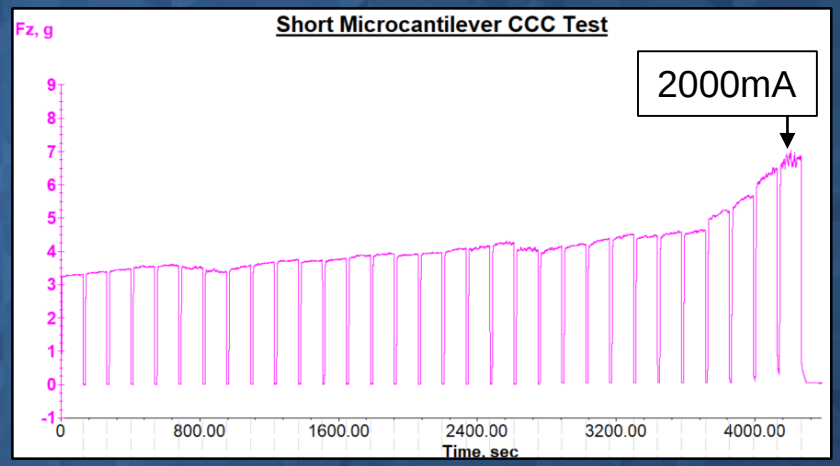
- **Force can be adjusted based on application**
  - 4g and 5g probe data shown
- **CCC**
  - Microcantilever probe tested from 300mA to 2000mA and did not show failure
  - Current on time = 2 min
  - Current off time = 10 s



Example data for short microcantilever force, 3.8g



Example data for medium microcantilever force, 5.2g

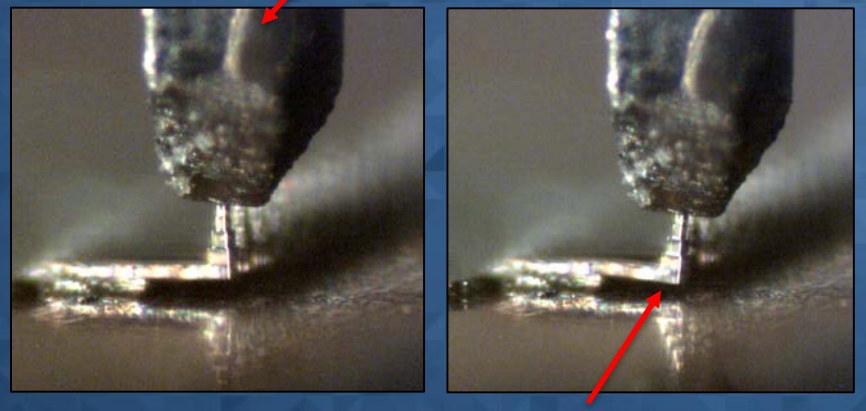


CCC Test showed no cantilever failure up to 2000mA

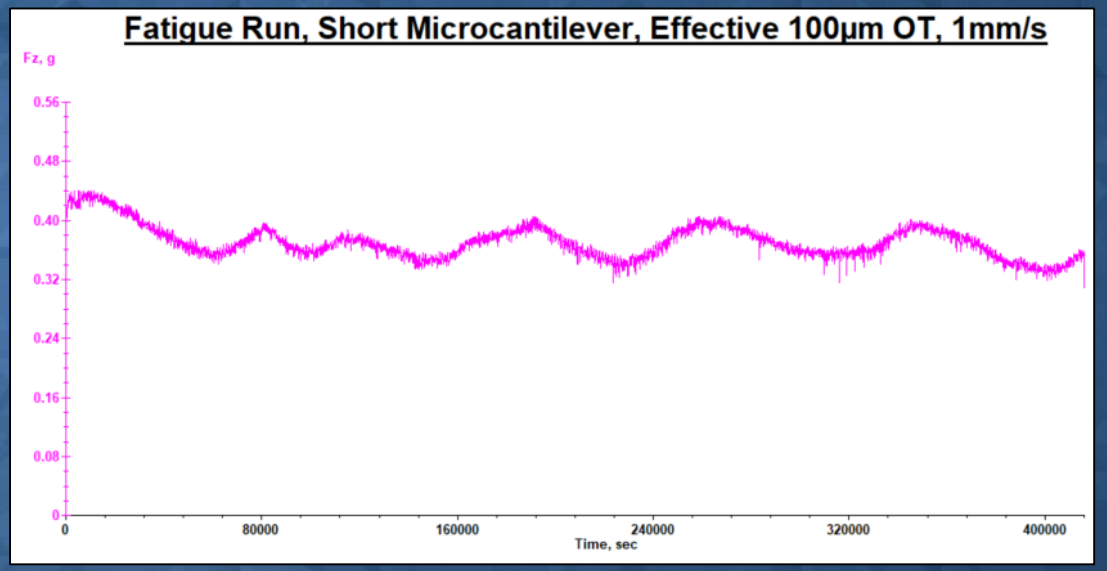
Fatigue Run

- **Microcantilever probes tested on Bruker tribometer**
  - Cantilever probe survived over 5.8 million cycles at an effective 100µm OT
  - No failure at end of test

Tribometer probe



Microcantilever probe under compression



Fatigue run graph shows force over time at 14 cycles/second

Probes are extremely durable and reliable

Conclusion & Next Steps

- **Novel concepts in ultra high frequency, high reliability RF testing**
  - Resistant against foreign material with tall microcantilever probes
  - Good CRES with 2-4 µm lateral scrub
  - Durability of 5.8 million cycles
- **Continuous improvements to higher frequencies and lower pitch**
- **Repairability**
  - Due to the durability of the probes, repair should be very infrequent
  - Modular construction allows quick customer replaceable, inexpensive flex coupon
- **Seeking customers for beta site engagements**

How to successfully embrace the era of 5G mmWave test

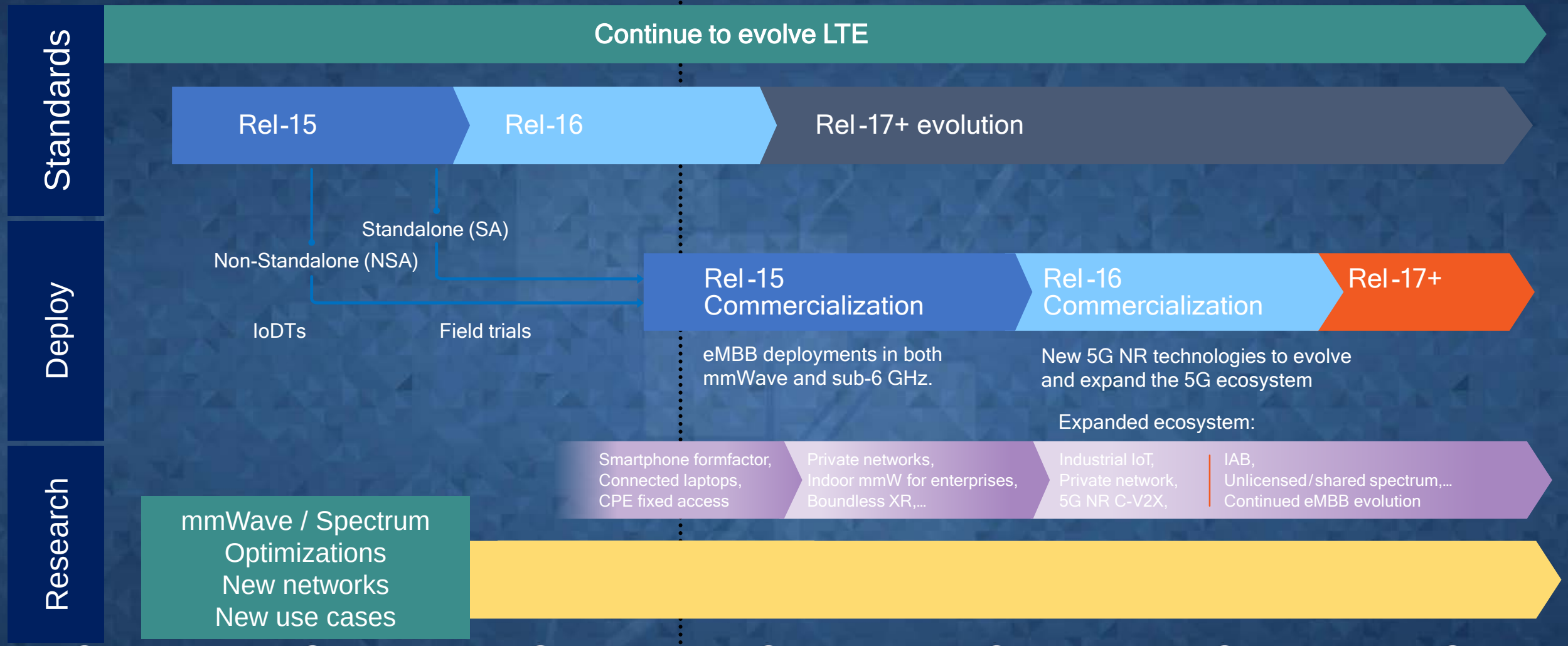
John Su
Technical Marketing Engineer

Hsinchu, Taiwan, October 17-18, 2019

Overview

- How is 5G progress status and why mmWave?
- Conquer mmWave Test Challenge
- Methodology of mmWave Test for Wafer Conductive, OTA validation & Production
- Summary / Conclusion
- Follow-On Work

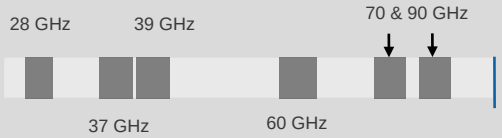
3GPP 5G Timeline



Author

Key Test Challenges for mmWave 5G

Multi-Standard / Multi-Band Coverage



Ultra-wide Bandwidths

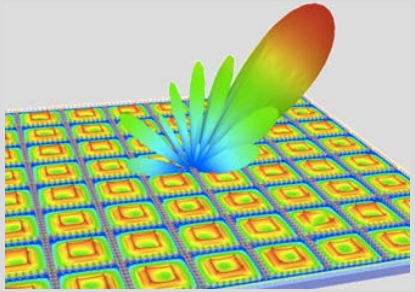
4G: 200 MHz

4.5 G: 640 MHz

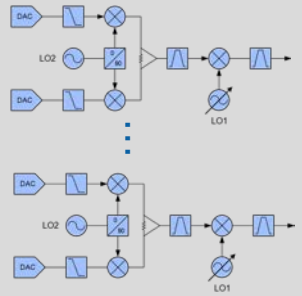
5G: 800 MHz (Phase 1)

5G: 2 GHz (Phase 2)

Antenna Arrays and Beamforming Validation

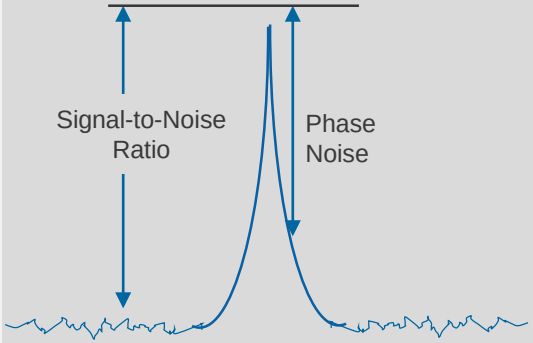


Channel Scaling for MIMO / CA

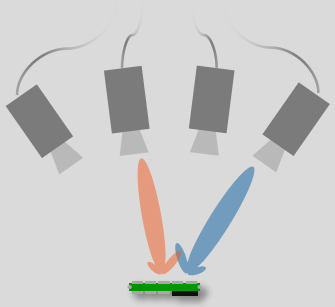


2 – 128 MIMO channels

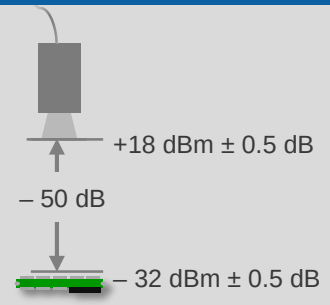
Managing Noise in High Loss Operation



OTA Performance



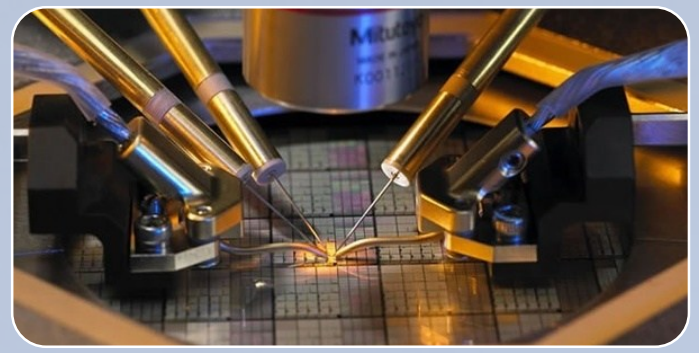
Calibrated Air Interfaces and Chambers



Near field / Far Field

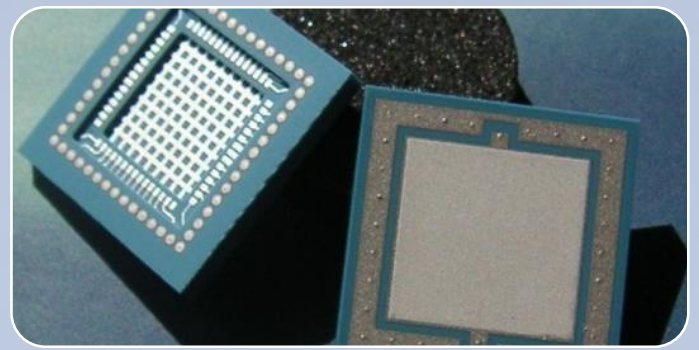
Total Cost of Test

5G mmWave Test Needs



Si Wafer Level

- Known good die
- Primarily conducted test for now
- OTA is not necessary unless for antenna on die



AiP Level

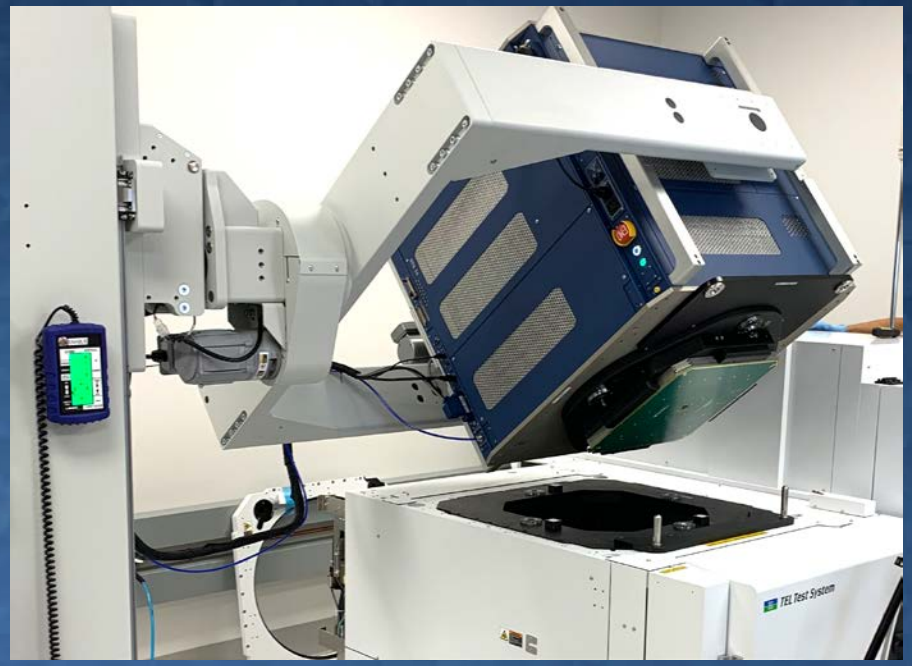
- Uniform radiated RF performance on all elements
- No conducted test exists
- OTA is a must

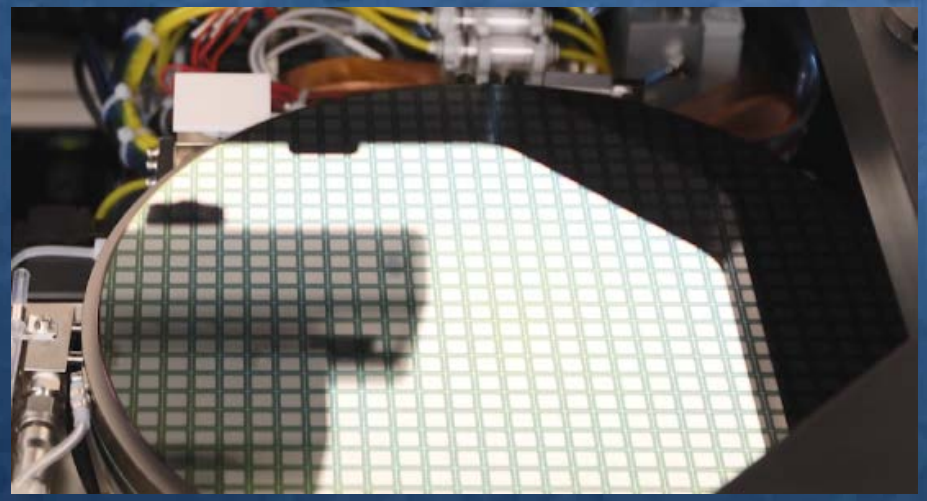
RRH Level

- Well calibrated RF performance & synchronization
- No beam spec tested in production
- OTA test to reduce in-field replacements cost

Wafer Level Test

- Wafer Level mmWave Test is not new, typically do measurement before for Harmonic test
- Due to mmWave IC architecture revolution, DUT type not only traditional RF FEM; cover from RF Transceiver, Beamformer, Up/ Down Converter, integrated FEM, Phase Array Antenna……
- Beamformer & Phase Array Antenna make mmWave channel requirement significantly increase





Typical Test Item

RX
- Adjustable Gain
- Gain Ripple
- Phase Shifter
- OIP3
- ISOLATION
- NF
- EVM
- ACPR

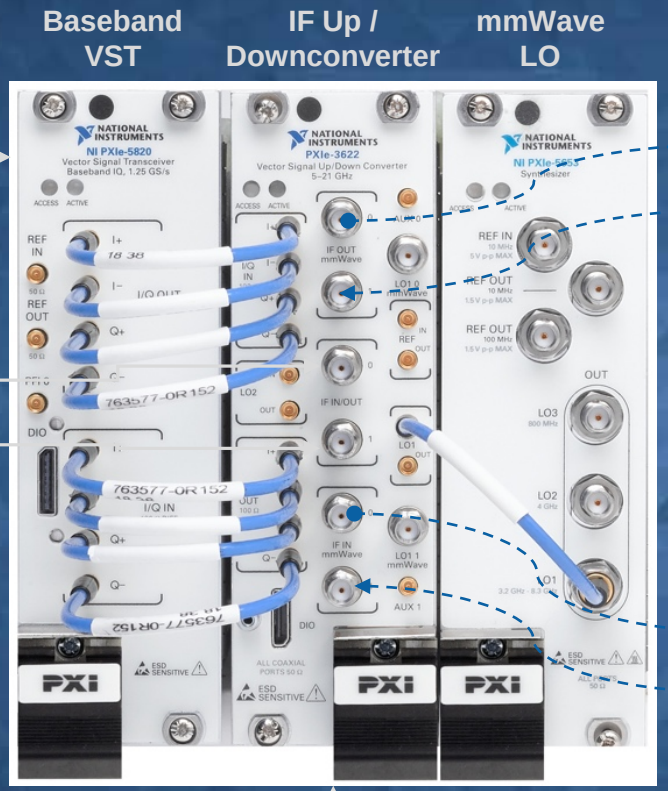
TX
- Adjustable Gain
- Gain Ripple
- Phase Shifter
- OP1dB
- OIP3
- AMPM
- PAE
- ISOLATION
- NF
- EVM
- ACPR

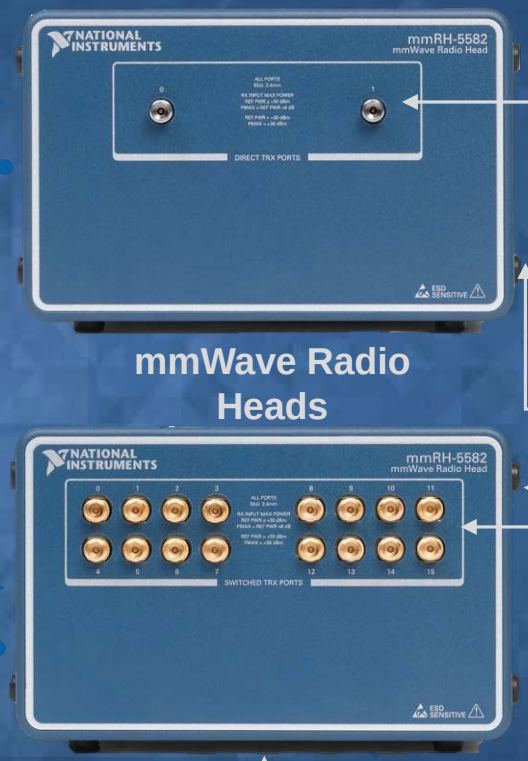
Flexible Configuration for mmWave IC Test

1 GHz BW Baseband
Modular for upgradeability

2x IF Test Ports
Bi-directional, 5 – 21 GHz
Test V & H Polarities

High IF Up/Downconverter
Future proof for bands expansion
5G mmWave IF and 7 GHz WLAN





mmWave Radio Heads

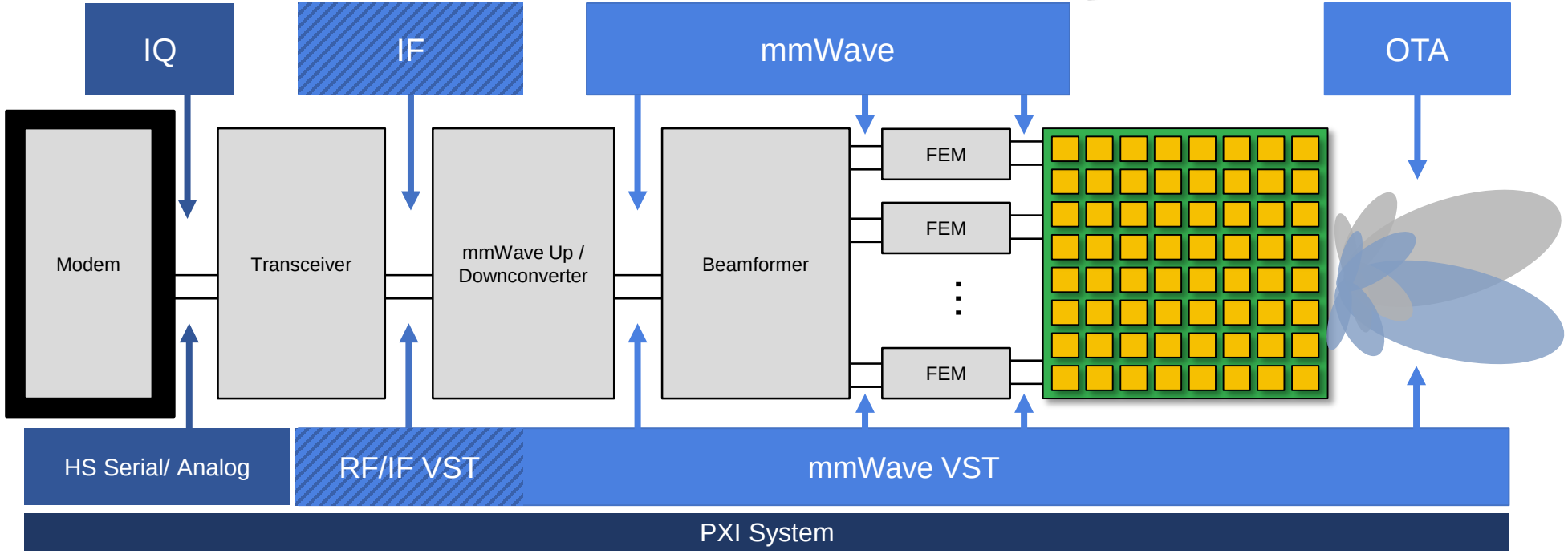
***Direct* TRX Ports**
Higher power delivery
V & H polarity connections

Multiple Port Configurations
Optimized mapping to *array* of DUT architectures

Integrated solid-state switching
Removes connectivity and calibration burden for multi-port

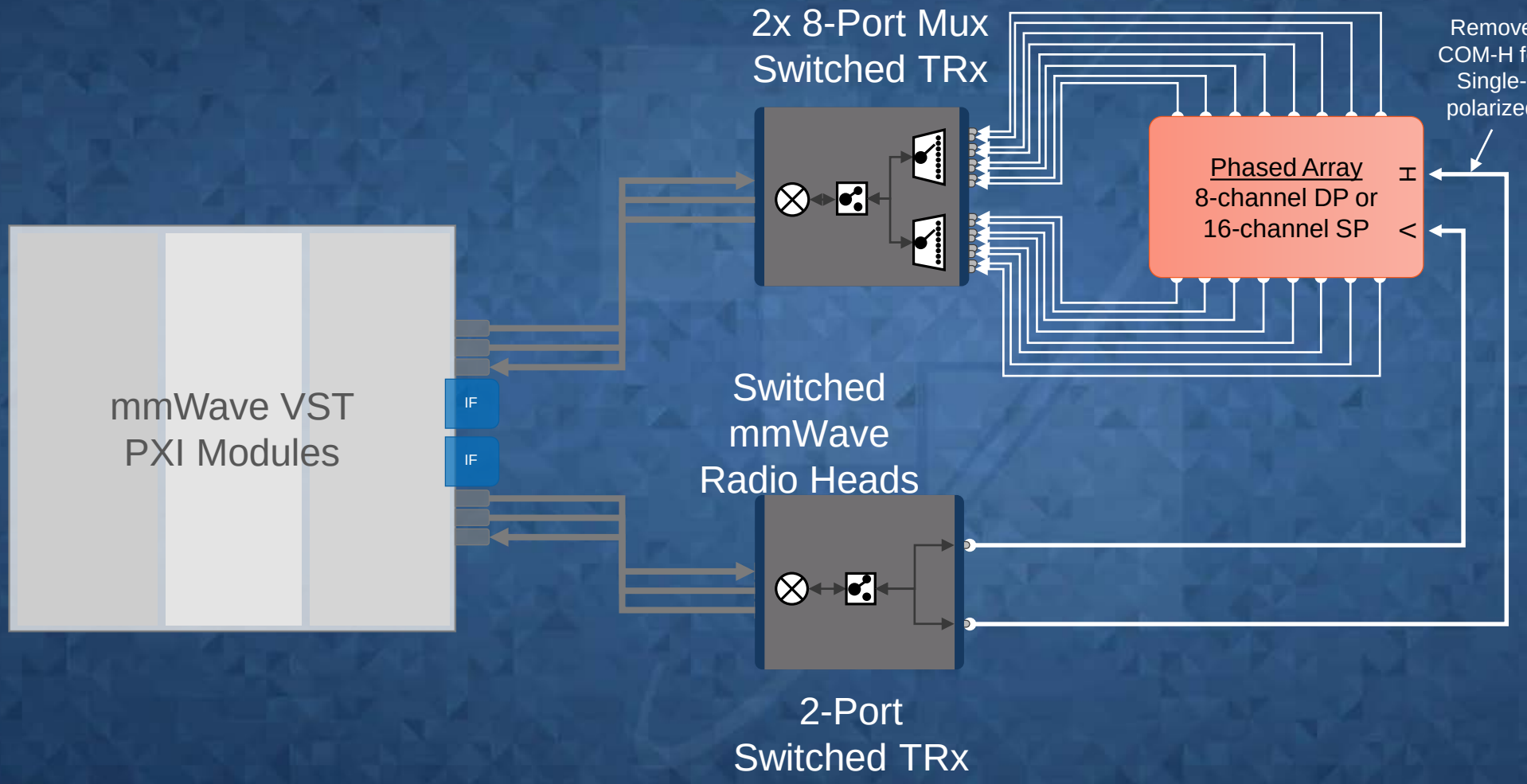
Remote mmWave Conversion
Flexible placement
Scalability for future bands

One Solution to Test the Complete Signal Chain



Example Test Configuration:

Up to 8-ch – Dual Polarized or 16-ch Single Polarized RF-RF Phased Array



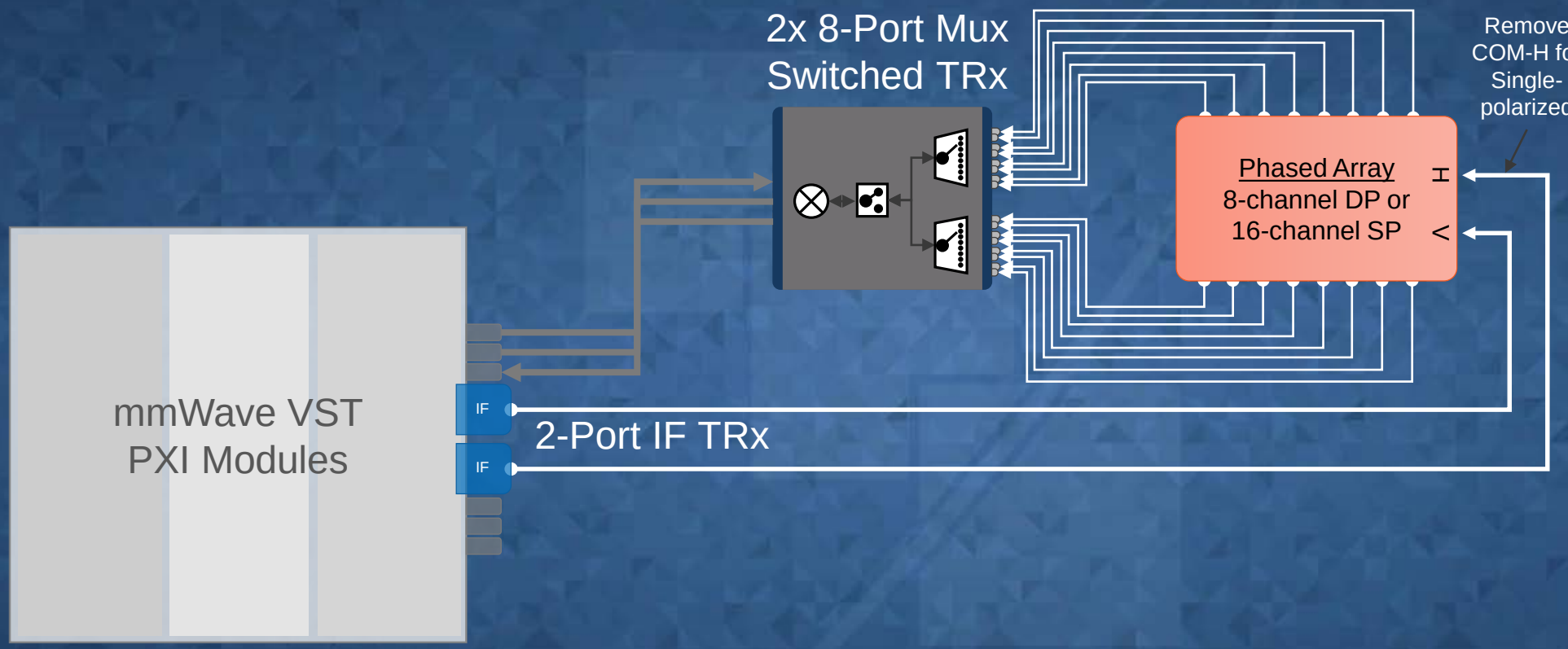
Typical Tests

- Gain vs. state
- Phase vs. state
- Ch-Ch phase
- Compression (PxdB)
- O/IIP3
- Modulation Accuracy
  - EVM
  - Impairments
  - Flatness
- ACLR
- SEM
- Noise Figure
- Crosstalk
- Return Loss
- Efficiency

NI RFmx

Example Test Configuration:

Up to 8-ch – Dual Polarized or 16-ch Single Polarized IF-RF Phased Array



Typical Tests

- Gain vs. state
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- Modulation Accuracy
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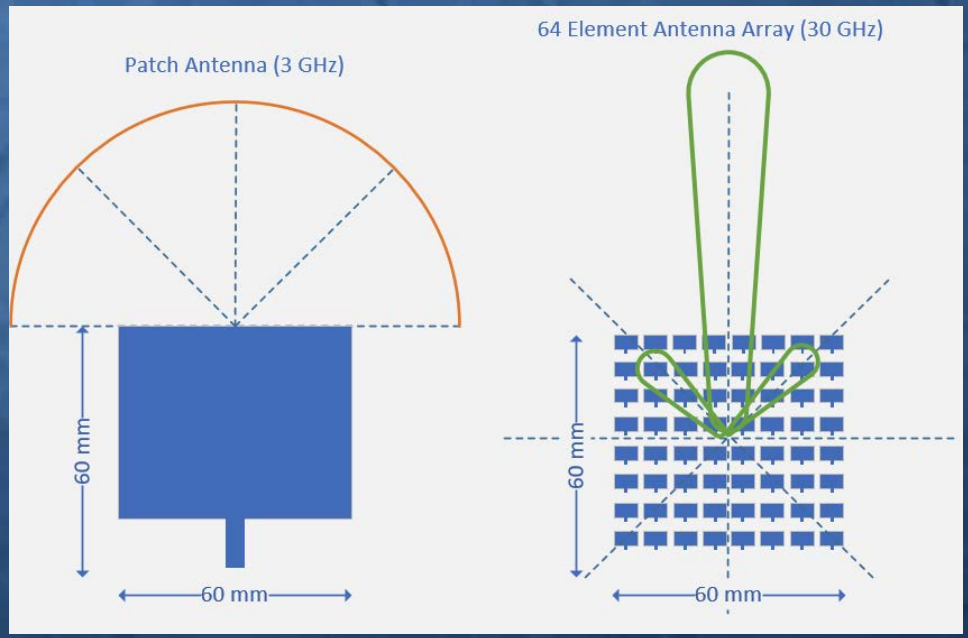
  - Impairments
  - Flatness
- ACLR
- SEM
- Noise Figure
- Crosstalk
- Return Loss
- Efficiency

NI RFmx

OTA: Beamforming to Overcome High Path Loss (**dB**)

	850MHz	28GHz	38GHz
10m	51.03	81.38	84.04
500m	85.01	115.36	118.02
1km	91.03	121.38	124.04

~30dB
1000x



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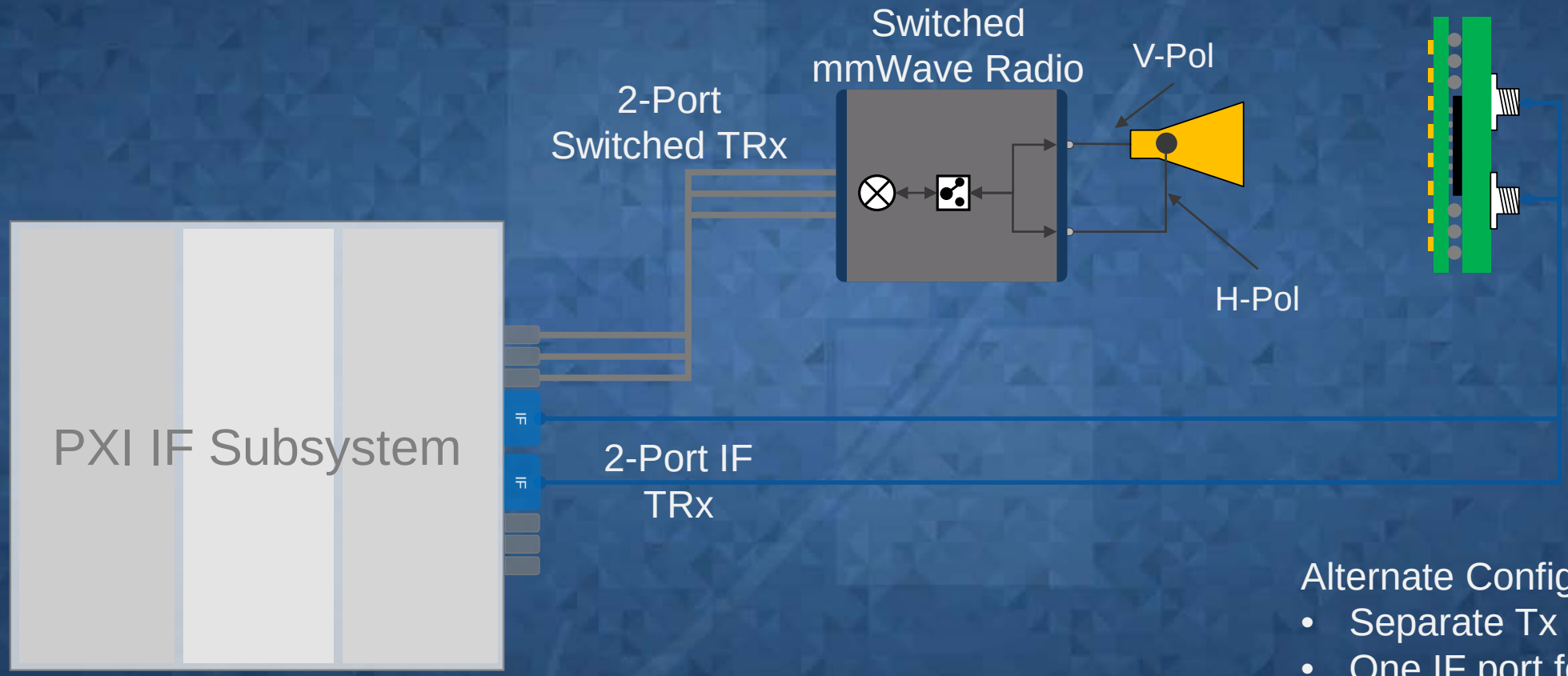
Up to 8-ch – Dual Polarized or 16-ch Single Polarized IF-RF Phased Array

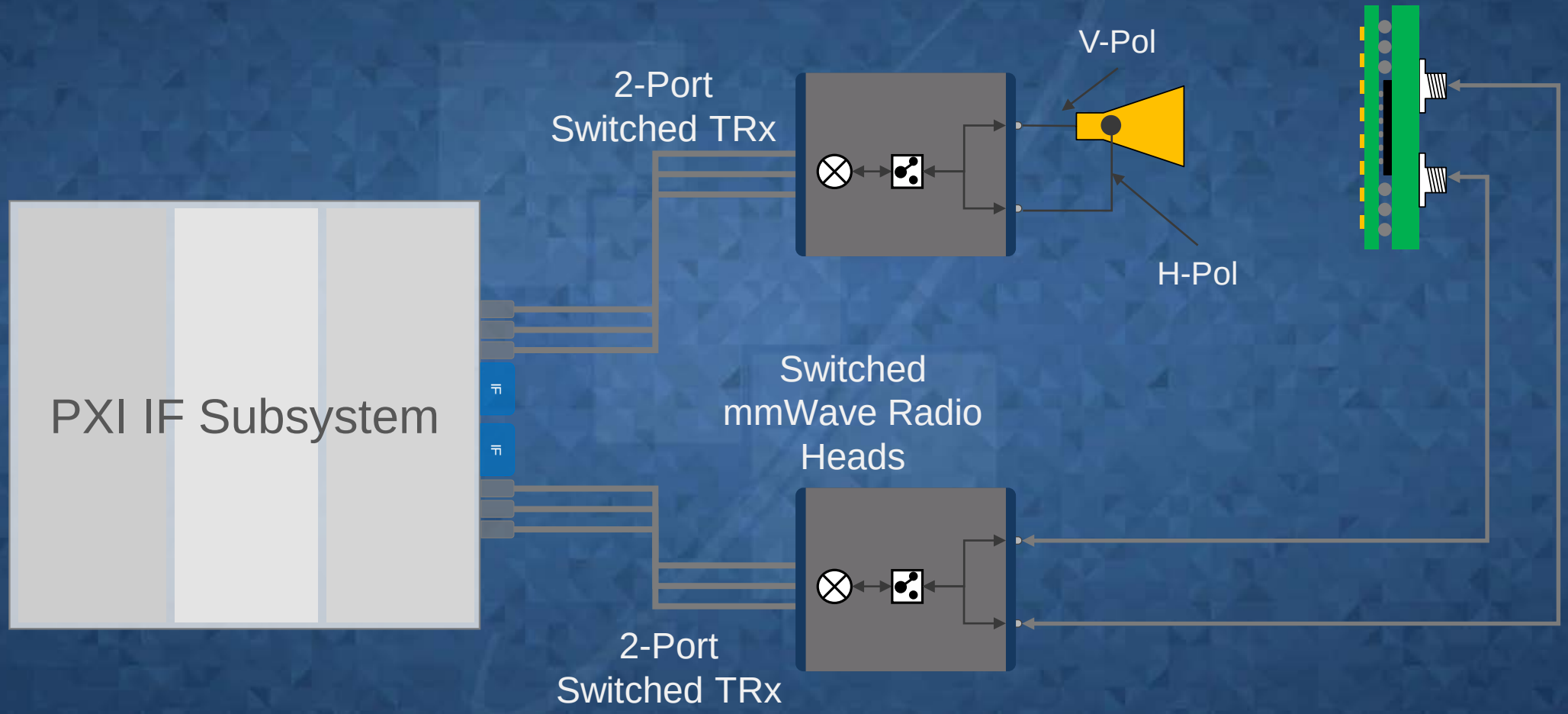


Alternate Configurations:

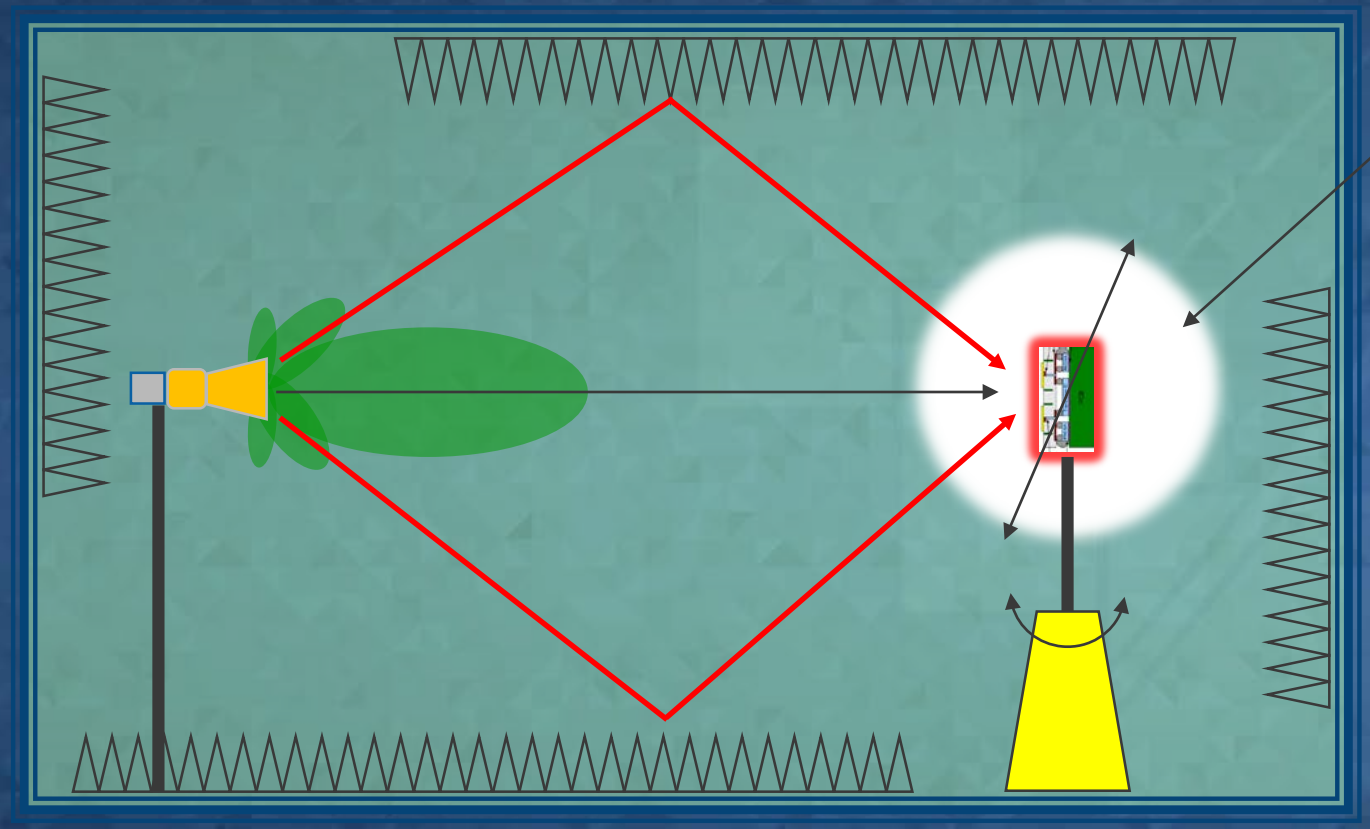
- Separate Tx and Rx I/O
- One IF port for single polarization

mmWave VST OTA Example Configuration:

Single or Dual Polarization RF-RF Phased Array Antenna Module



OTA Tests Need a Quiet Zone



Quiet zone

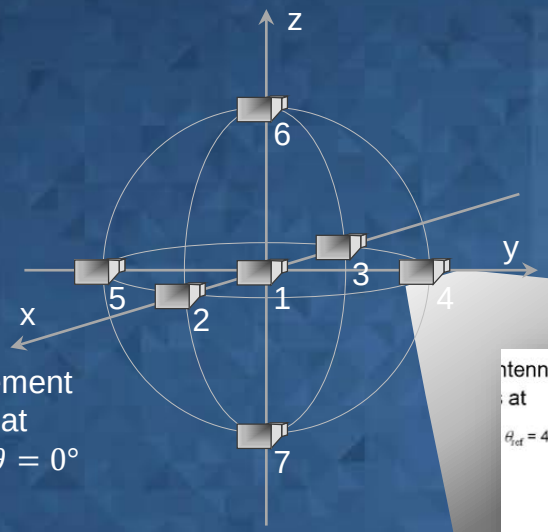
- Minimized power and phase variations due to reflectivity
- Approximating far-field, plane wave conditions

Quiet zone size S

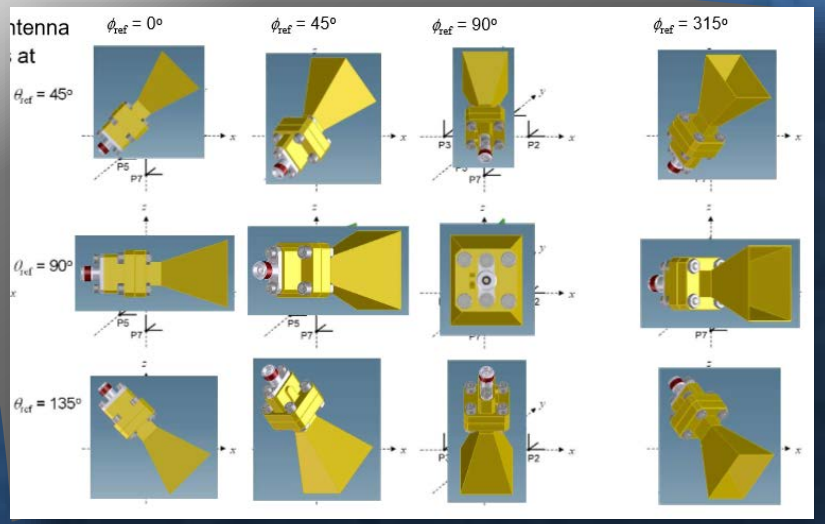
- Must accommodate antenna under test
- Bounded by desired maximum variations
- Influenced by chamber design including absorbers, positioner, fixturing, cabling, …

3GPP: Characterize the **NR mmWave** Quiet Zone

Reference Positions and Orientations, Polarization



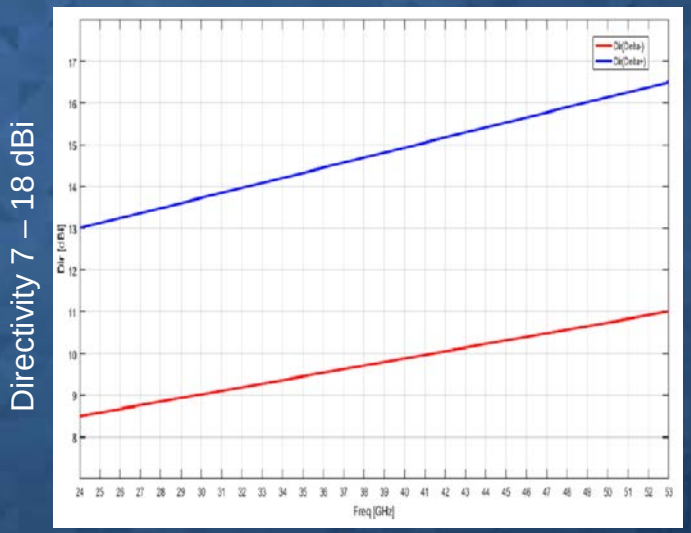
Measurement antenna at $\phi = 0°, \theta = 0°$



- 7 positions
- 26 orientations
- 2 polarizations

Reference AUT (ref. antenna)

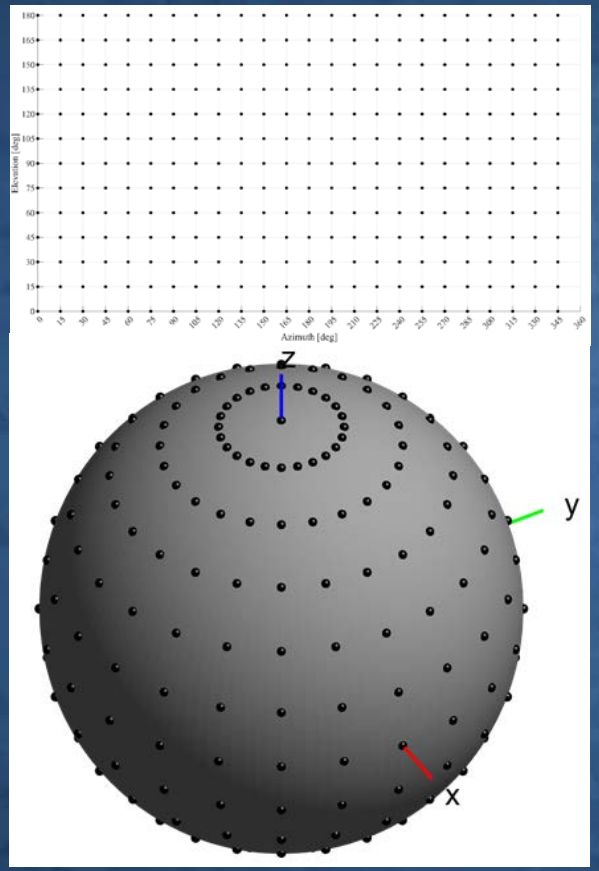
- Directivity similar to expected DUTs
- 3GPP defines directivity mask (min/max vs. frequency)

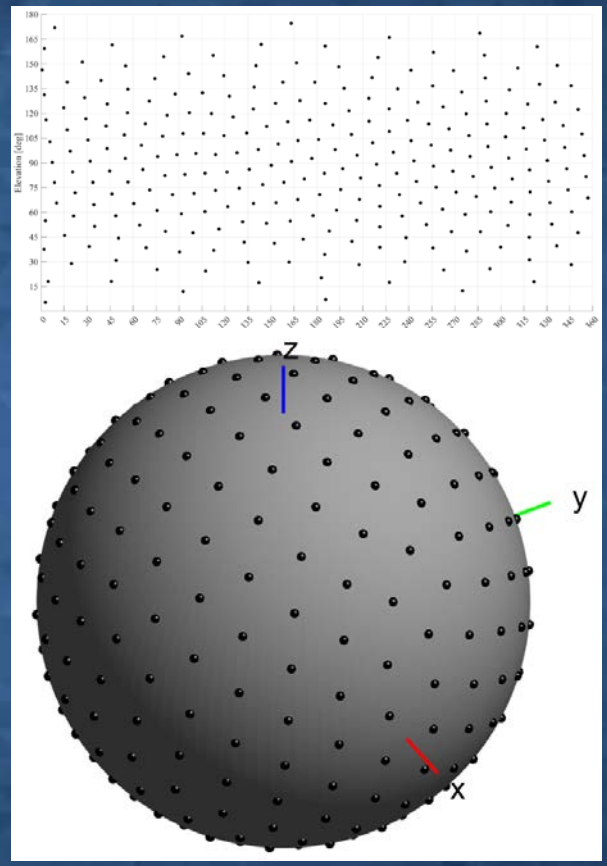


Frequency 24 – 53 GHz

See 3GPP TR 38.810 v16.0.0, §D

Spatial Scanning Grids





constant step size grid with $\Delta\theta=\Delta\phi=15^{o}$ - 266 points

mmWave VST for Over-the-Air Test

Software

Hardware

Test Execution

- Sequencing
- DUT Control
- Sweeping
- Position Control
- Measure

User Interface

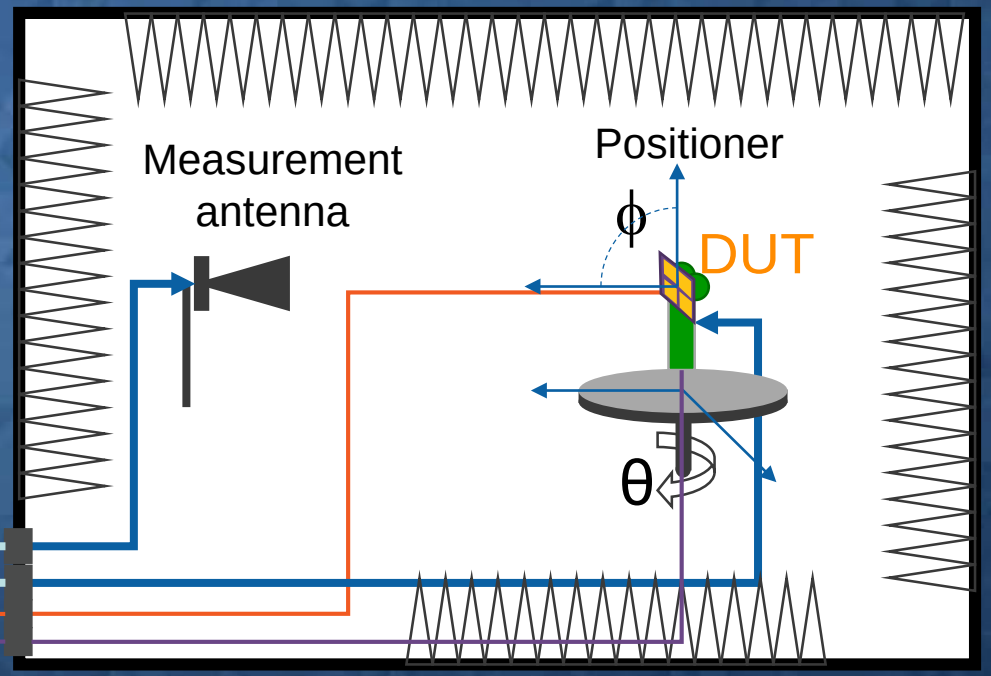
- Configure
- Visualize
- Post-process

Instruments

- mmWave
- DUT Control
- Position Control

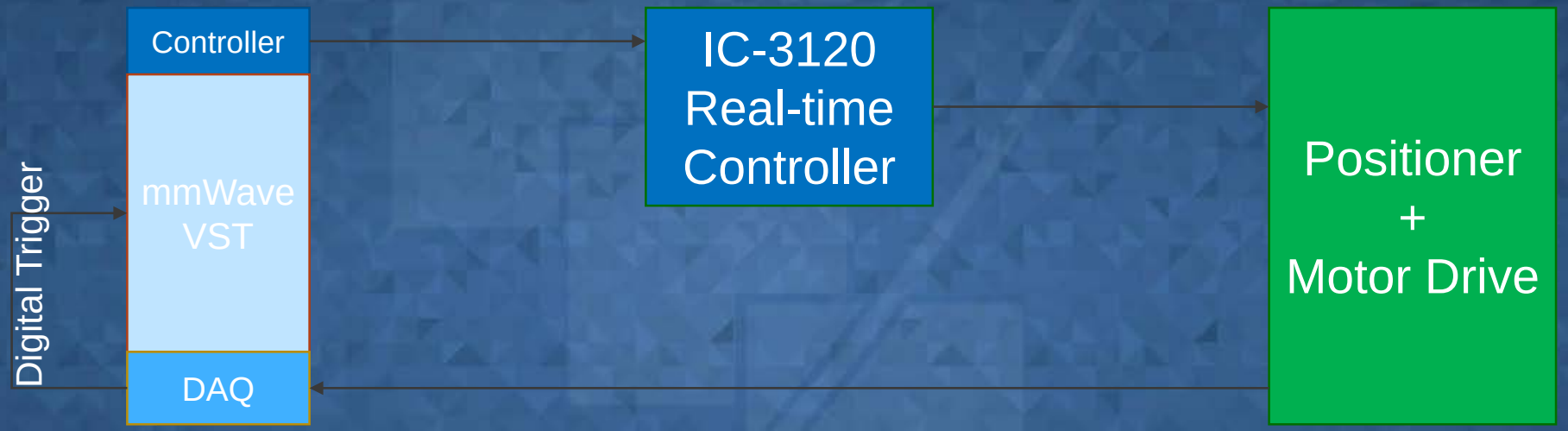
Switching & Conditioning

OTA Chamber



Reference antenna

Improving Test Time with HW-accelerated, Continuous Motion



- Patented positioning – instrumentation synchronization
- 5x or greater measurement times than SW-controlled solutions

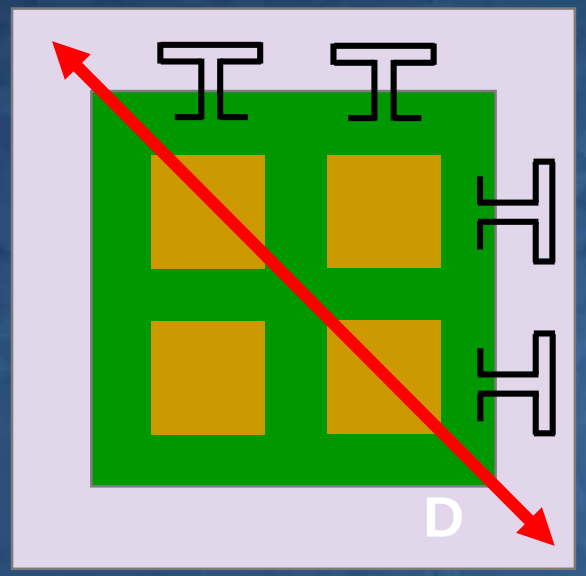
NI mmWave OTA Validation Test – HW Accelerated

Benchmark

No. of grid points (constant density)	Competitor - Turntable 360° Rotation 160° elevation Measurements every 4°	NI HW-Timed 360° Rotation 180° elevation
Test Setting	4-Port CW Measurements, simultaneous H-V polarization	5G NR Waveform, independent H and V sweeps
3600	540 s (9 min)	84 s

6X Faster

Device under Test



Types within focus:

- IF to RF phased array + antenna
- RF to RF phased array + antenna
- Baseband to RF + antenna

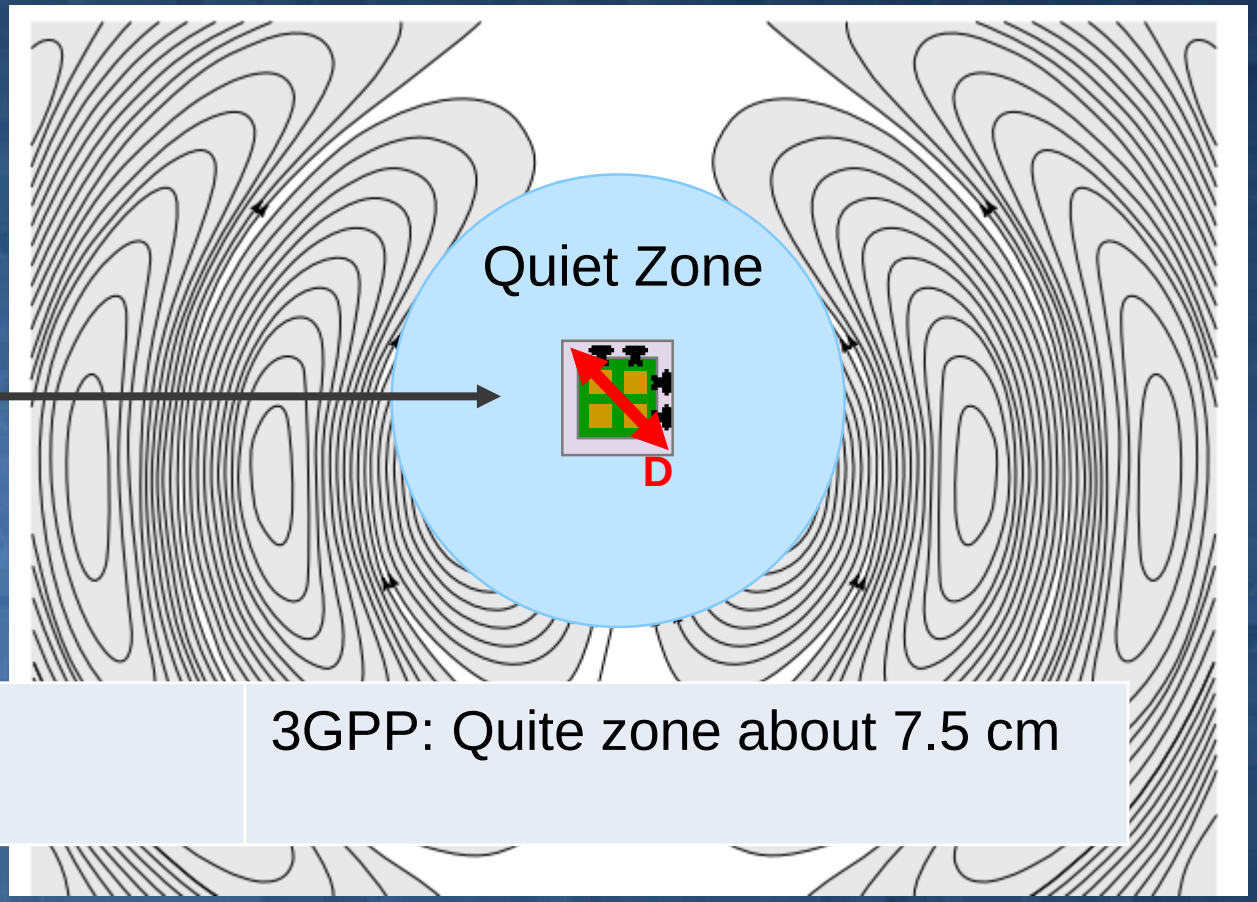
Size/aperture “D”

- No more than 5 cm (for UE, small cells)
- Determines – through far-field distance –
  - Chamber size

Space Requirements

Far field conditions at

$$r > \frac{2D^2}{\lambda}$$



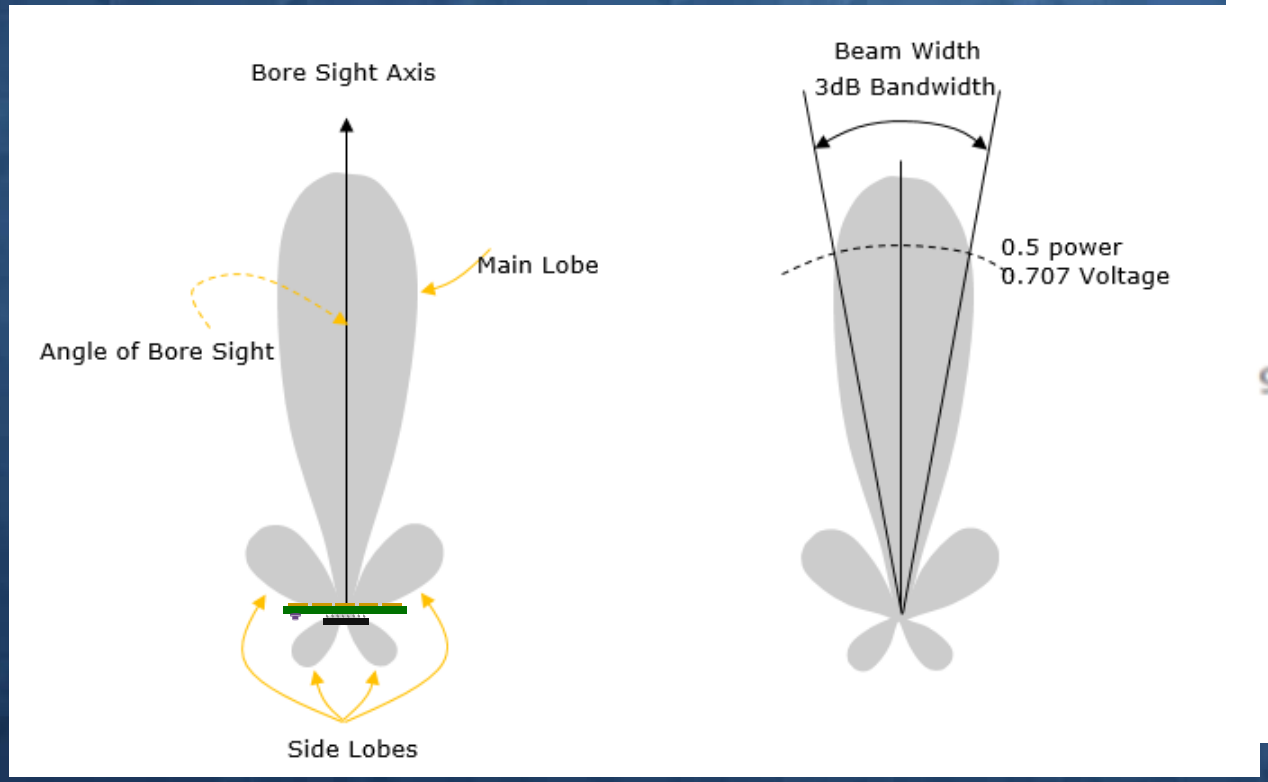
28 GHz D = 5 cm	r > 47 cm	3GPP: Quite zone about 7.5 cm

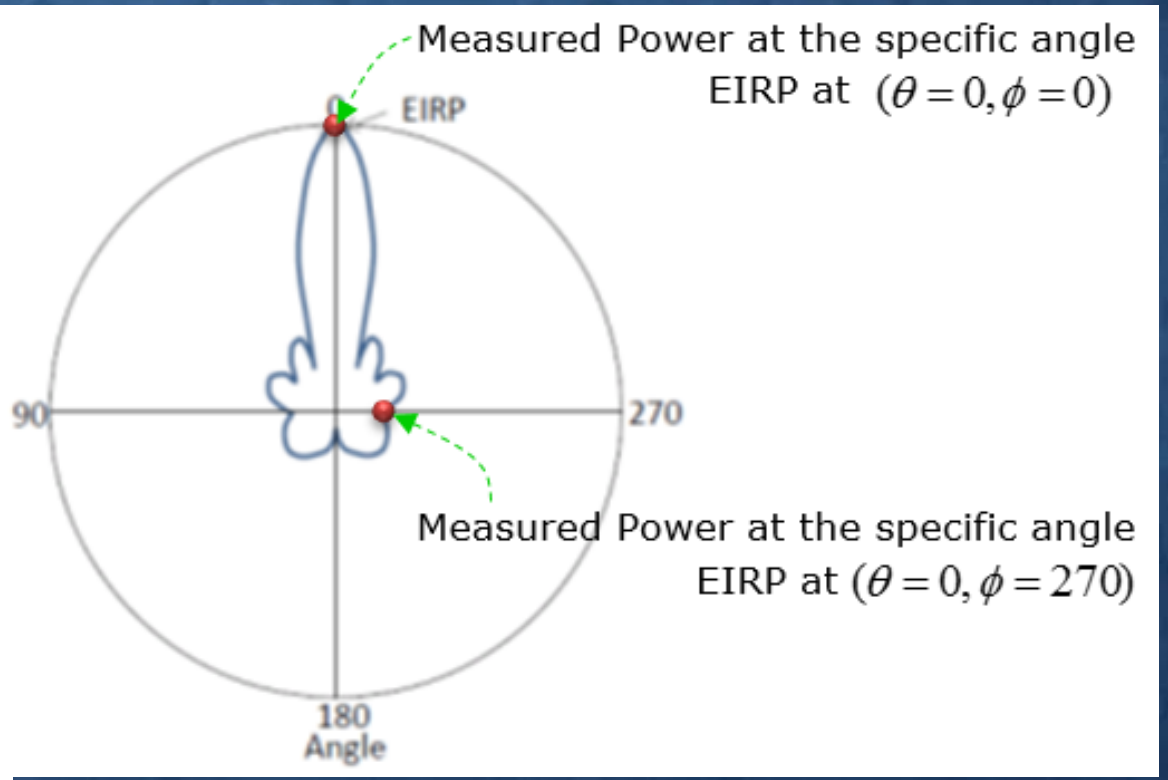
➔ Chamber size maybe 1.5m x 1m x 1m

Effective Isotropic Radiated Power (EIRP)

$$P_{Rx} = P_{TE} - PL_{Rx} + G_{Rx}$$

Measurement antenna (Rx)





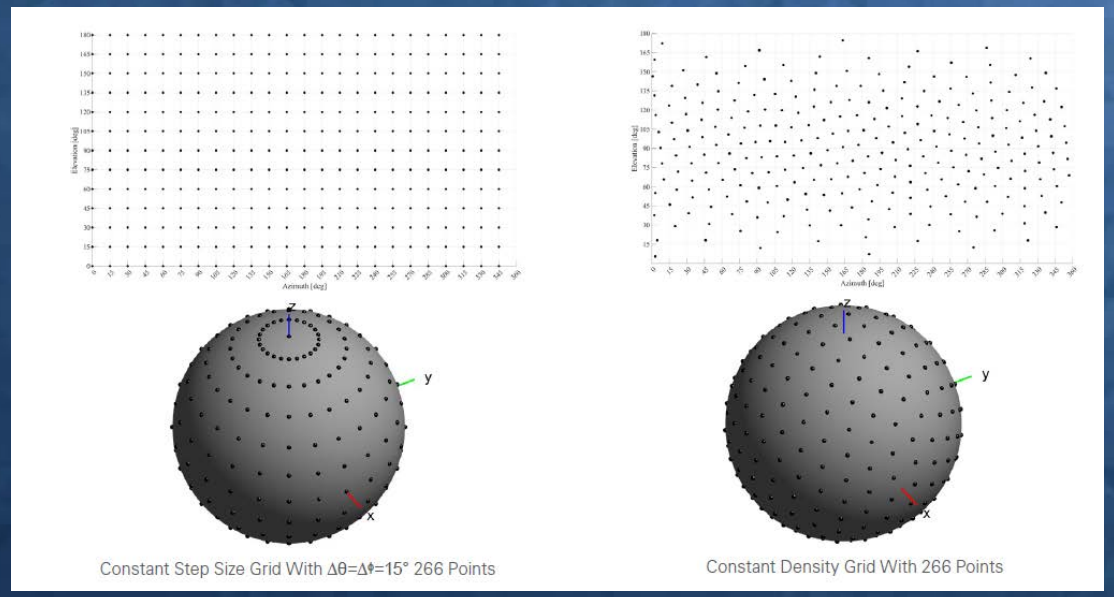
Total Radiated Power (TRP)

$$P_{Rx} = P_{TE} - PL_{Rx} + G_{Rx}$$

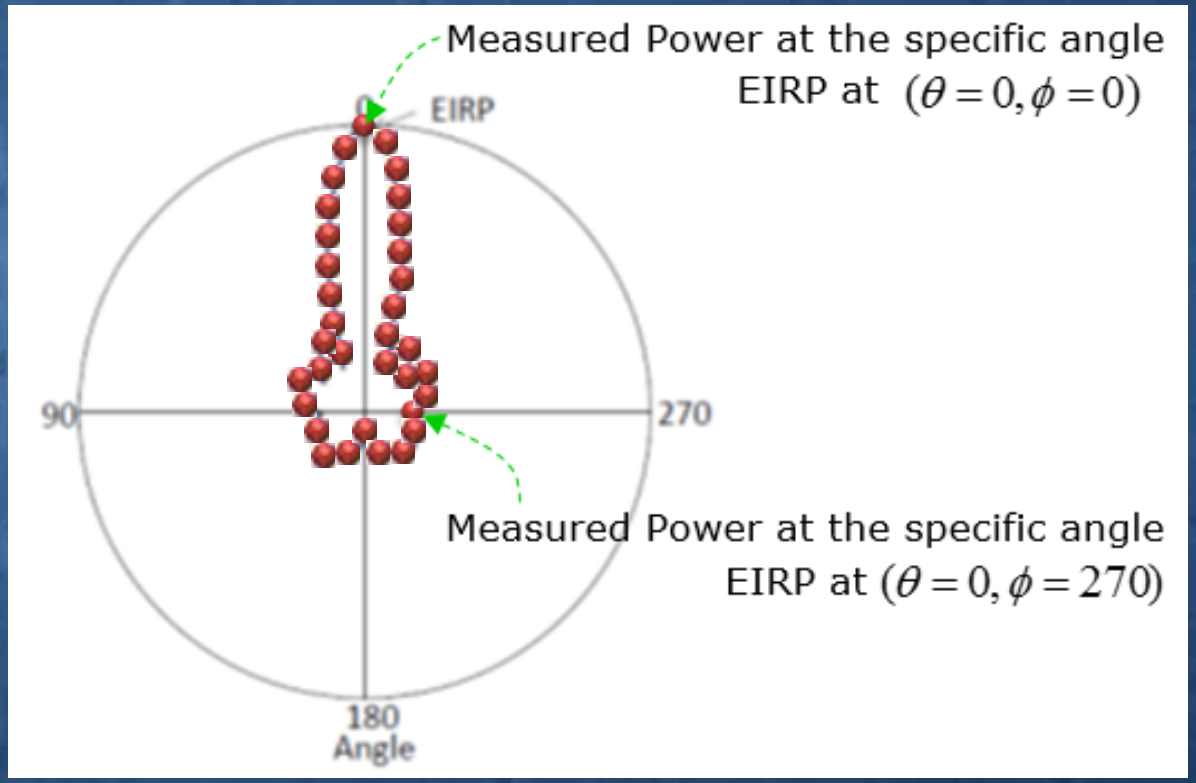
$$TRP = \frac{1}{4\pi}\int_{\theta=0}^{\pi}\int_{\phi=0}^{2\pi}(EiRP_{\theta}(\theta,\phi) + EiRP_{\phi}(\theta,\phi))\sin(\theta)d\phi d\theta$$

$$TRP \cong \frac{\pi}{2NM}\sum_{i=1}^{N-1}\sum_{j=0}^{M-1}\left[EiRP_{\theta}(\theta_i,\phi_j) + EiRP_{\phi}(\theta_i,\phi_j)\right]\sin(\theta_i)$$

Directivity = EIRP - TRP



Measurement antenna (Rx)



NI help you make 5G real !

SWTEST ASIA 2019

Ultra High Temperature Probe Card Solution for Automotive IC Testing

FormFactor™

Hirofumi Nagata
Alan Liao

Hsinchu, Taiwan, October 17-18, 2019

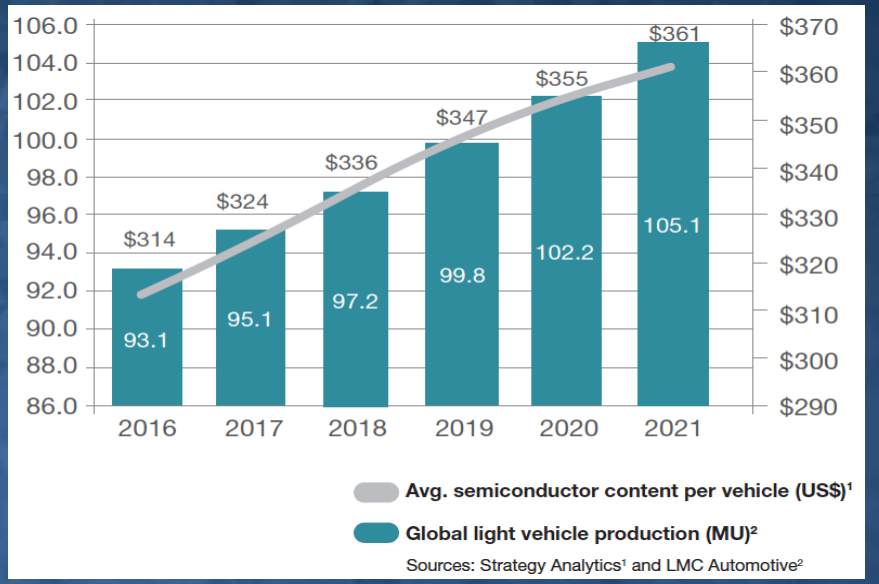
Agenda

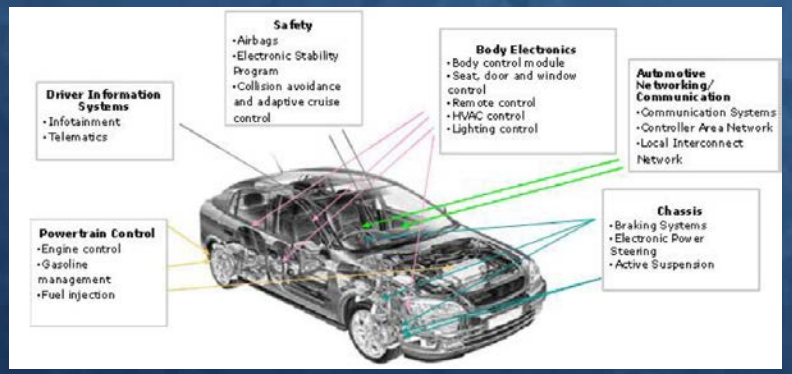
- Automotive IC Market Overview
- Automotive IC Test Requirements and Probe Card Challenges
- FormFactor Ultra High Temperature Probe Card Solution
- Probe Characterization Result Under Ultra High Temperature Testing Environment
- Actual Probe Card Performance Result by Leading Automotive IC Customer
- Summary and Acknowledgement

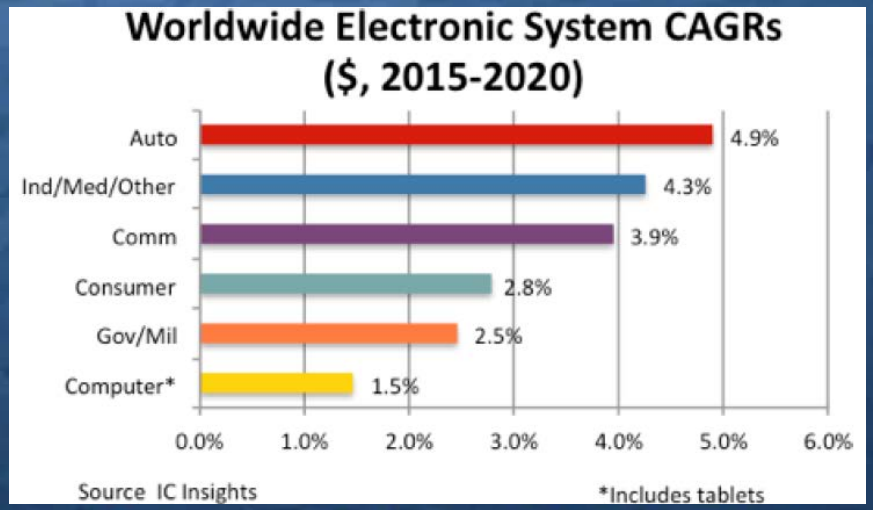
Automotive Semiconductor Market Overview

Drive Demand of New Testing Solution

- **Automotive electronics is a fast-growing market**
  - Predictions are between 3%~12% CAGR over next 5 years
  - Average number of semiconductors in a car increases significantly in modern cars
  - Key drivers for automotive IC growth
    - Critical safety system
    - Increased fuel efficiency
    - Navigation and communication
    - Comfort & entertainment features







Automotive Safety Consideration: Zero Defect Expectation

- **IC manufacturers adopt zero defects Parts per Million (DPPM) design methodology and test to this standard**
  - Finding tennis ball in football field
- **Reasons:**
  - Failure rate at the automotive level is higher
  - massive recall and serious economic distress
- **Probing Requirement:**
  - No Dielectric punch-through

Automotive IC Wafer Sort Test Challenges

- **Harsh outdoor environment**
- **Testing at full thermal range**
- **Minimize bond pad reliability impact**
- **Support large volume demand**
- **Lower test cost**

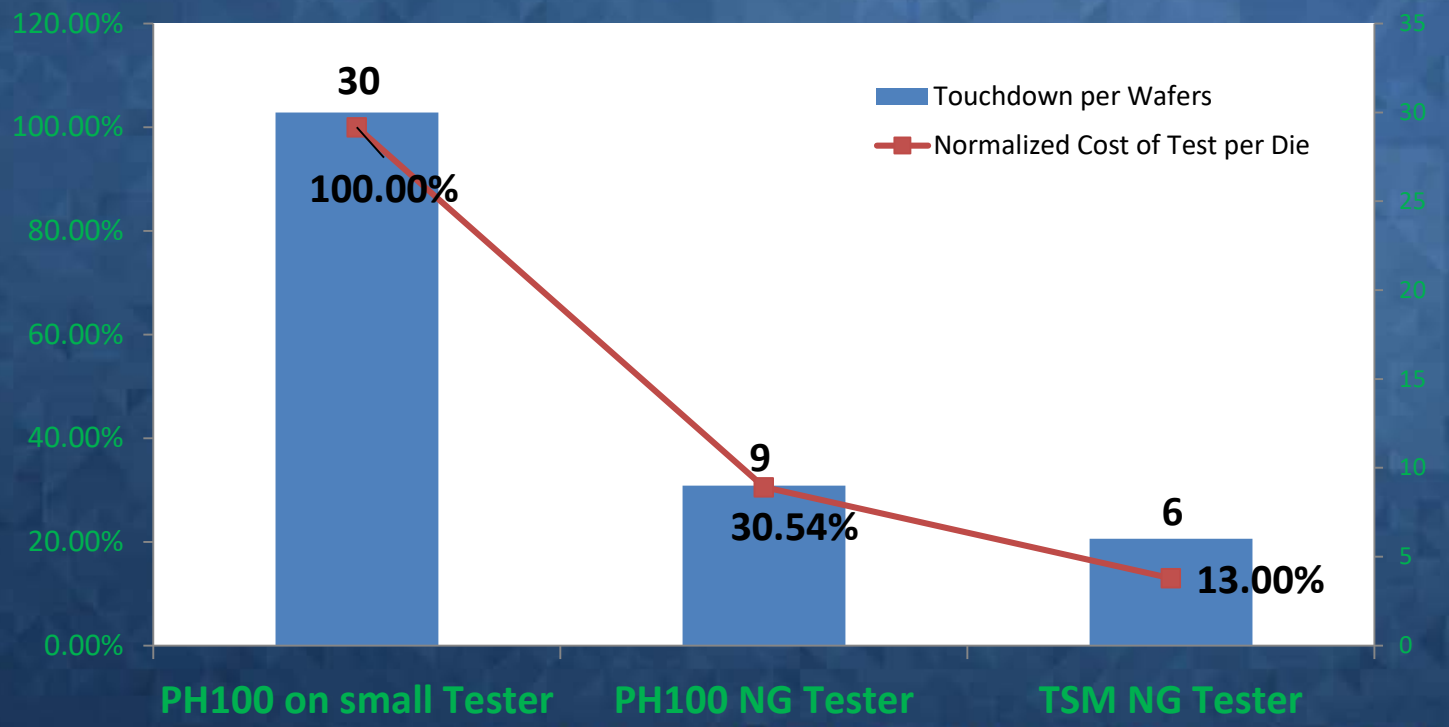
Probe card requirements:

- Wafer sort test with multiple insertion: cold, room, hot temp
- High temp test required
  125°C → 150°C → 175°C
- Multiple TD at same bond pad
- Large active area + high parallelism for SoCs

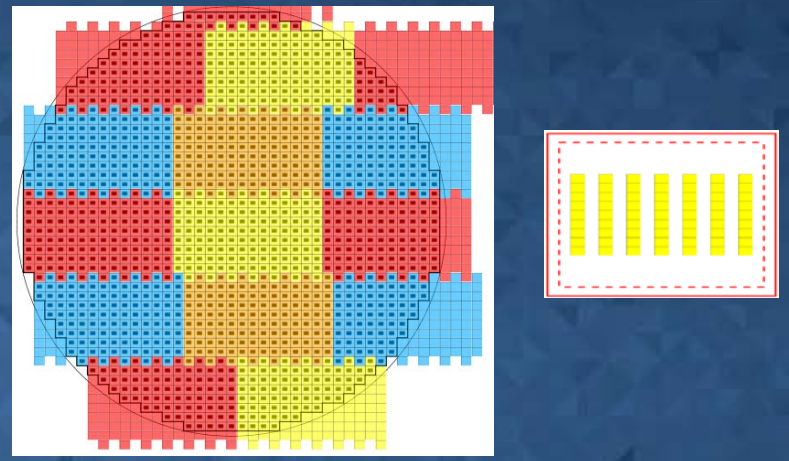
Increase Test Efficiency = Reduce Cost of Test

Maximize Number of DUTs to Reduce Number of TDs

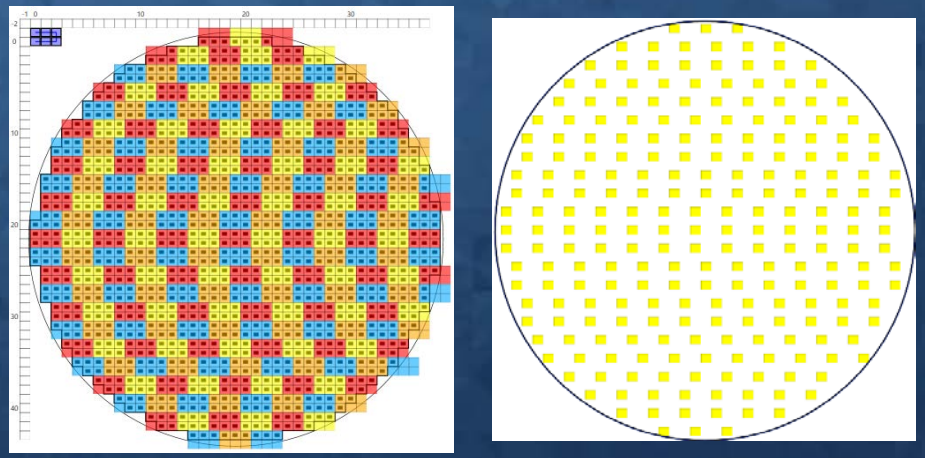
- **Require Full Wafer Touch Down Maximize Touch Down Efficiency**
- **Increase Touch Down Efficiency to Reduce Cost of Test**



30 TD 63 DUT PH100 Touch Down Pattern



6 TD 234 DUT Full Wafer Contact TD Pattern

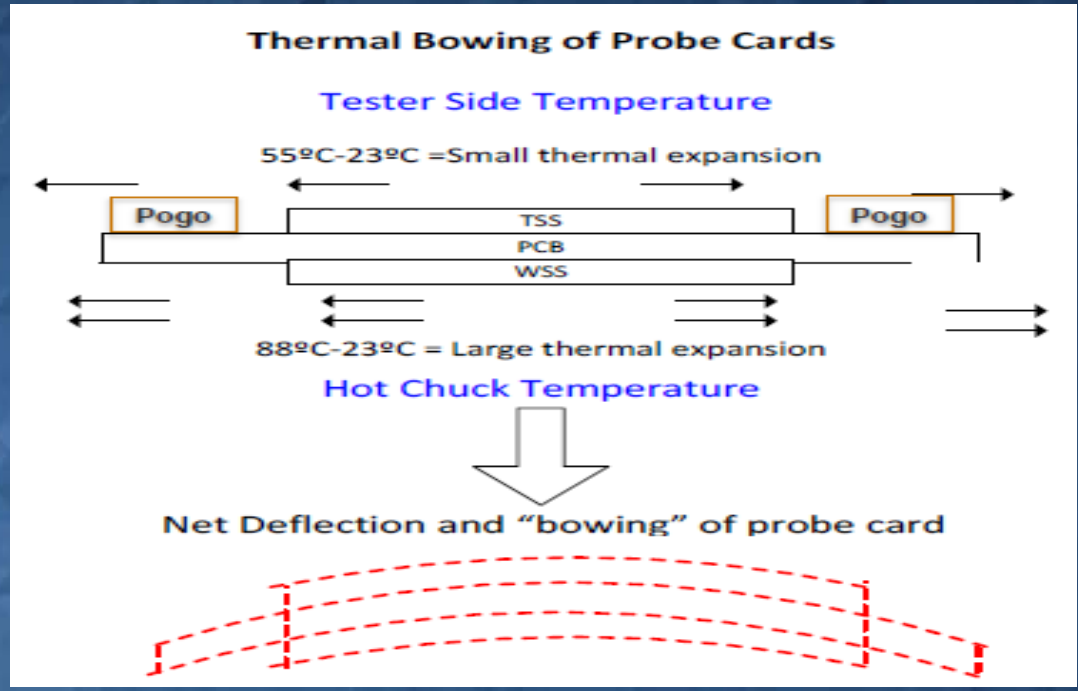


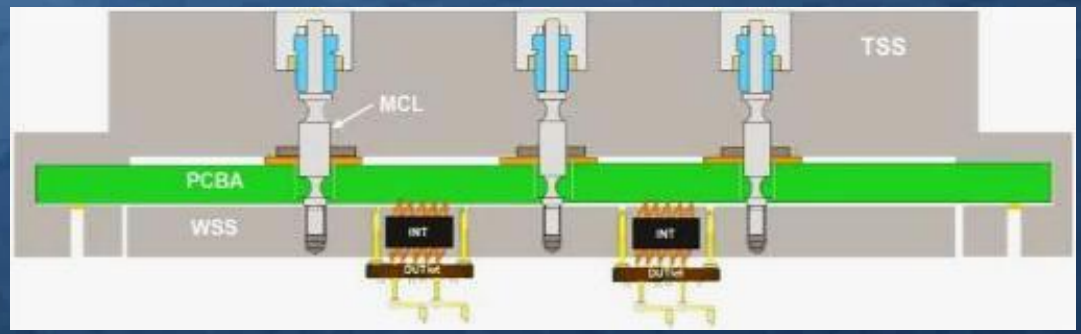
TrueScale Matrix Probe Card

Thermal Planarity Control

- **Thermal gradients in probe card produce differential expansion across probe card components and can produce probe card bow**

- **Design and build the probe card for better thermal planarity control**
  - Mechanical simulation to understand thermal behavior
  - Design automation (real-time probe card deformation simulation) to optimize **M**echanical **C**oupling **L**ink location for planarity control
  - Added flexible shim kit design on inner tester side stiffener
  - Bridge beam hardware add to PC outgoing PXI metrology tool to simulate test head docking condition for planarity adjustment
  - AOT/POT analysis on field to further understand deflection force



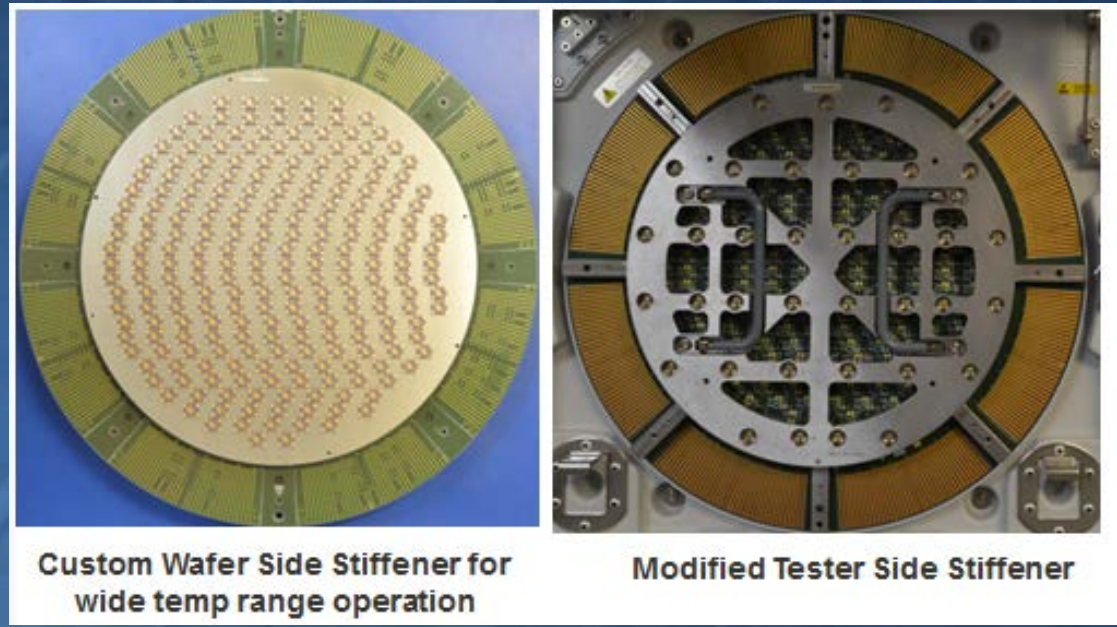


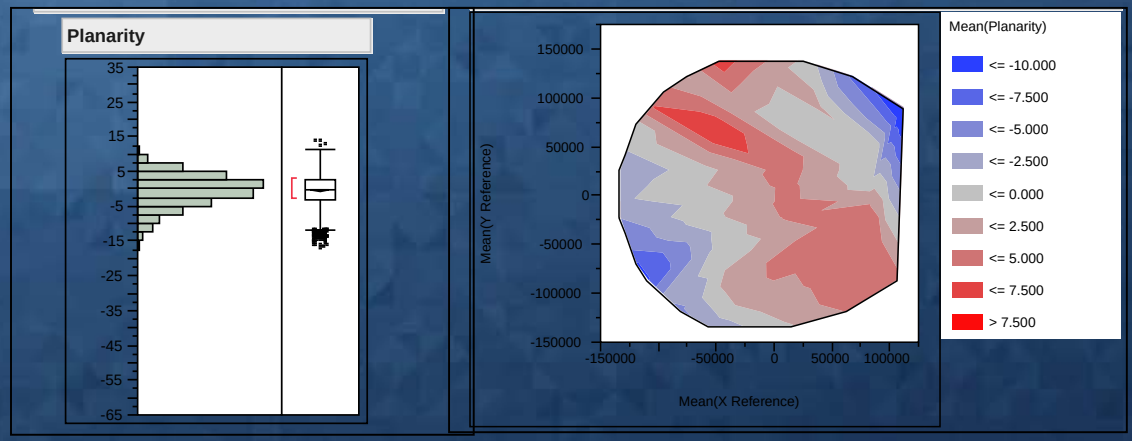
TrueScale Matrix Probe Card Architecture

Optimize for High Parallelism and Ultra High Temperature

- **Probe Card Design Requirements**
  - 300mm probing active area
  - Support >256 DUTs, >35000 Probe Count
  - Smallest Pad Size and Pitch: ~55um/65um
  - Temperature Range: -40 to +165°C

- **TSM PC Achieved Large Active Area with Highest Parallelism**
  - Full 300mm active area probing to improve touchdown efficiency
  - FFI proprietary touchdown efficiency analysis software and service
  - T11 UHT Probe Rated -40 to +175°C
  - Modified TSS and Matrix architecture achieved 30um planarity





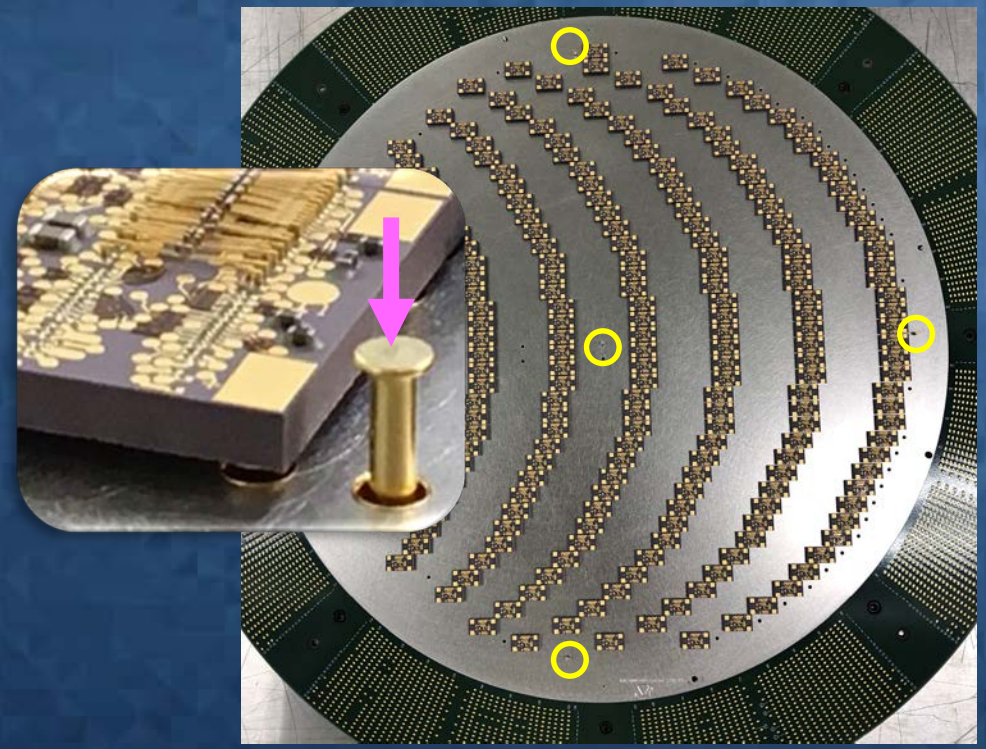
DragonBlade T11.4 Ultra High Temperature Probe

Metric	T11	T11 UHT
Max Temperature (°C) / AOT (um)	<=130°C/75um <=160°C/65um	**175°C/100um**
Min pad Pitch (um)	50um	60um
Scrub Ratio	~10%	
Current Carrier Capacity (ISMI)	1.2A	>1A
Typical spring constant (gram-force / mil)	0.8 g/mil	
Tip sizes at beginning of life (um)	6um, 8.5um, or 14um ±3um	
Tip sizes at end of life (um)	20um	

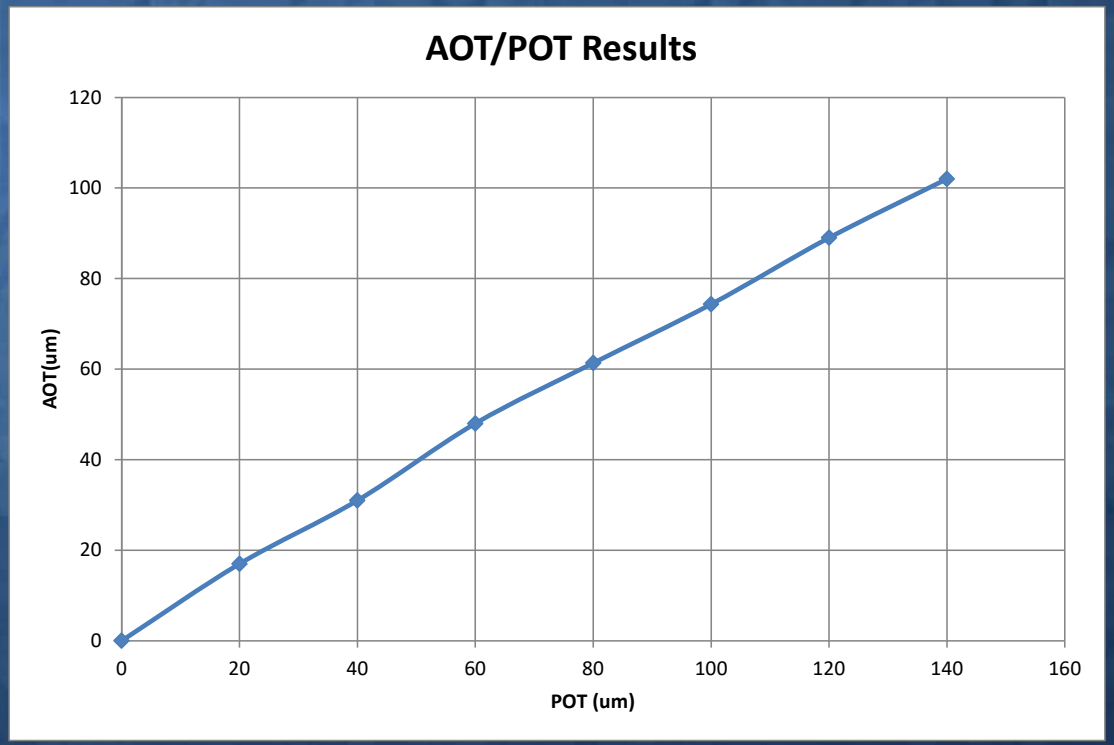
Actual Over-Travel vs. Program Over-Travel Analysis

- **Using Pin and Sleeve to analyze probe actual over-travel**

  Install Pin & Sleeve at 5 locations on the PH.
  Check that the pins have shifted upwards
  due to the chuck loading



AOT/POT Results ≈ 75%

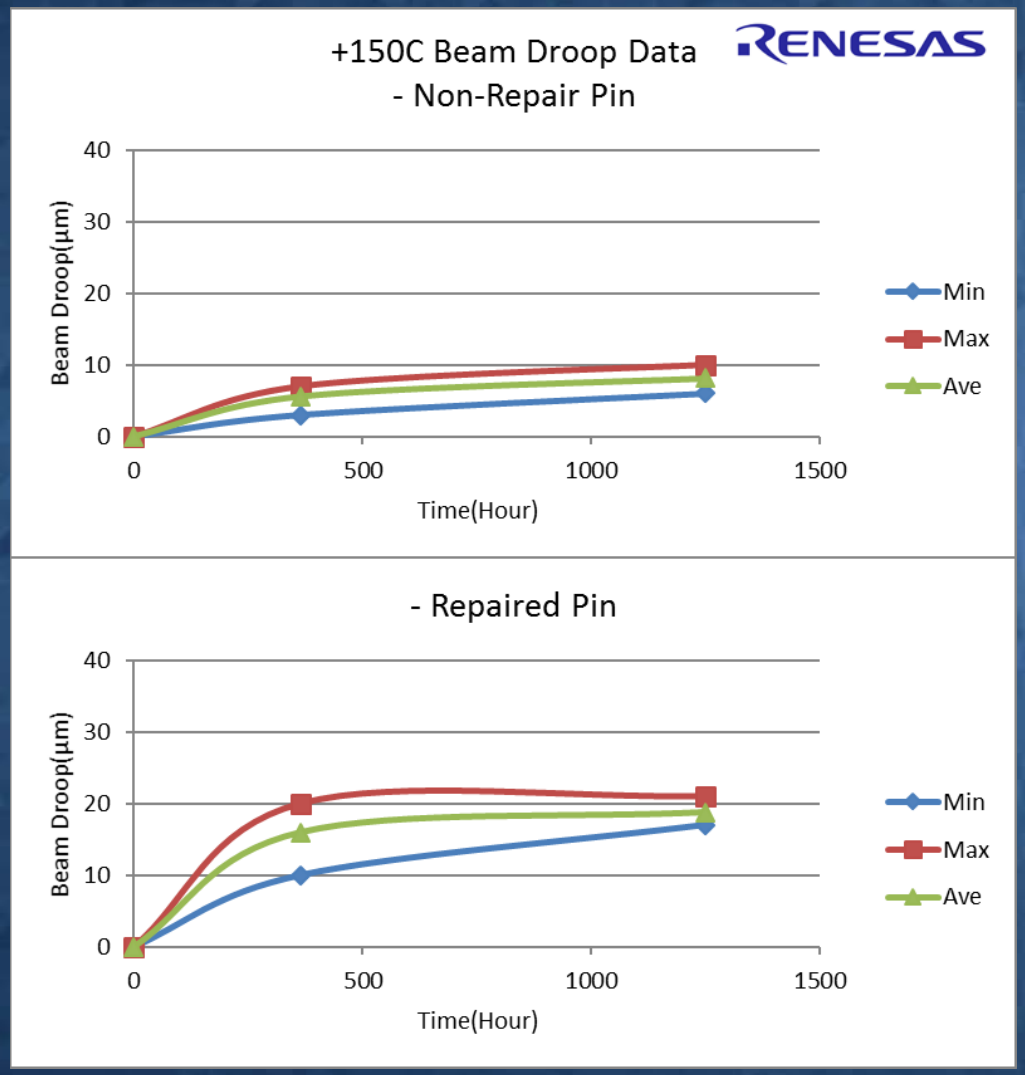


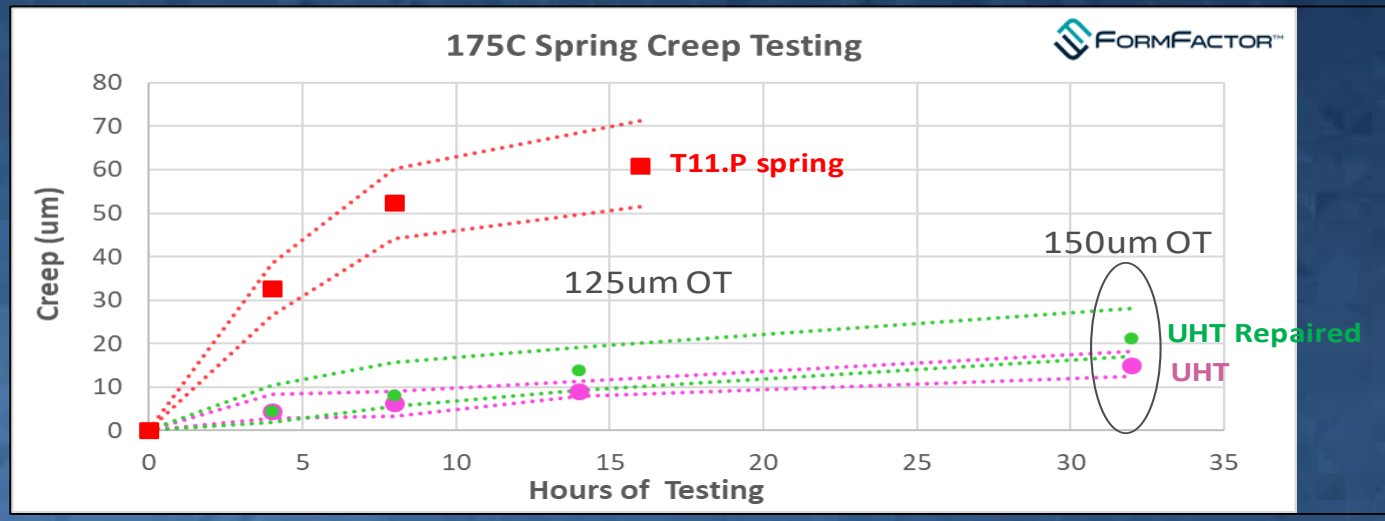
Final Result in Production Test Environment

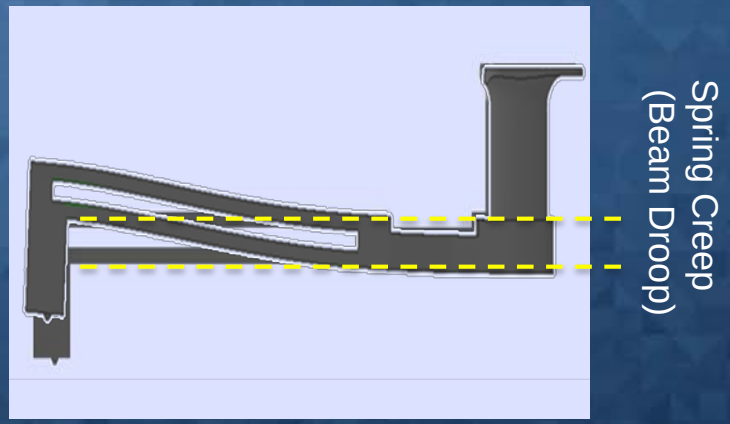
- **Renesas agreed to share their collecting data.**
  - Beam creep data
  - Contact Resistance
  - Probe Mark Characterization Data
  - Probe Mark Photos

DragonBlade T11.4_UHT Performance

Same capability as T11.2 with 2x hot temp performance

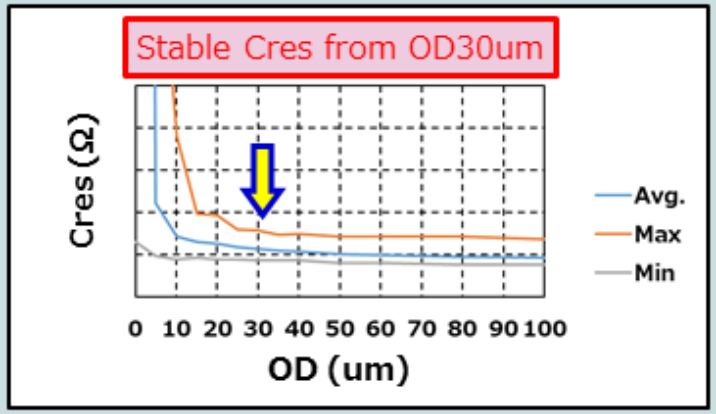
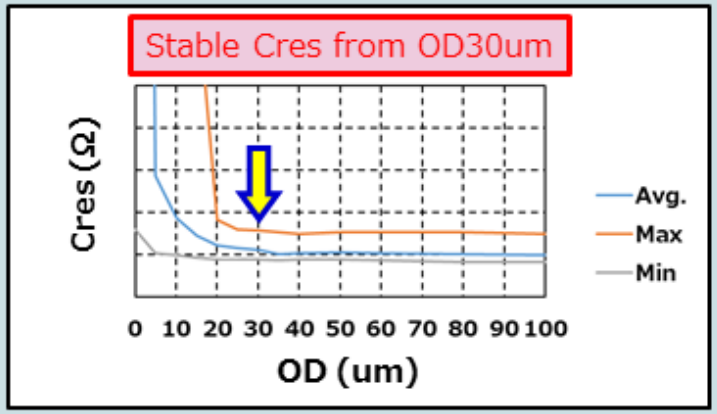
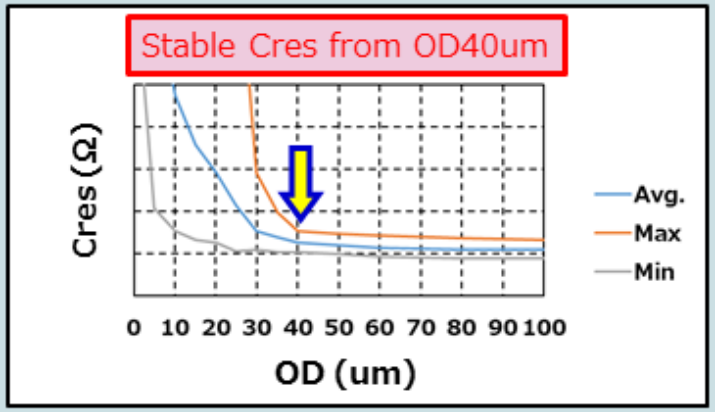






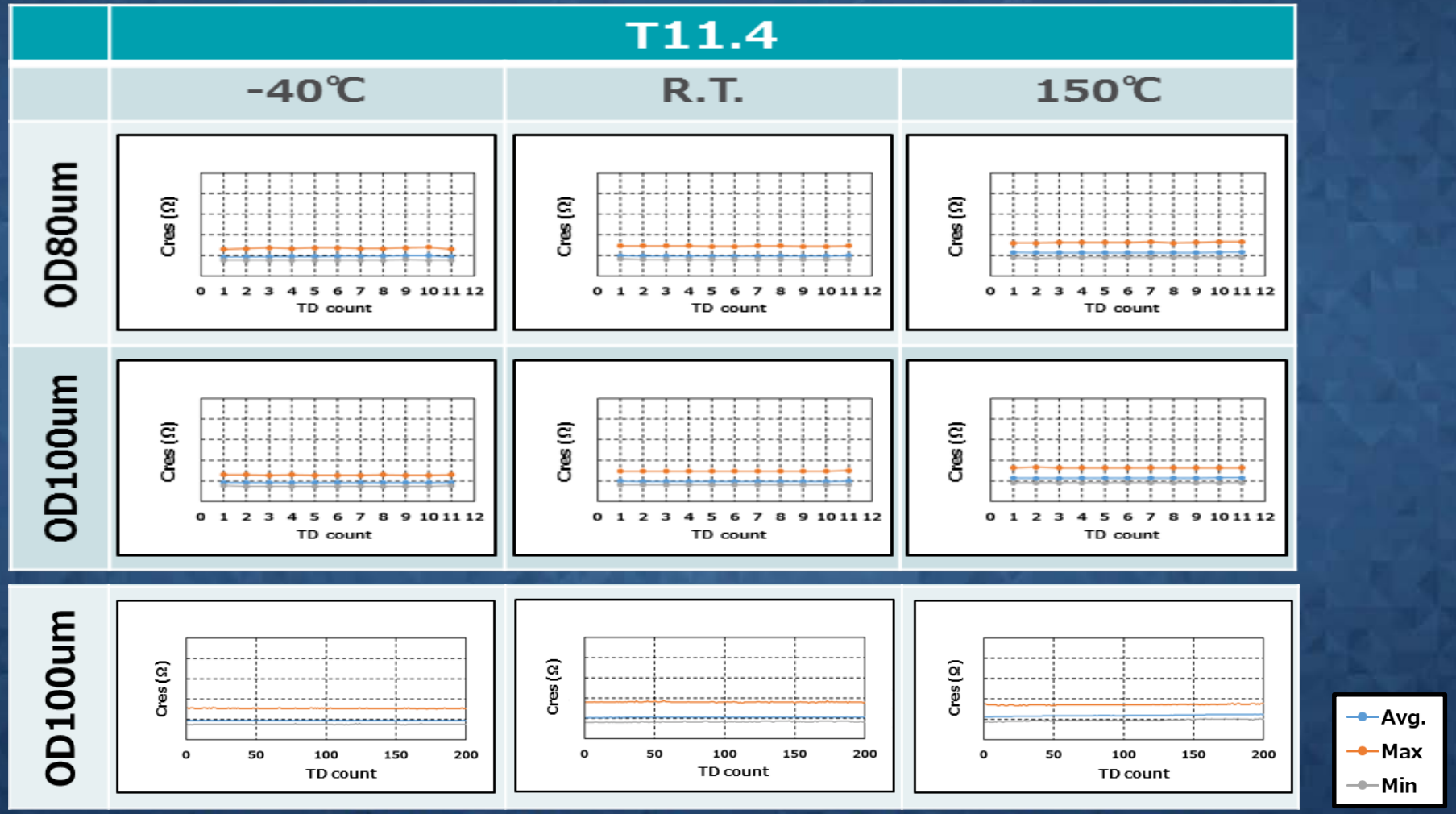
Contact Resistance vs. OD

- **T11.4 archived stable Cres from 30-40μm OD.**

	-40℃	R.T.	150℃
T11.4			

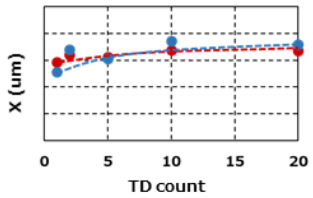
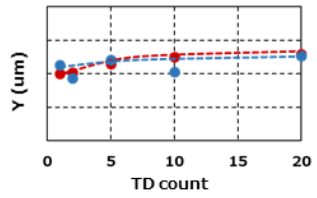
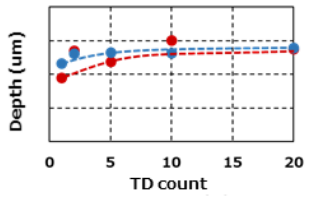
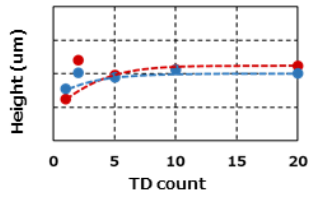
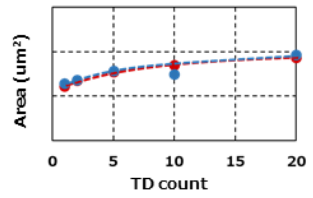
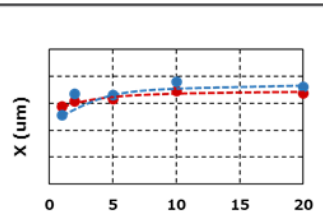
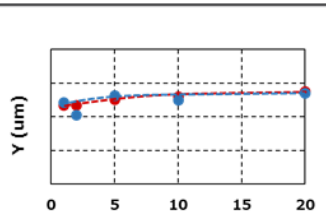
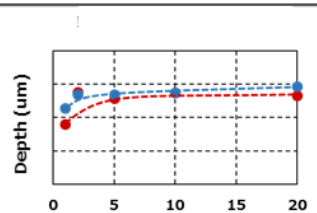
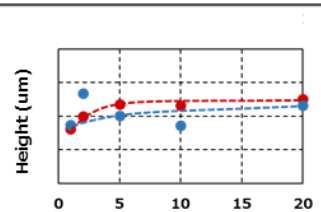
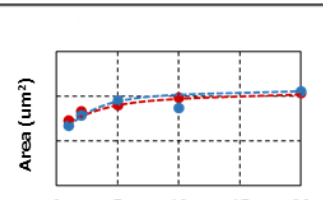
Multi-Contact Performance

- **T11.4 archived stable Cres for all cases.**
  - 10 times TD and move to new surface at 11th TD and 200 times TD test

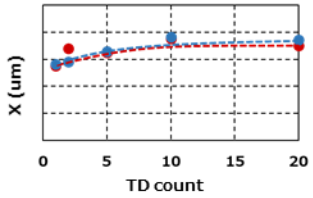
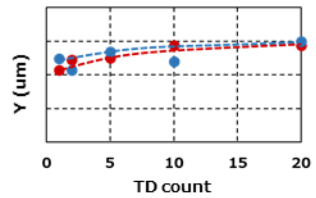
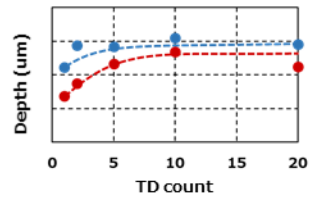
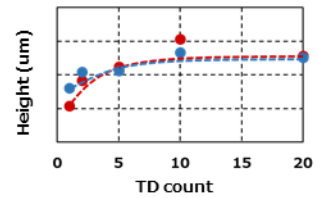
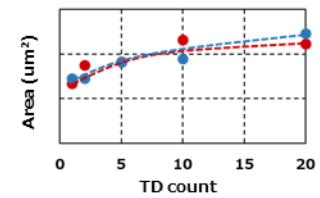
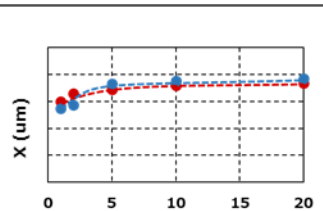
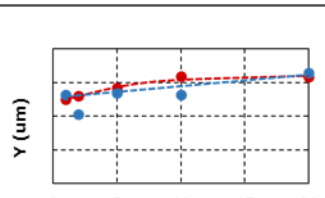
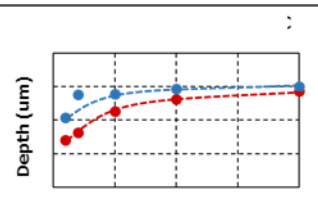
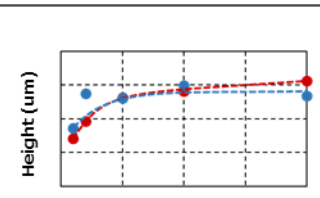
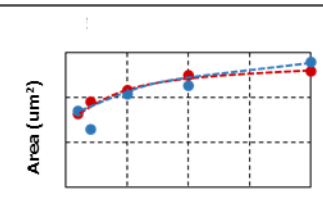


T11.4 Probe Mark Size Analysis

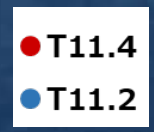
Probe Mark Size Past Extreme Temperature Test

	X-dim	Y-dim	Scrub depth	Prow height	Probe Mark area
OD80um					
OD100um					

Prober Chuck Temperature: -40°C

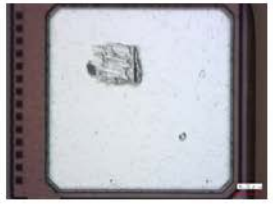
	X-dim	Y-dim	Scrub depth	Prow height	Probe Mark area
OD80um					
OD100um					

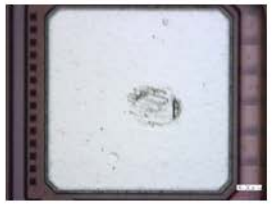
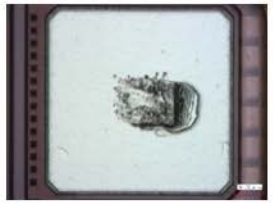
Prober Chuck Temperature: -160°C



T11.4 Probe Mark and Pad Reliability Analysis

No Under Pad Damage at 20TD

	Single TD	Multi-TD : 5 times	Multi-TD : 20 times
OD80um			
OD100um			

	Single TD	Multi-TD : 5 times	Multi-TD : 20 times
OD80um			
OD100um			

Cold Temperature: -40°C

Hot Temperature: -160°C

Summary

- Automotive IC market continues growing with large demand and zero defects parts
- FormFactor Matrix platform with T11 Ultra High Temp probe provides capability of meeting zero defect testing requirement and the highest testing efficiency for automotive IC wafer sort test
- TrueScale Matrix with T11 UHT probe solution has been validated by key automotive customer and deployed to various tester platforms including T2000, V93K DD, J750

Acknowledgement

Special Thanks!

Tom Watson

Engineering Follow

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Application Engineering Manager

Takahiro Mizoi

Senior staff engineer of test technology development dept

Space Transforming Probes
SWTest Asia

Dominik Schmidt, PhD
Gary Grube
Translarity Corp

Hsinchu, Taiwan, October 17-18, 2019

Agenda

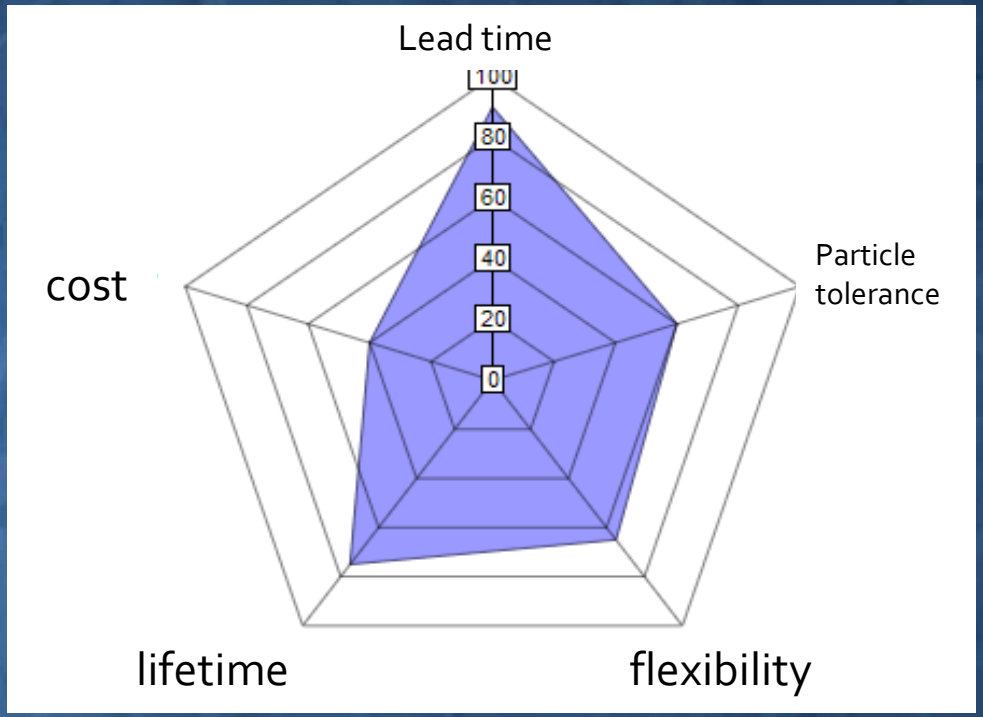
- Introduction
- Motivation
- Space-transforming Probes for Different Application
  - FLASH
  - LCDD
  - CMOS imaging/VCSEL/LED
  - Very tight pitch applications
- Conclusions/Future Work

Introduction – today's probecard issues

- Cost of space transformation is not scaling
  - MLO aimed at millions of units, not 10's units
  - MLOs take 8 weeks, large NREs and huge unit cost
  - LT Ceramics are difficult scale below 100um
  - HT Ceramics are difficult to process
  - Thermal issues becoming more complex across the board
- Fundamental problem: large PCB/silicon TCE mismatch results in need for strain relief
  - MLO delamination
  - Misalignment during operation
  - Moisture, BGA attach, force balancing…

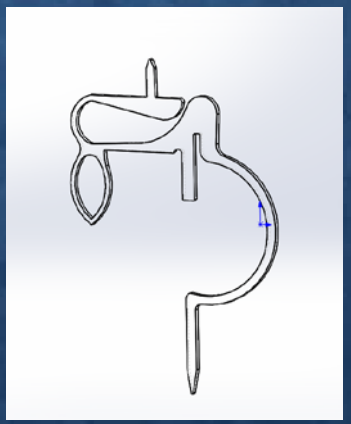
Motivation – can we improve across the board?

- Overall cost
- Lead time
- Particle tolerance
- Repeatability
- Field repair-ability
- Lifetime
- Flexibility and cost of design changes



The most versatile element is the probe

- Modern 2.5D MEMS processing can be used to create nearly arbitrary shapes
- Designs can now be “ported” between foundries
- Improvements in metallurgy mean that probes can be made extremely reliable
- Probe costs can be scaled with volume
- Unlike MLO, probes can be reused in multiple designs



The ideal probe

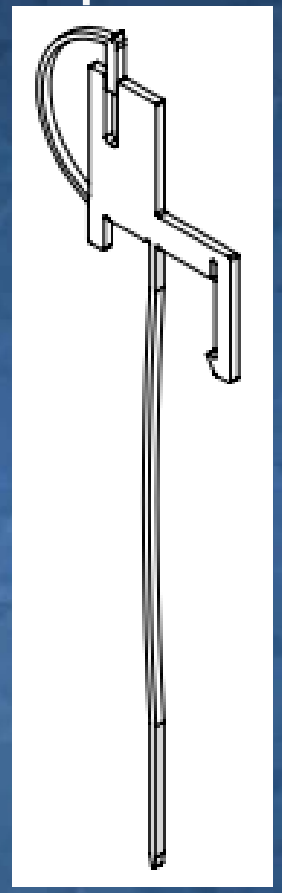
- No idea 'universal' probe
- Specific to lead-on-edge (single, dual and four-sided):
  - FLASH
  - CIS
  - VCSEL
  - LED
- High density in "1.5" dimensions
- This is approximately 40% of the probecard market today

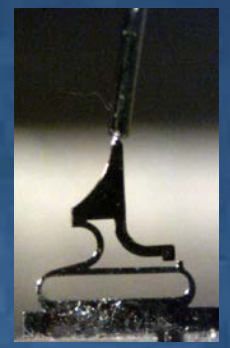
The ideal probe

- Pre-loaded to the PCB
  - Allows up to 100um of thermal movement (across 300mm)
- All electro-mechanicals comparable to best-in-class 80um MEMS (CCC, Planarity, Alignment)
- ALL space transformation enabled by the probe
  - 80um up to 400um FLASH/CIS (enabling simple PCB)
  - 20um up to 100um LCDD/LED (enabling "simple" flex/lamination)
- Simple 2D processing! Previous architectures generally used complex 3D MEMS

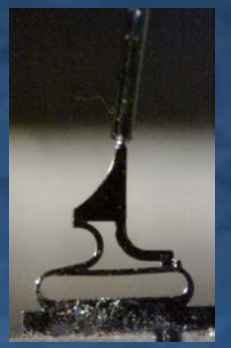
Space Transforming Probe Family (pat pending) for XYZ offset

- Leverages standard Translarity's 2D MEMS design portfolio. 39um, 50um, 65um, 80um
- Enables tighter pitch assemblies to connect directly to PCB
- Engineered scrub on both, PCB and wafer sides
- Configurable probe force. 1.5-8gf
- Utilizes standard test floor infrastructure – cleaning media, prober interface, etc.
- Configurable probe depth to match required prober integration
- Enables component placement in close proximity to the probe





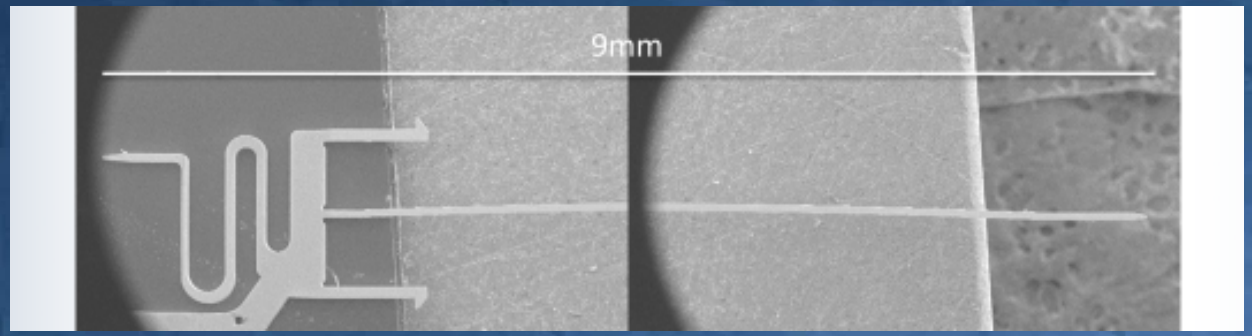
Probe at 0µm overtravel

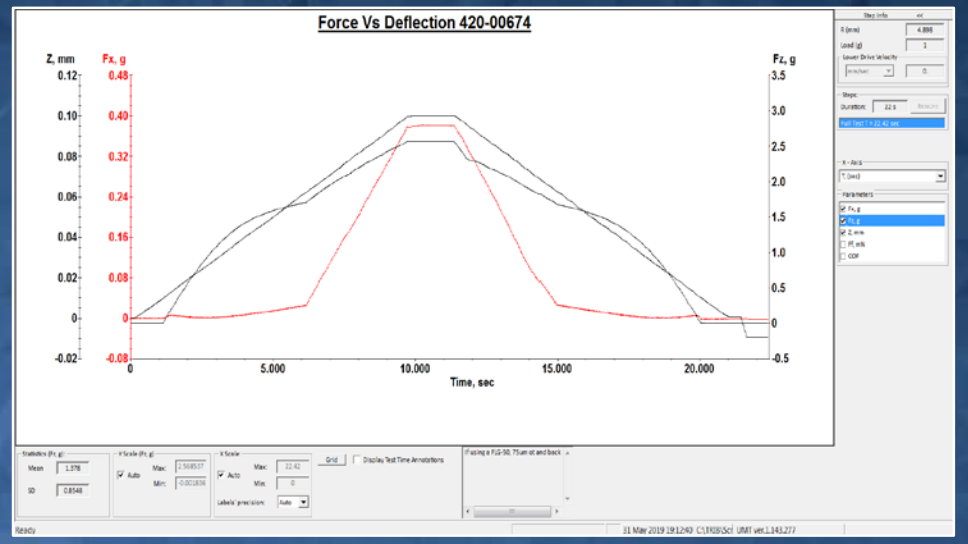


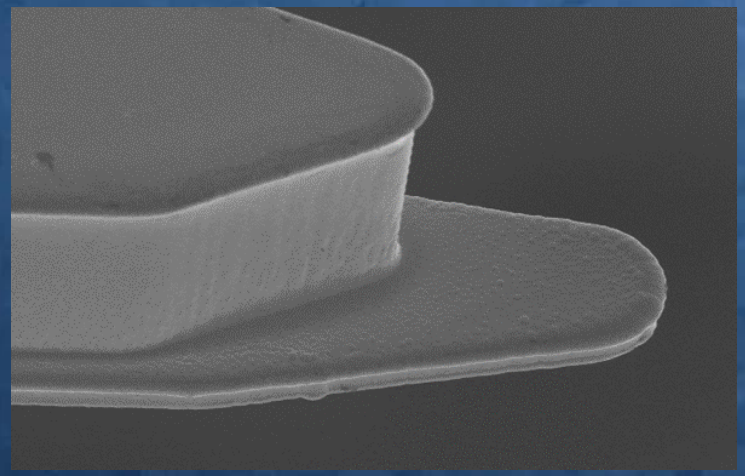
Probe at 100µm overtravel

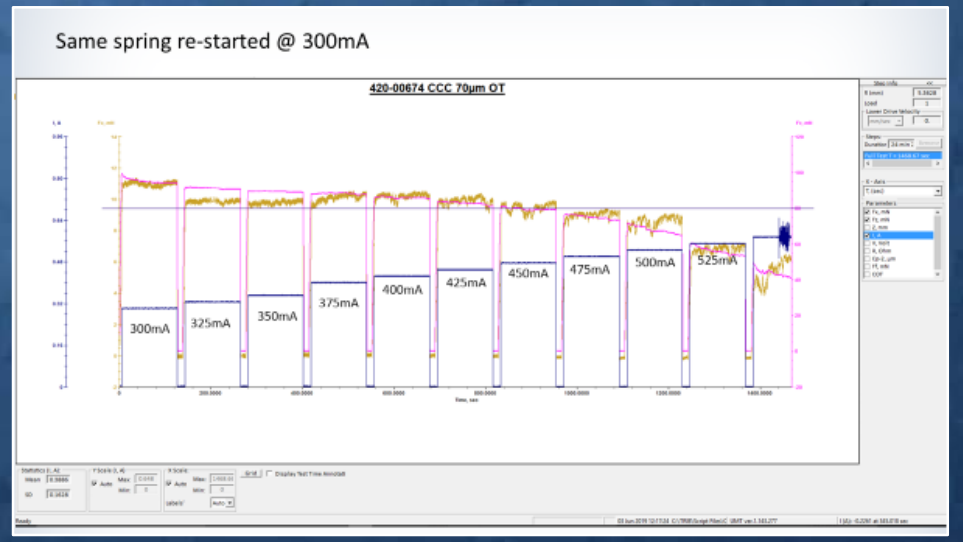
Allows probe lateral transformation consistent with all existing PCB Technologies

Tested across CCC, force, offset, space transformation, temp

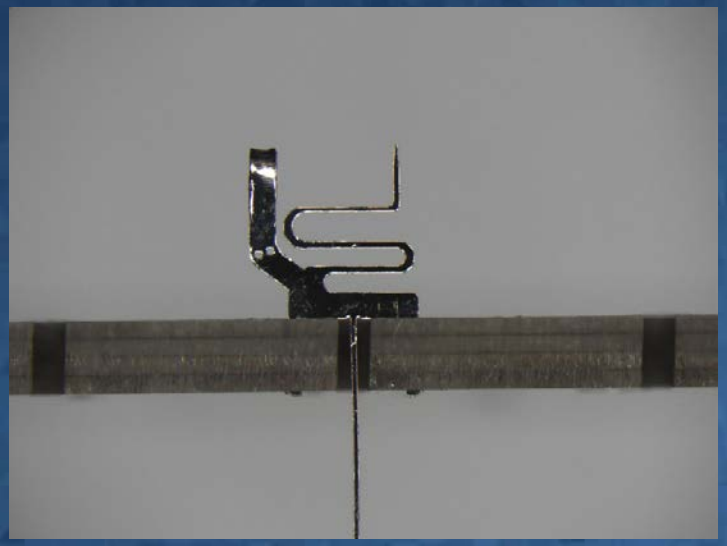


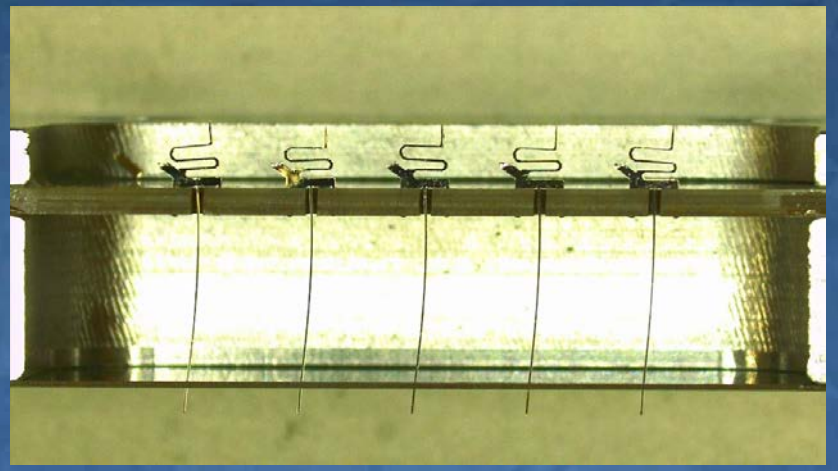


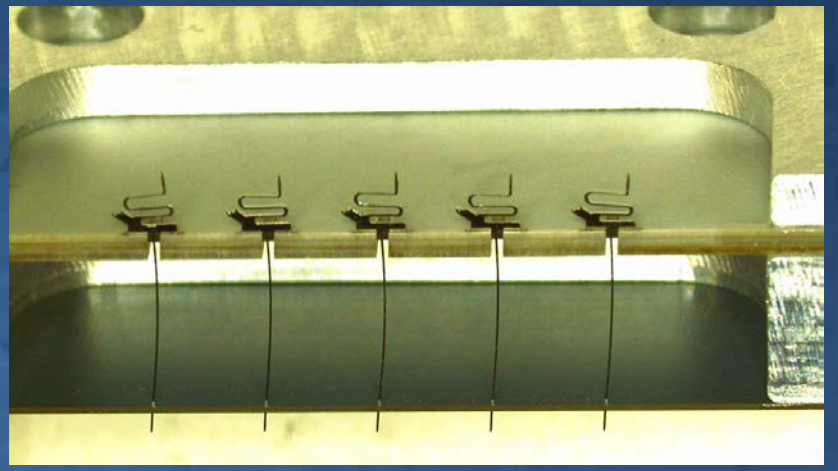


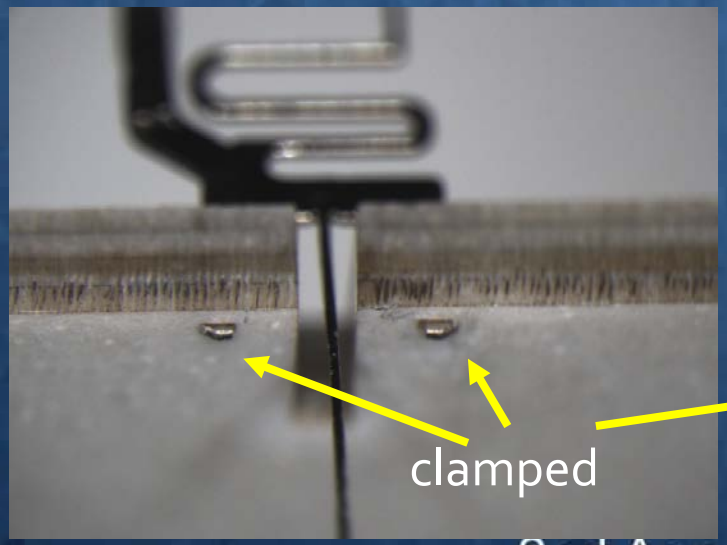


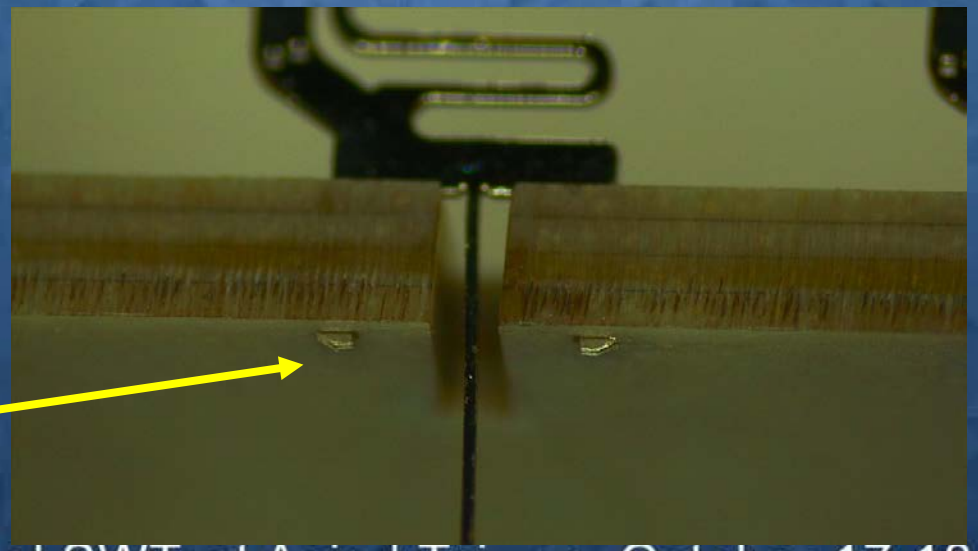
Tested in a variety of configurations









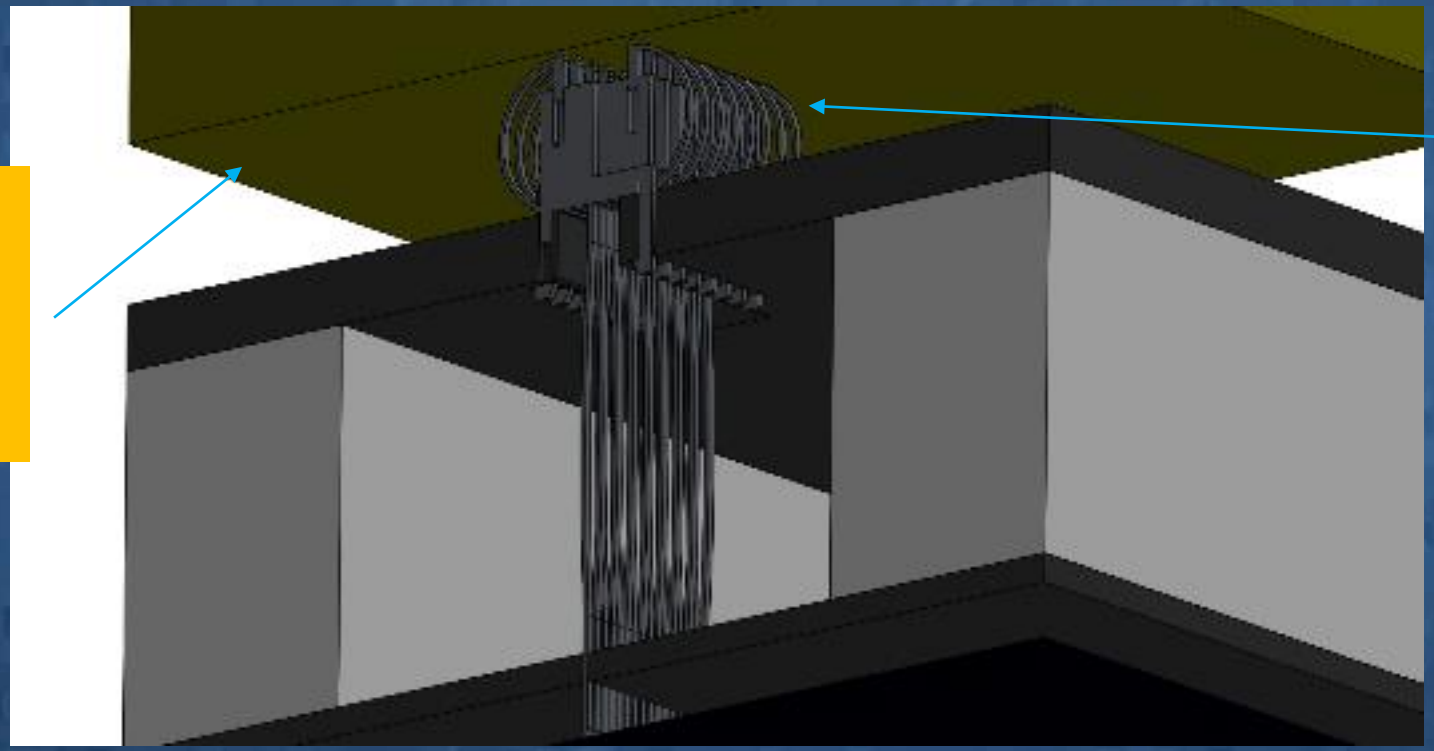


Applications:

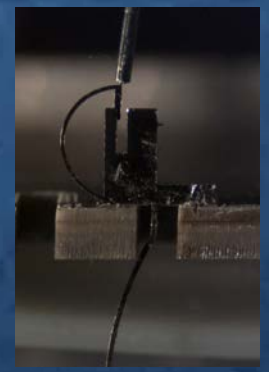
- FLASH is the single largest application ~$250-$300M
- Relatively little probehead innovation over the past decade
- Typical designs use a ceramic-laminate space transformer plus an interposer
- Probes can be re-used across products, but ceramics/MLOs generally cannot
- Target with STP is to reduce cost by 50%

FLASH Probecard Application

Smart design allows room for component mounting

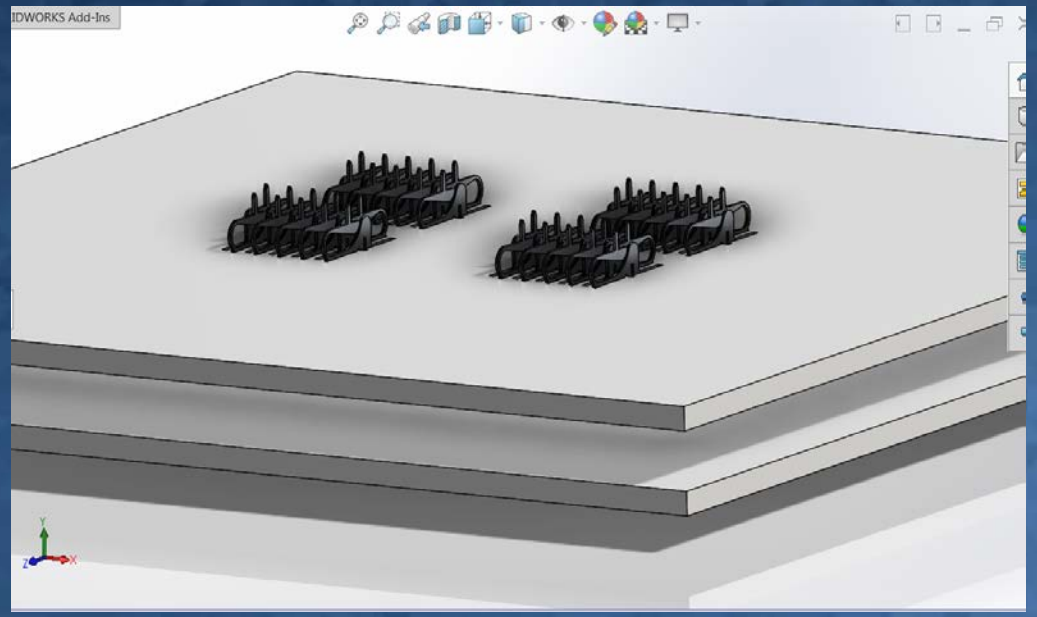


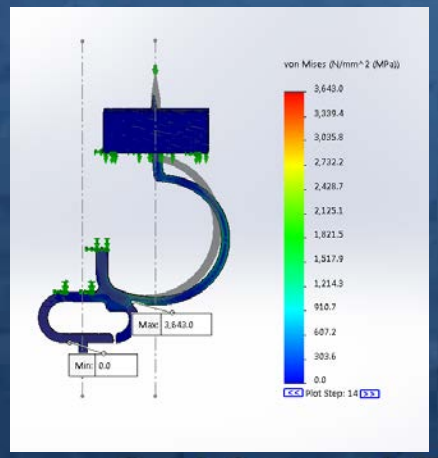
Distal side design MEMS probe allows for **independent** compliance to PCB

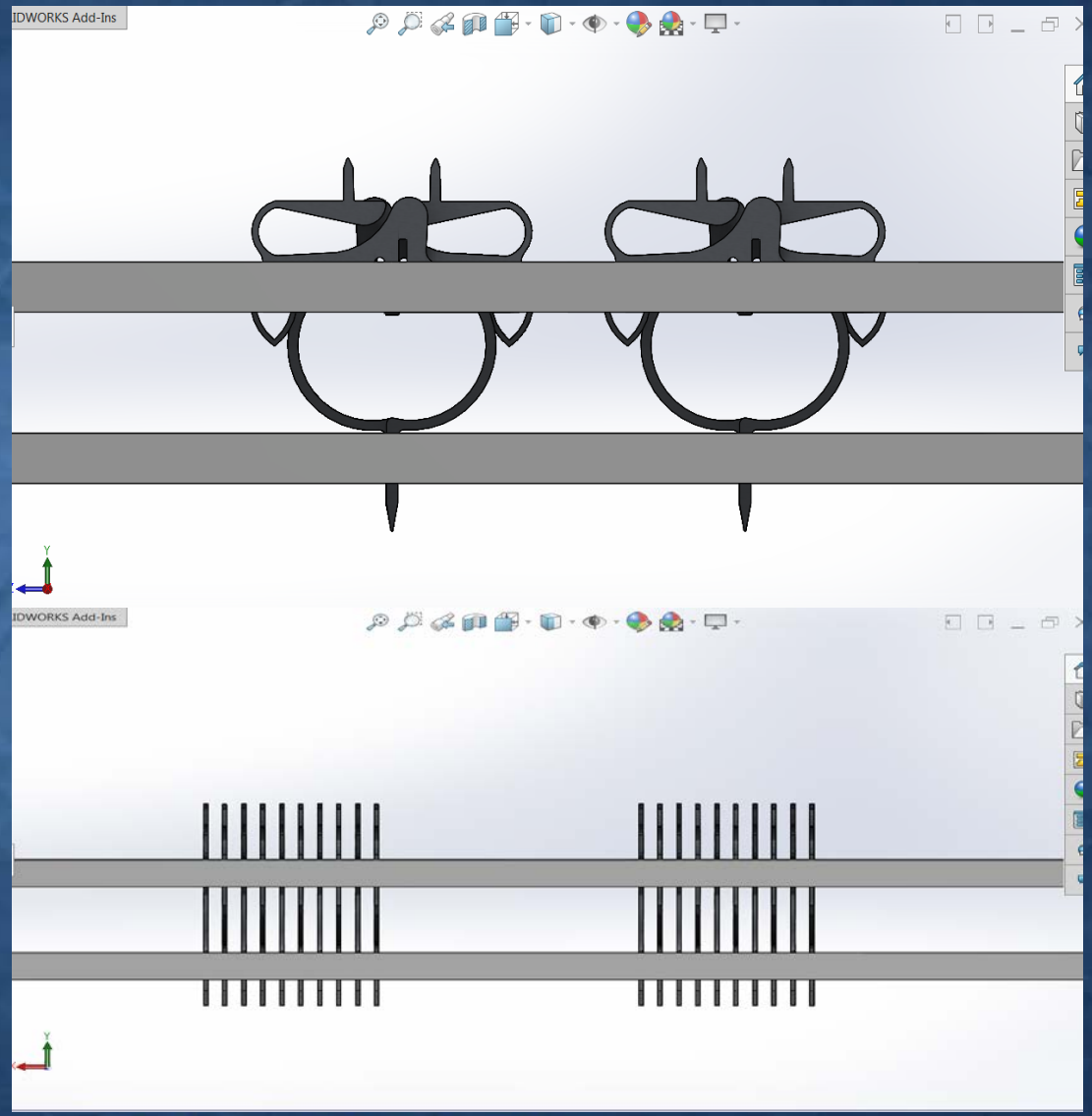


Probe at 100µm overtravel

Sensor Probecard Application







LCDD Probecard Application

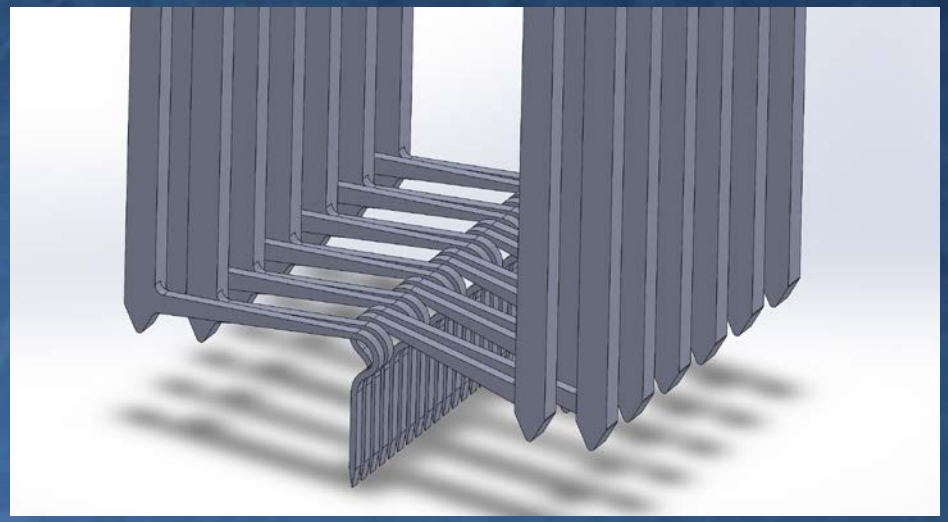
- Translarity shipped a 39um pitch MEMS product recently
- Current technology can probably be pushed to ~32um (15um probe size)
- Beyond that, multiple problems appear to be intractable:
  - CCC decreases precipitously
  - X-Y accuracy in drilled holes very difficult to achieve, especially as taper becomes larger than hole size
- And yet the LCDD market and LED markets require pitches of 18-30um, maybe less

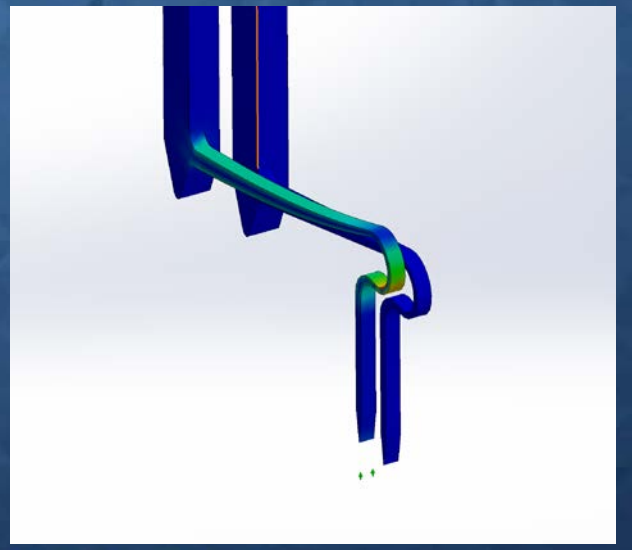
Extreme Pitch Applications

- Halving of 40um pitch could give 20um
- Most of the probe is still 40um
- Decouples CCC and compliance

But

- Assembly is complicated and delicate
- Rotational errors result in x-y offsets
- Testing multiple columns is difficult



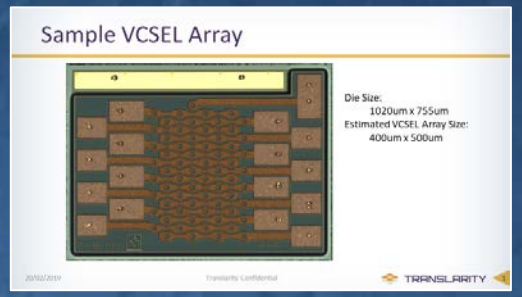


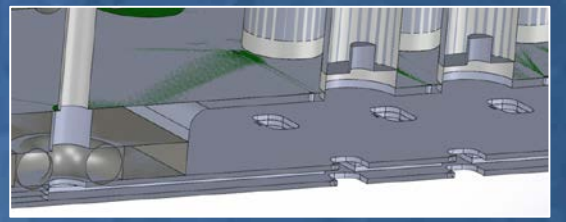
Optical Applications

- Attractive market for advanced optical probecards ~$200M
- CMOS imagers, LEDs, LCD products, VCSELs
- Today primarily served by cantilever and needle cards
  - High parallelism is difficult, pad damage, frequent repair
- High degree of complexity in instrumented probecards
  - We have added optical sensors to probecards, as well as light sources

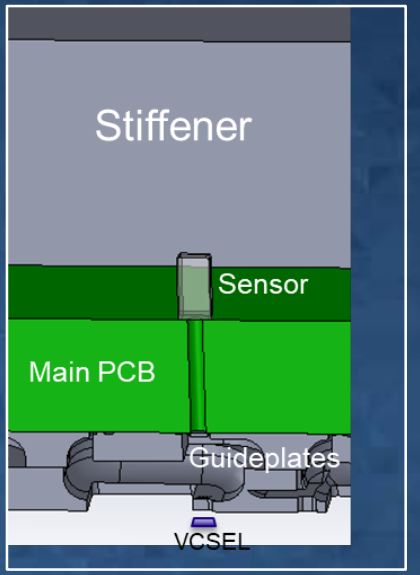
VCSEL Probecard Application

- Provides direct device performance **(optical, temp, electrical, etc)** during testing for wafer sort yield
- ST Probes allow light path from VCSEL to the measurement unit
- Optical measurement to VCSEL array output

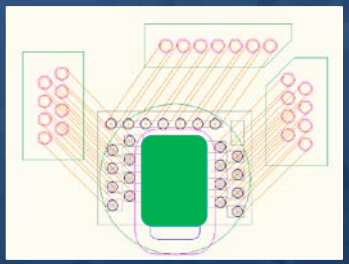




MEMS style IPC – X section

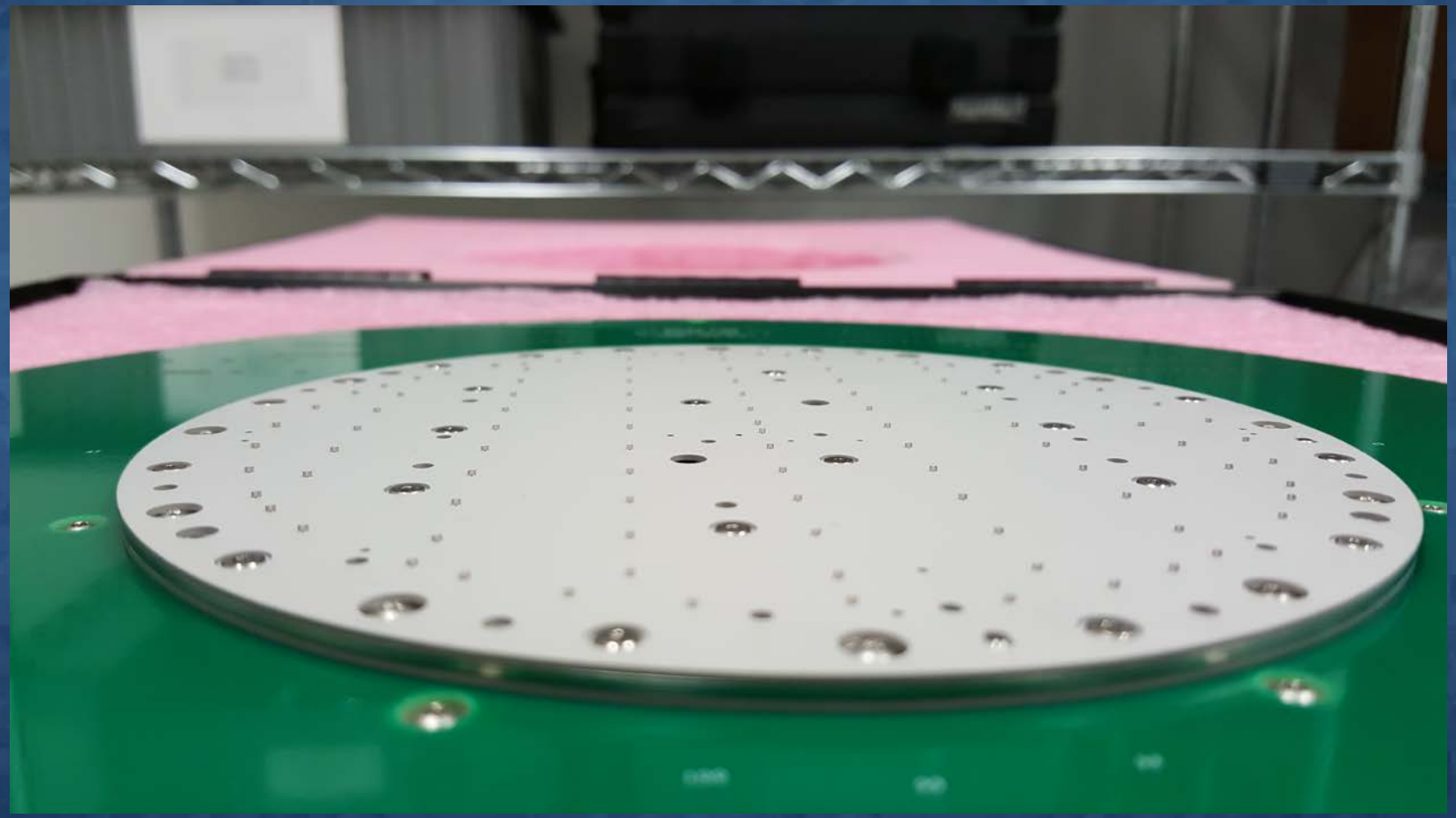


Cobra style IPC – X section

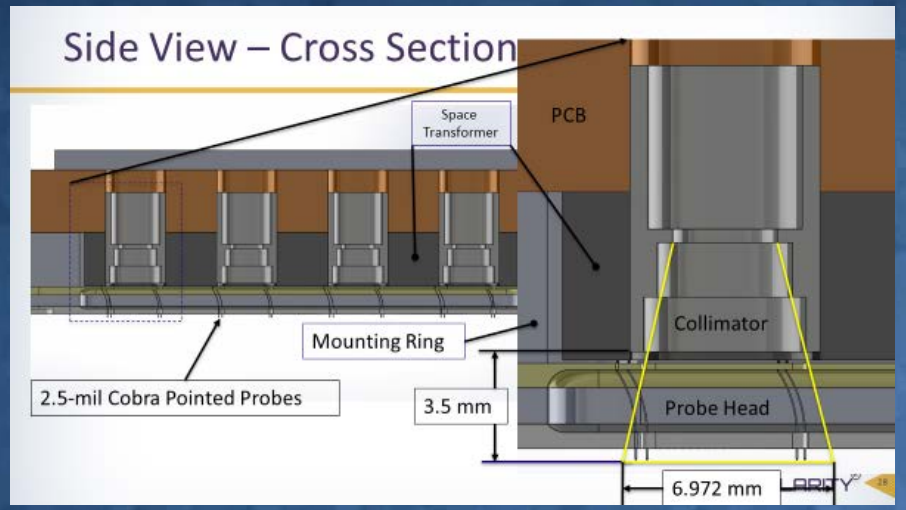


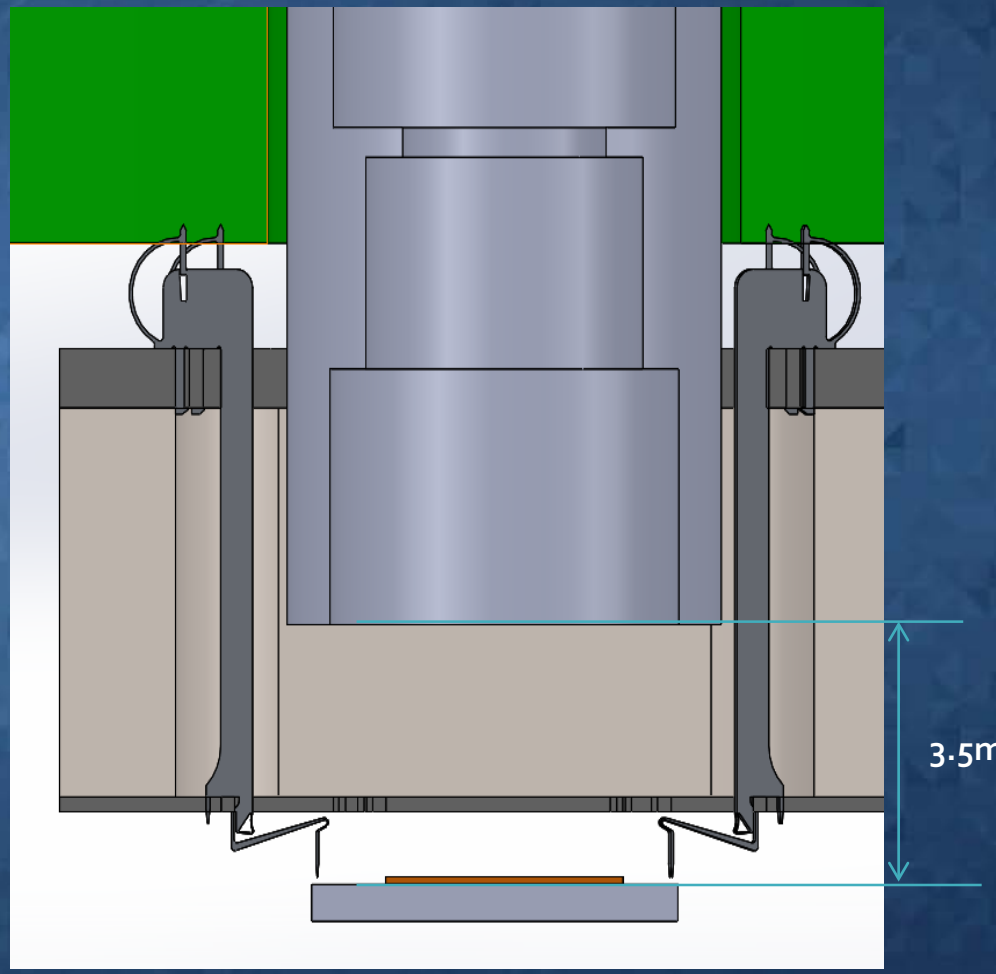
VCSEL active area on wafer near pads

VCSEL 100 site card



CMOS imaging/LED Applications





- Achieves 8.6mm probe depth without interposer.
- Achieves space transformation within probe design. No separate space transformer required.
- Probe is out of the optical path because of offset design.
- Single pin replaceable.

Challenges

- Cost
  - If the STP costs a lot more than vertical MEMS, it negates some of the benefits (target is to be within 20% of the equivalent probe cost)
  - If more complex GPs are needed, this again reduces benefits (target is to use only 2 GPs with only 1 high precision – pat. pending)
  - If assembly is more complex, this is also a problem (target is to be able to offer easy field repair and comparable assembly – pat. pending)
- Probes sees new lateral stresses
  - Unwanted lateral movement needs to be controlled
- Guide Plate design is more complex

Conclusions/Future Work

- XYZ Space transformation generally doubles the cost of a probe head
- Space transforming probes can eliminate this cost, potentially enabling a large cost decrease in several markets
- Translarity has developed probes that accomplish this goal and is now engaging with customers on specific implementations
- Significant work left on long-term reliability qualification, large-area precision ceramics and pitch-halving architectures

SWTEST ASIA 2019

Temperature Accuracy at High Wattage Wafer Test – a Novel Method to Control Device Temperature

Klemens Reitinger
CEO/CTO

Hsinchu, Taiwan, October 17-18, 2019

Agenda

- Why talk about Power in Wafer Test?
- Market Demand
- Technical Background
- Effects to Wafer Test
- Challenges and Experimental Data
- Possible Solutions
- Summary and Outlook
- Q&A

Why talk about Power in Wafer Test?

- Electrical Power induced in Microchip during test acts like a heater
- This heat creates a temperature rise in the DUT which is undesired
- Test results will be unreliable with no control over test temperature
- Worst case the test cannot be done at wafer level

Market Demand

- **Demand of dealing with power is raising strongly in the past years because of:**
  - Massive parallel testing of low power devices (DRAM,….)
  - Parallel Testing of „mid power“ devices (GPU,…)
  - Testing at low temperatures (-40°C and lower) is more often required
  - New applications are coming up (WLBI at Silicon Photonics,…)

Technical Background: Path of the Heat

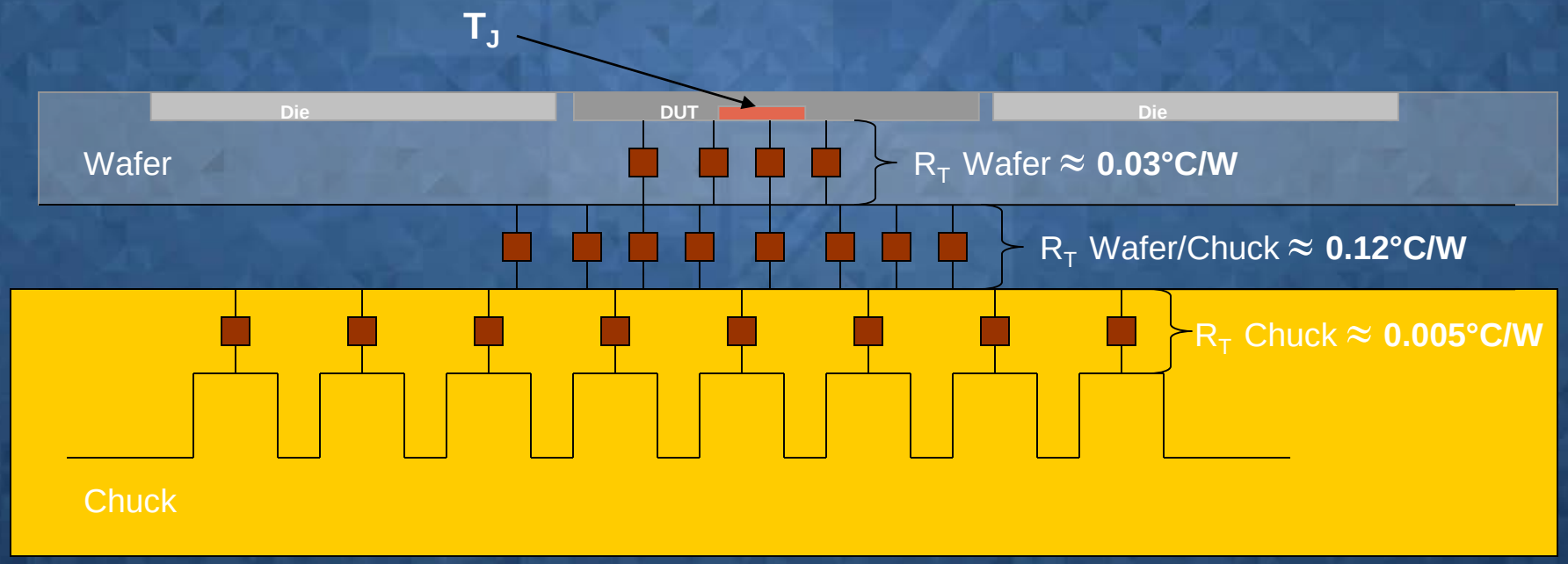
Wafer-to-Chuck Thermal Resistance is Largest Contributor

When 50 Watts is applied to DUT

R_T Wafer = 1.5°C (19.5% of Total R_T)

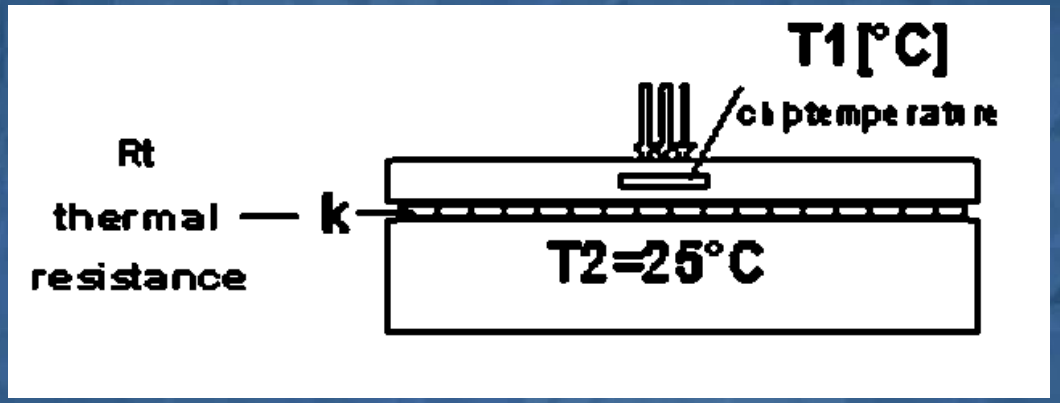
R_T Wafer/Chuck = 6.0°C (**77.9% of Total R_T**)

R_T Chuck = 0.2°C (2.6% of Total R_T)



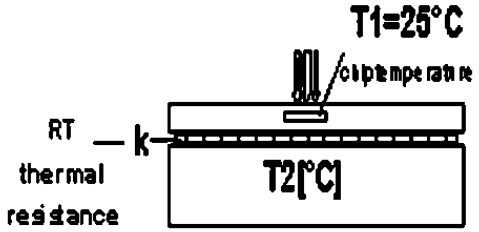
Technical Background: k-Value

(T1-T2) / Power = k (°C/W)



Chip Temperature (T1) =
Chuck Temperature (T2) + (Chip Power X Thermal Resistance k)

Wafer Test: Practical Influence of k-Value



Thermal resistance factor k*	Chip temperature constant T1	at P100W Chucktemp T2	at P 200W Chucktemp T2
0.1	+25°C	+15°C	+5°C
0.3	+25°C	-5°C	-35°C
0.5	+25°C	-25°C	-75°C

*Chip size = constant

Wafer Test: Typical CPU / GPU Test

- Mid-size chip
- Single or multiple test, not too many in parallel
- Very high wattage per chip
- Importance of sensor independence
- Multiple test temperatures
- Protection against thermal runaway needed

Wafer Test:Typical DRAM / Memory test

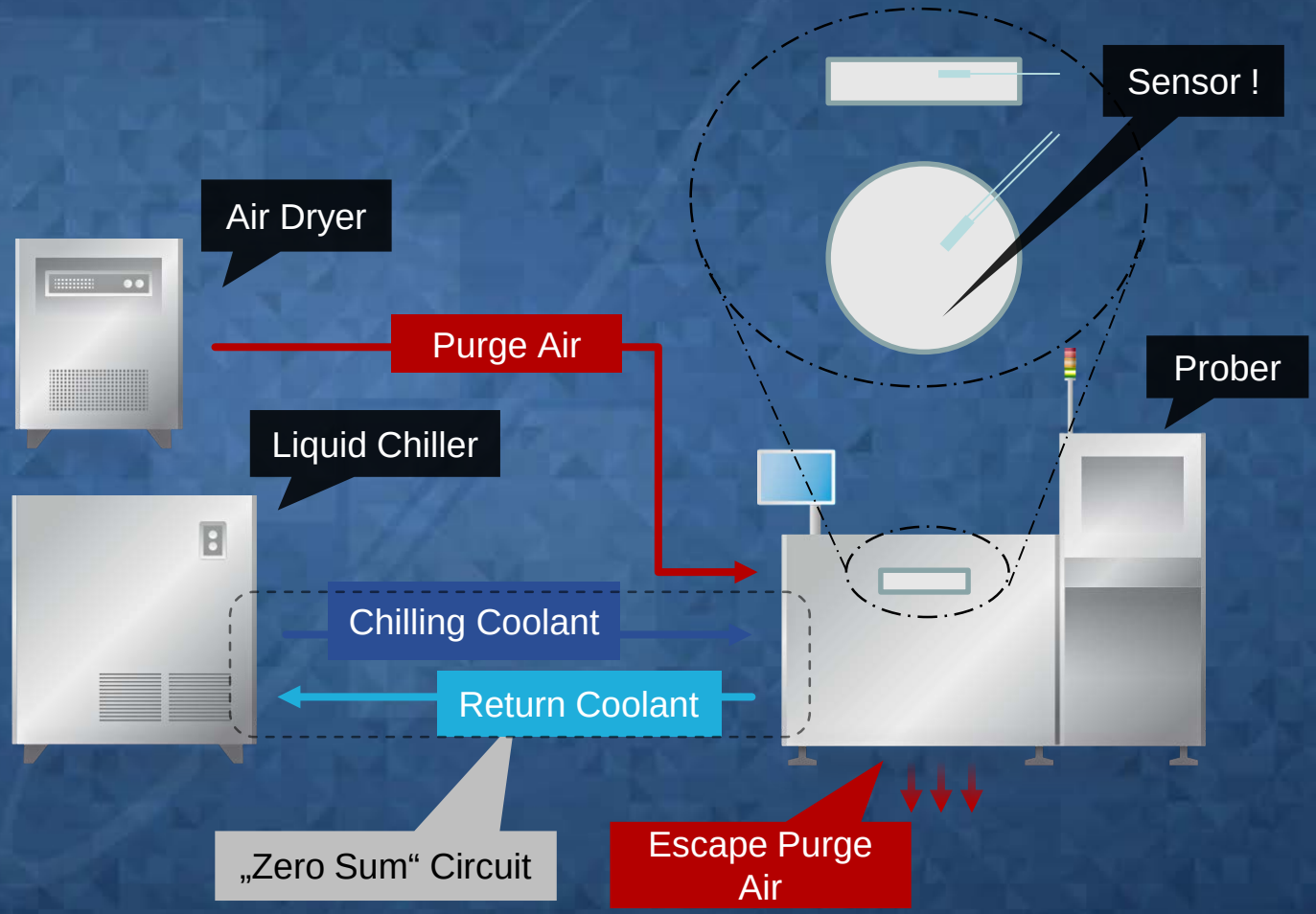
- Mid-sized chips
- Massive parallel testing, one touch down
- Low wattage per chip
- Sensor dependence not so important
- Good uniformity needed

Typical WLBI test

- Any size chips
- Massive parallel testing, one touch down
- High wattage per chip
- Sector temperature monitoring important
- Good uniformity needed, even in case of operating and not operating devices
- Multiple temperatures needed, special attention to higher temperatures

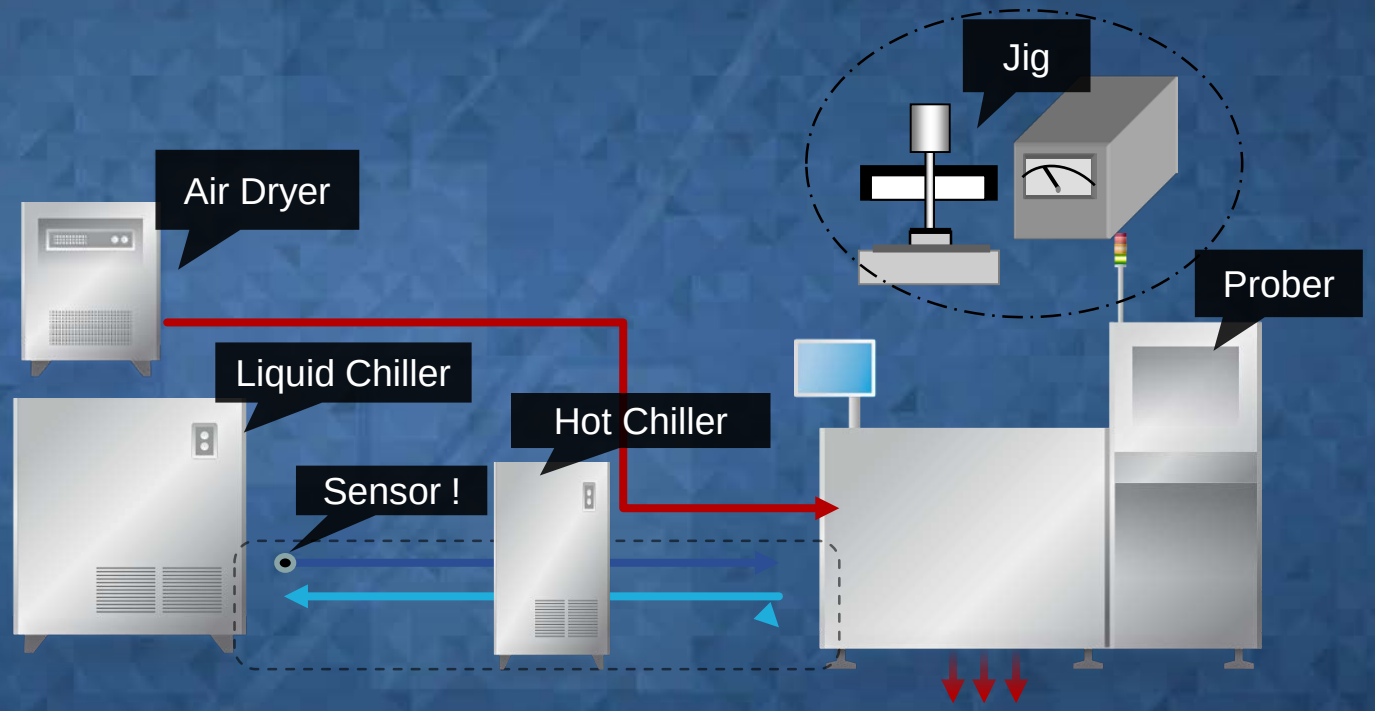
How to Deal with Power in Wafer Test

- **Standard Cold Wafer Test System**
- **Will react differently depending on position of power input in relation to sensor**



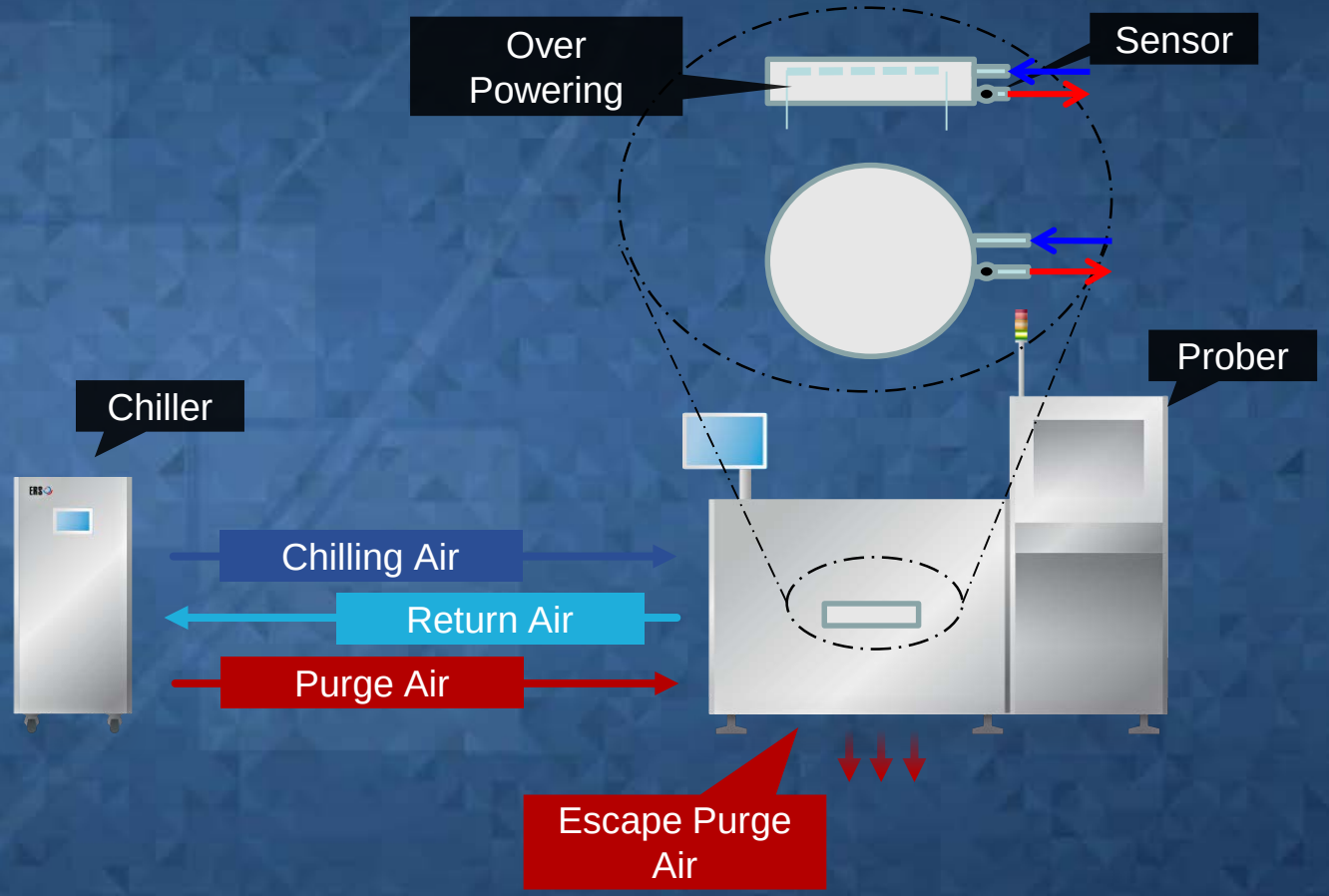
How to Deal with Power in Wafer Test

- Temperaure controlled by <u>coolant only</u>
- Independent of power input position
- Unflexible regarding power fluctuation



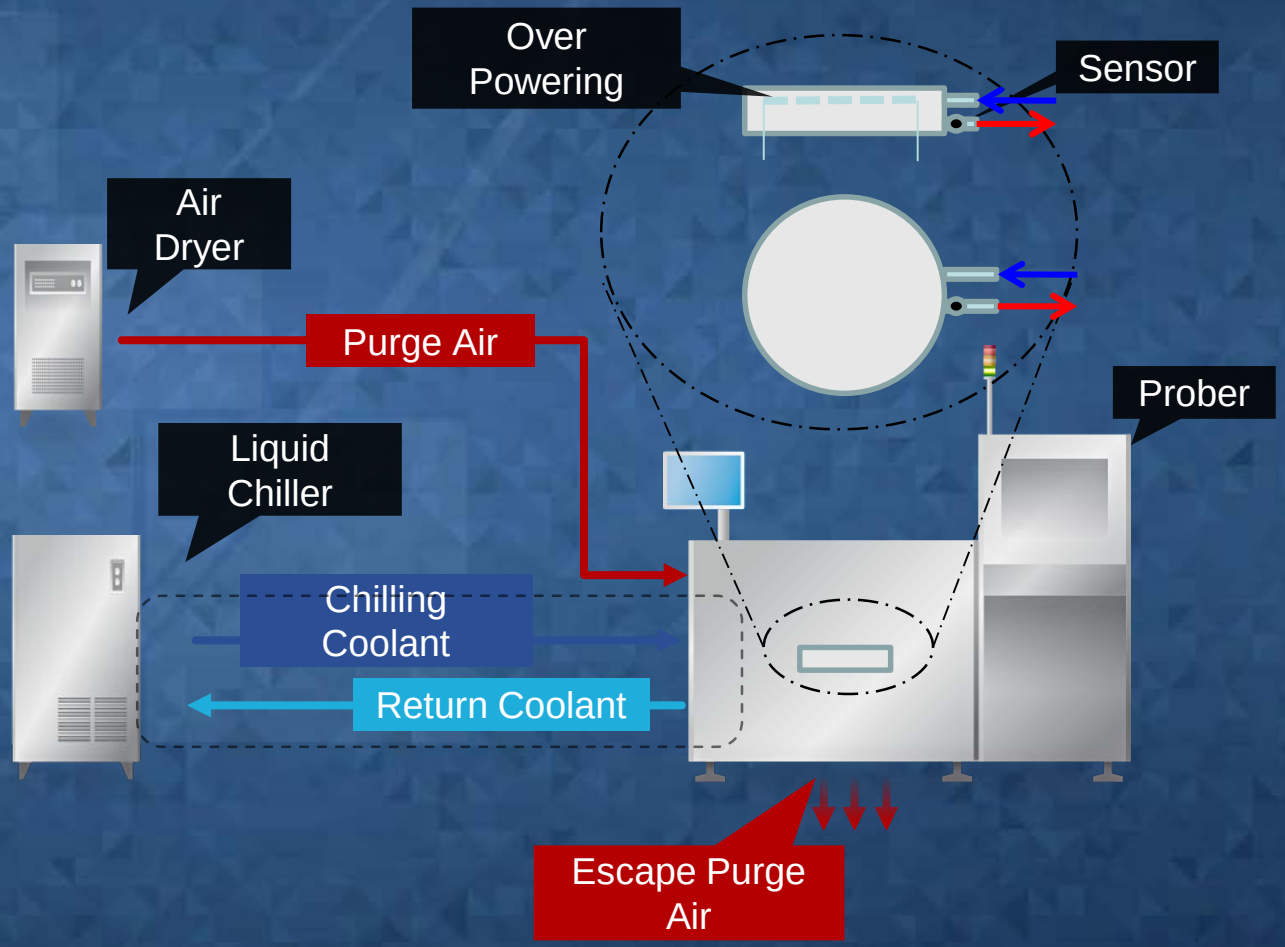
How to Deal with Power in Wafer Test Our Solution Air

- Temperaure controlled by coolant exit of the chuck
- Temperature controlled by heater overpowering
- Independent of power input position
- Flexible regarding power fluctuation



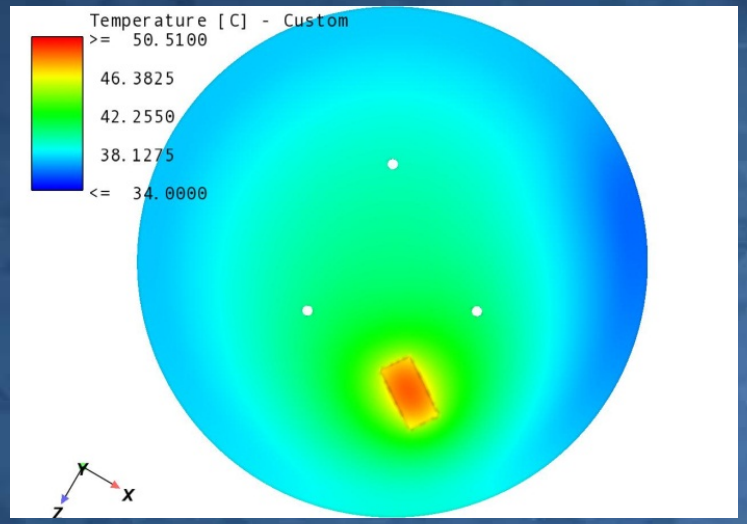
How to Deal with Power in Wafer Test Our Solution Liquid

- Temperaure controlled by coolant exit of the chuck
- Temperature controlled by heater overpowering
- Independent of power input position
- Unflexible regarding power fluctuation

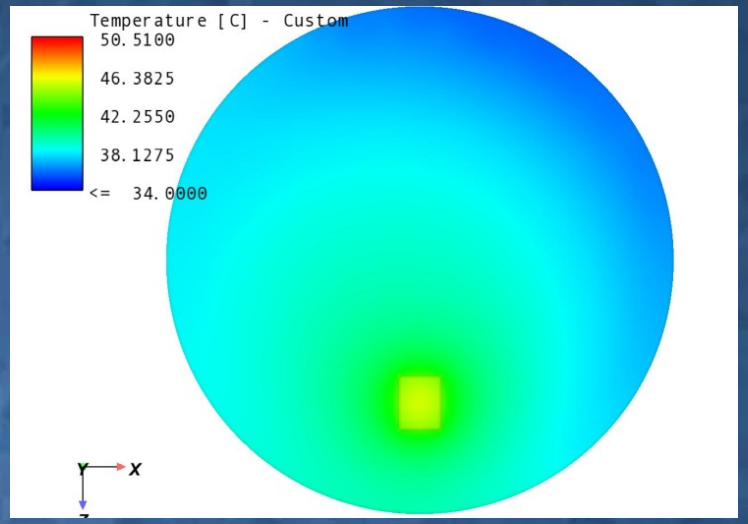


Thermal Simulation of Air Cooled Chuck

100W , 800mm^2 , 300l/min Air in @+20°C



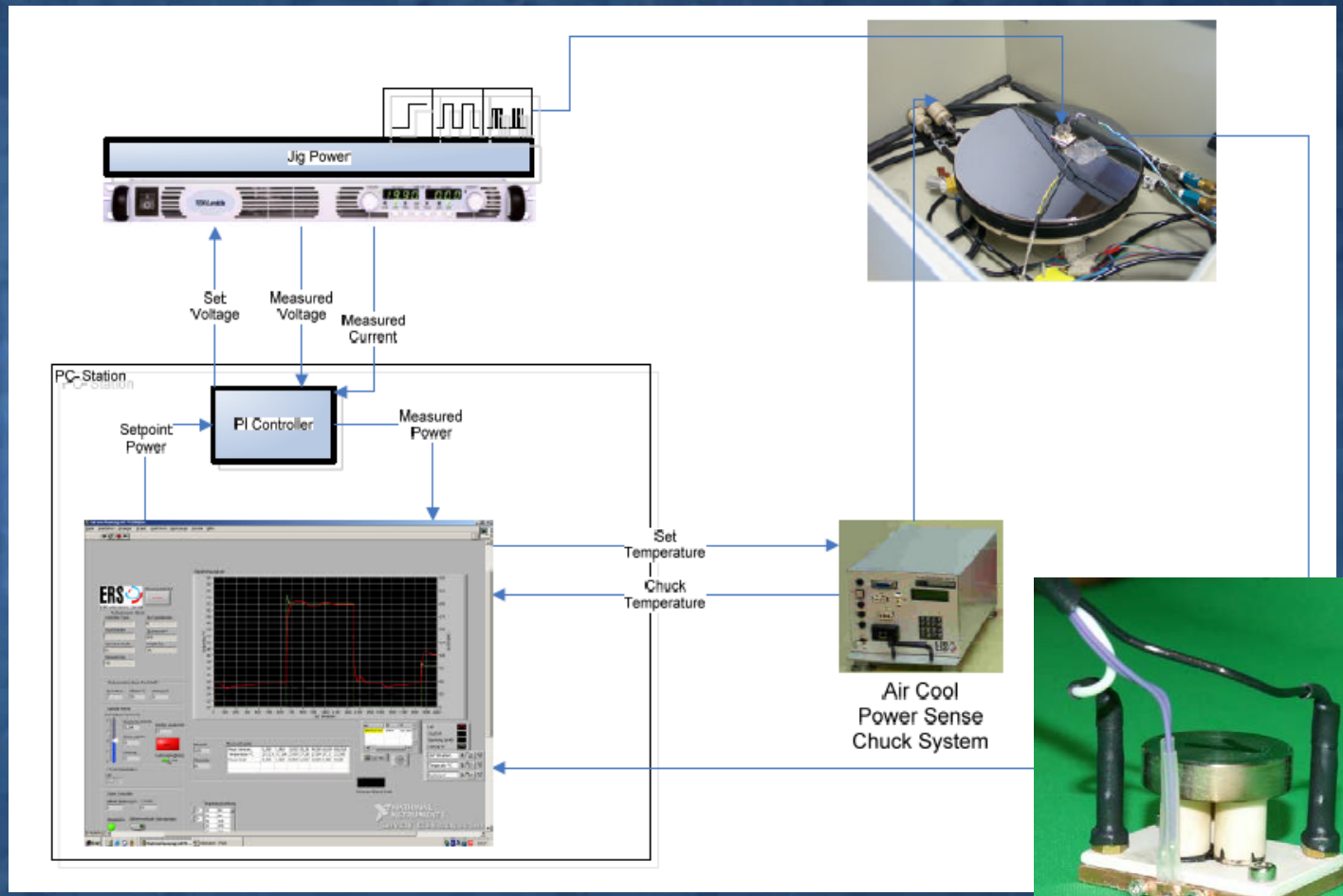
- **“Non High Power Chuck”**
  - Uneven Temperature Uniformity when Power is applied locally
  - Bad transmission of Heat
  - High Chip Temperature



- **“High Power Chuck”**
  - Good Temperature Uniformity when Power is applied locally
  - Good transmission of Heat
  - Low Chip Temperature

Test Set Up in Lab

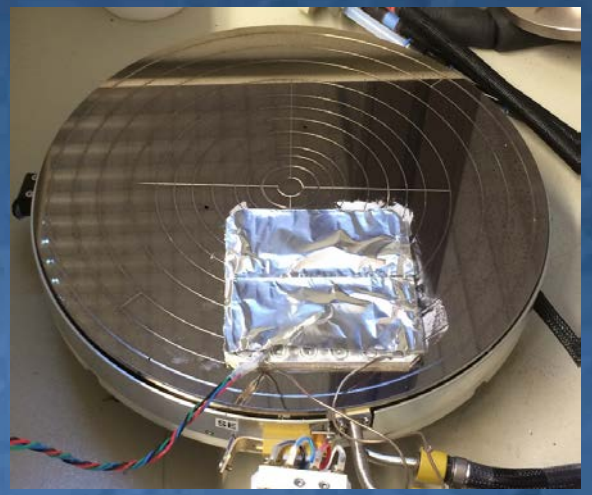
- Chuck with heat load and 6 sensors
- One sensor in the heater, one close to heater
- Chuck connected to liquid chiller and measurements are taken with and without load
- Heat up of the load and uniformity of the whole chuck was recorded



One sensor very close to load

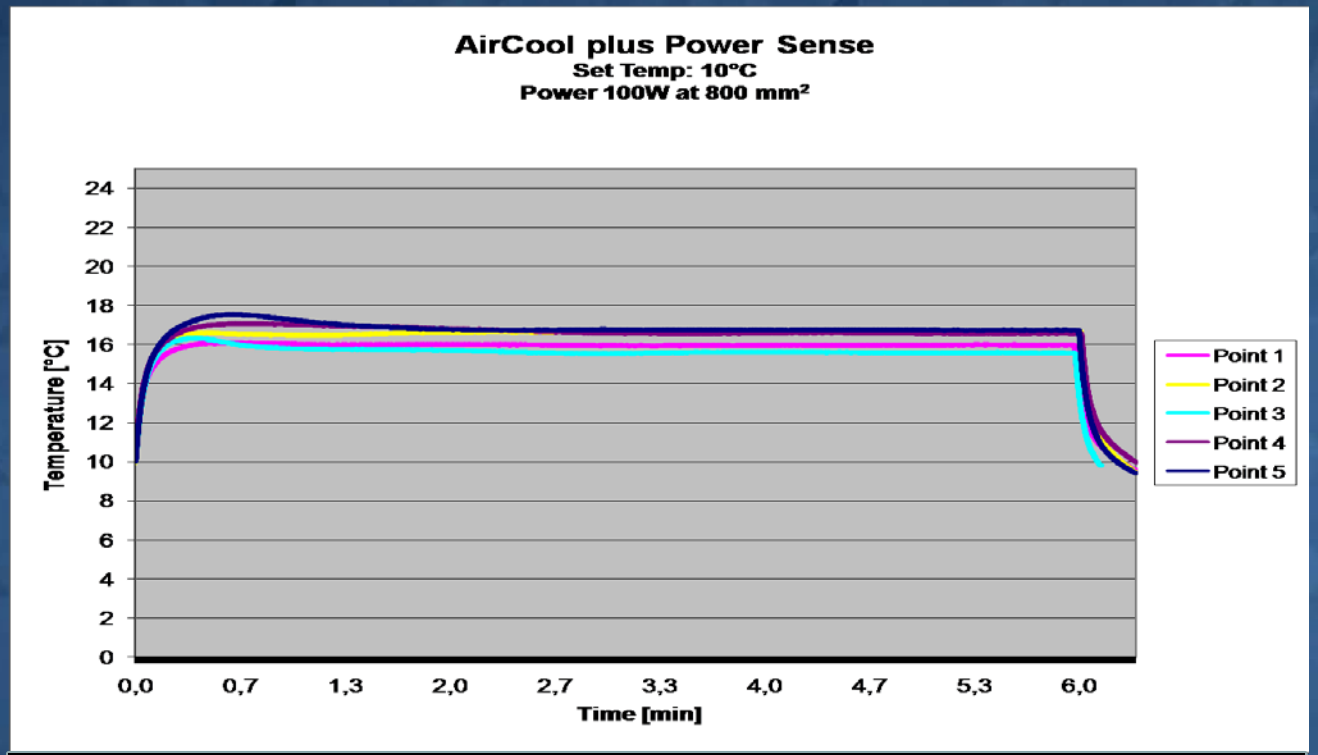
Set Up Different Load JIGs

- 100 x 100 mm
- 20 x 40 mm
- 10x10mm
- Full Wafer 200mm and 300mm

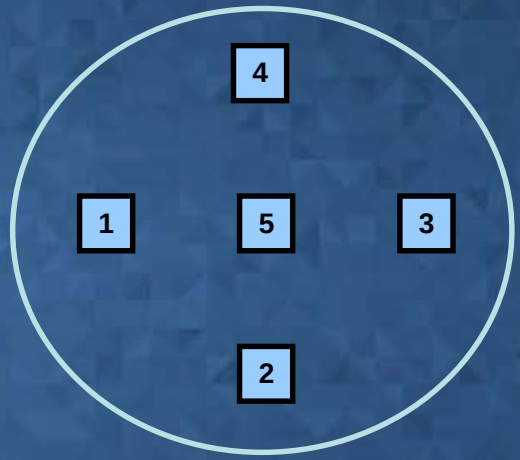


One sensor very close to load

Results AirCool Chuck 100W @ 800mm²



	Point 1	Point 2	Point 3	Point 4	Point 5
Maximum Temperature [°C]	16,13	16,70	16,35	17,08	17,56



Measurement Points on 300mm Chuck

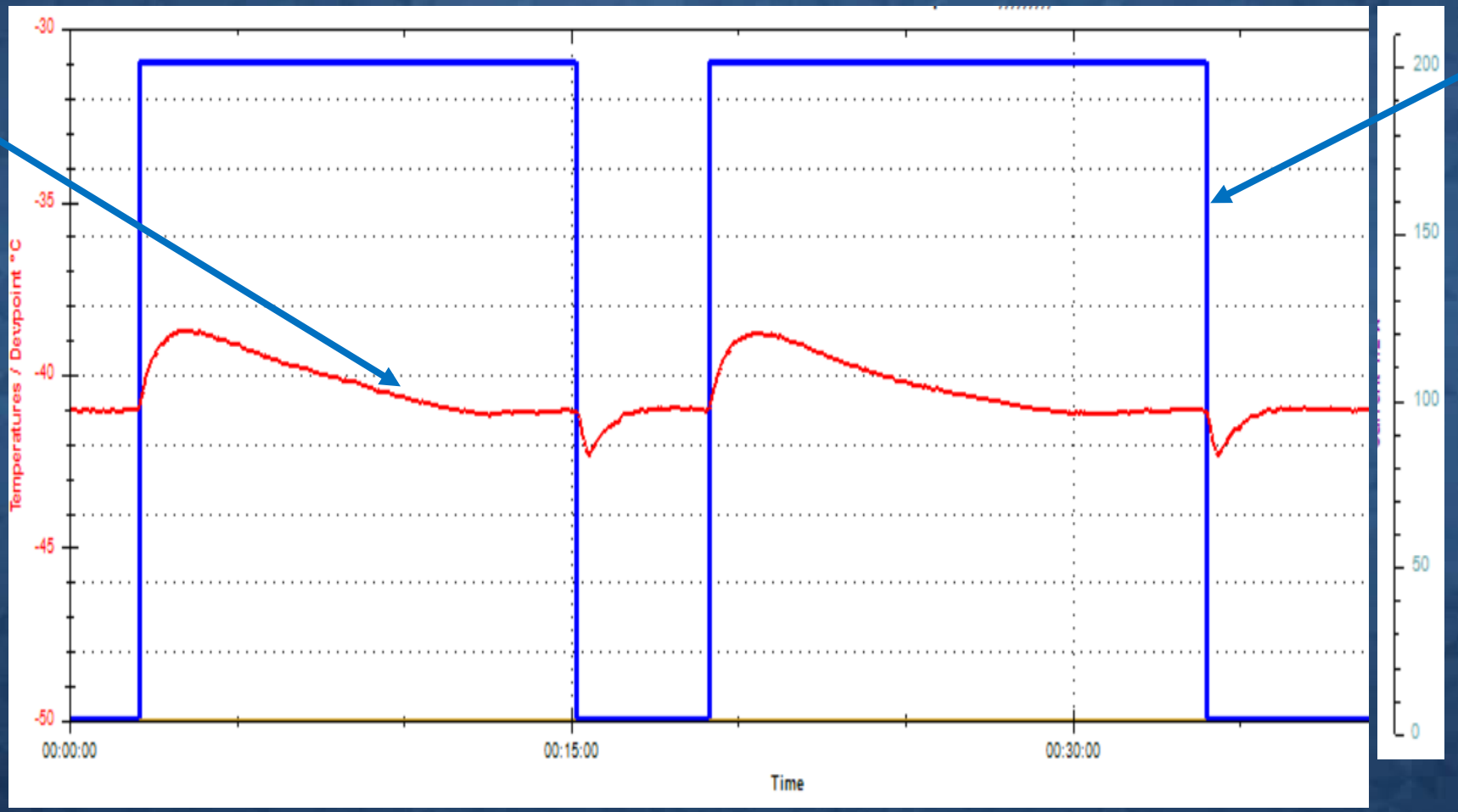
- k-value = 7°C / 100W = 0,07°C/W
- Jig Temperature Range within + 1,5°C / - 1°C

Results AirCool Chuck 200W @ 100cm²

Set Temperature -40°C

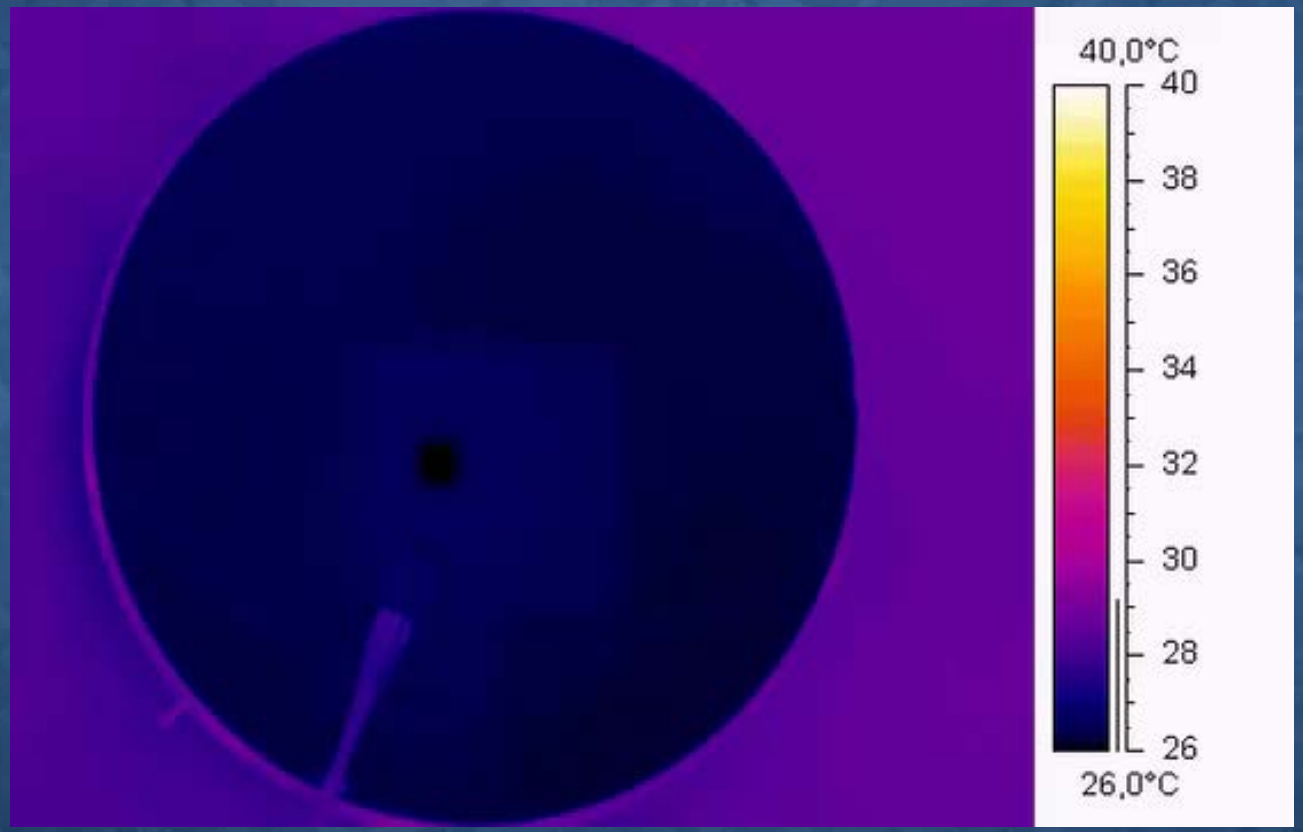
Chucktemp

Power



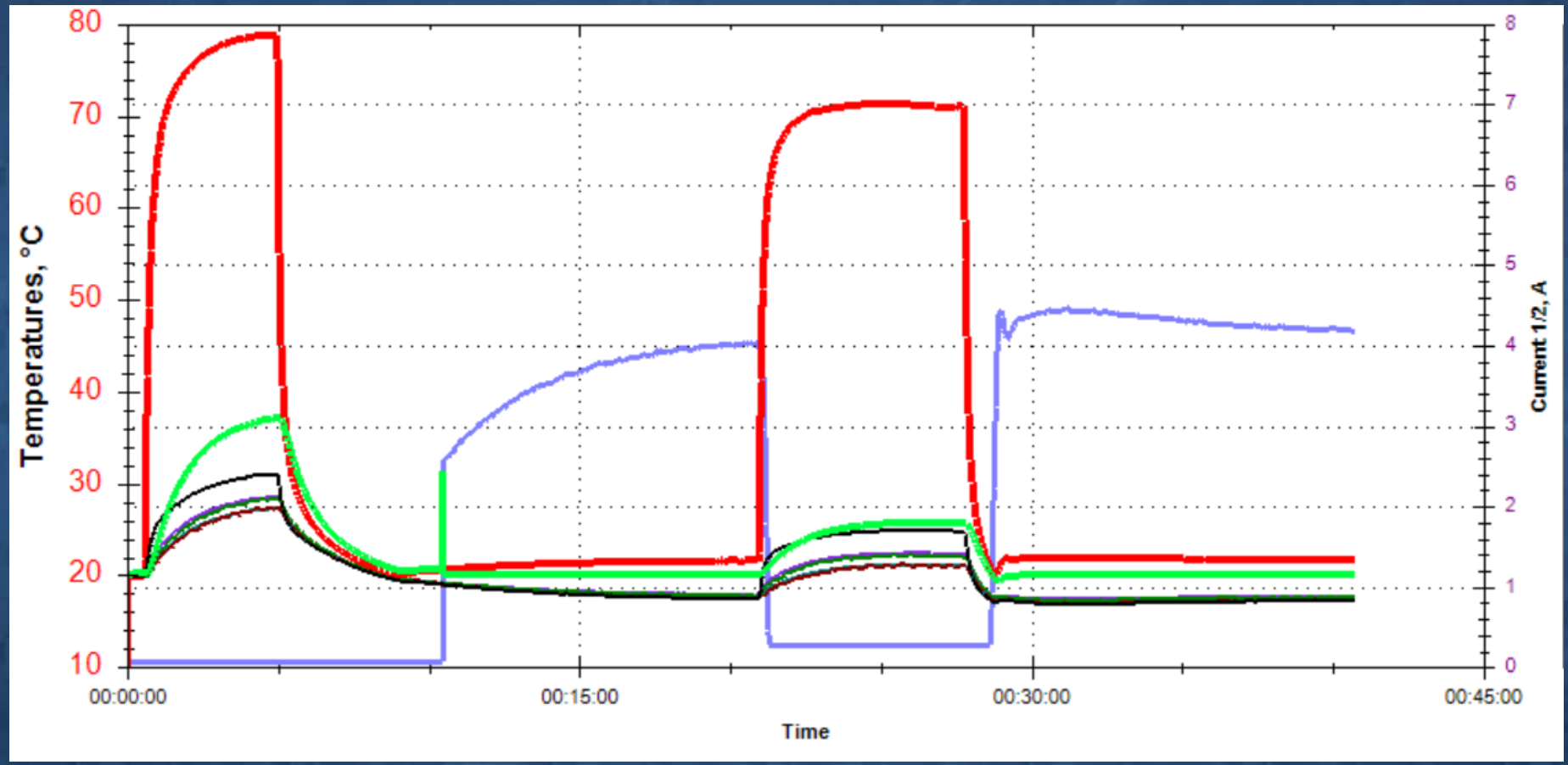
Thermal Camera Film

- **Device Size: 15x15mm, Power 200W, Temperature +20°C, Liquid Cooled Chuck**



Comparision Offset - Overpowering

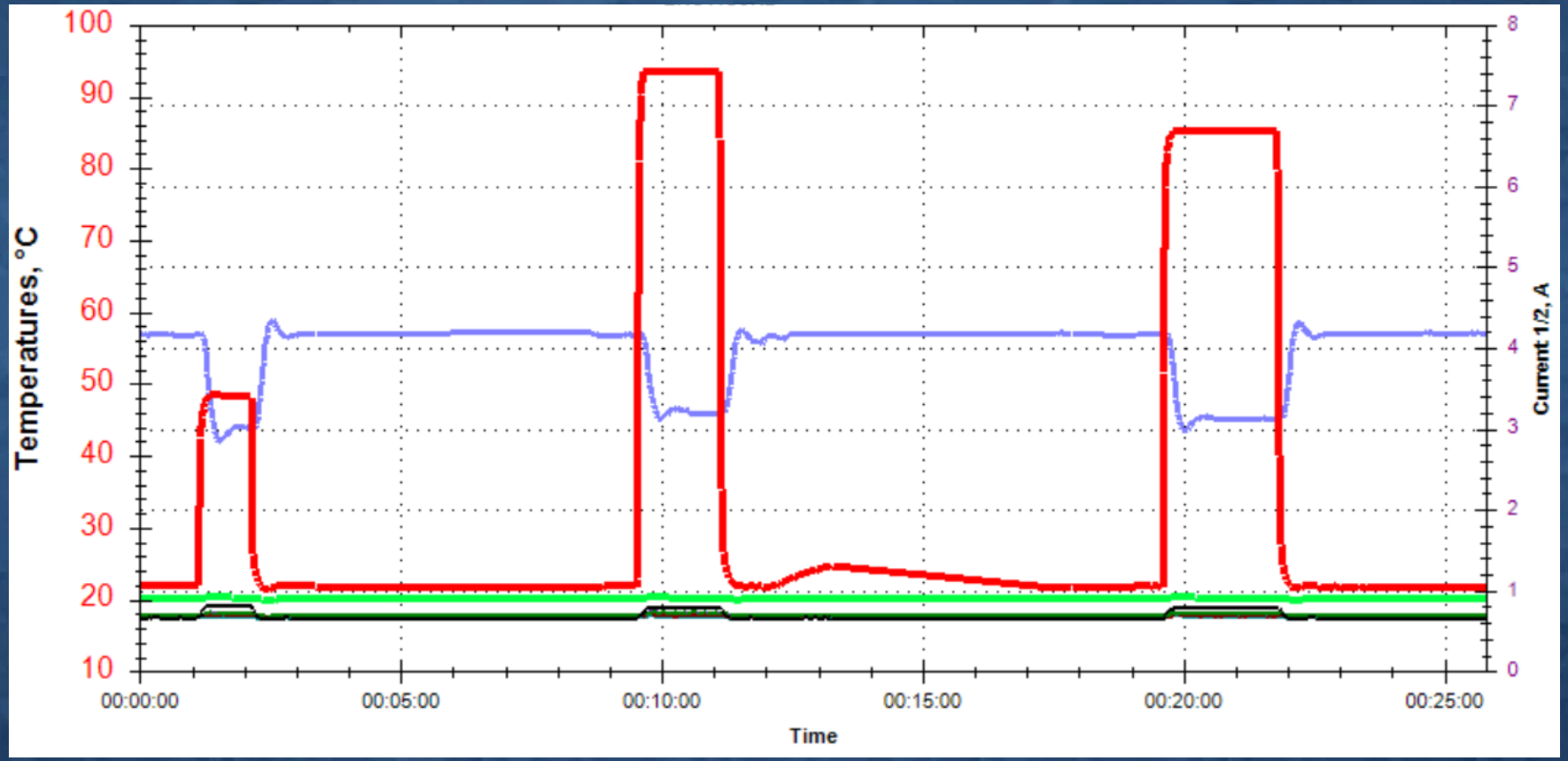
- **Device Size: 20x40mm, Power 500W, Temperature +20°C, Liquid Cooled Chuck**



K-value = Delta T / Power = 50K / 500 = 0,1 k/W -> Chip Temp = +70°C at +20°C Chuck

Comparision Different Materials

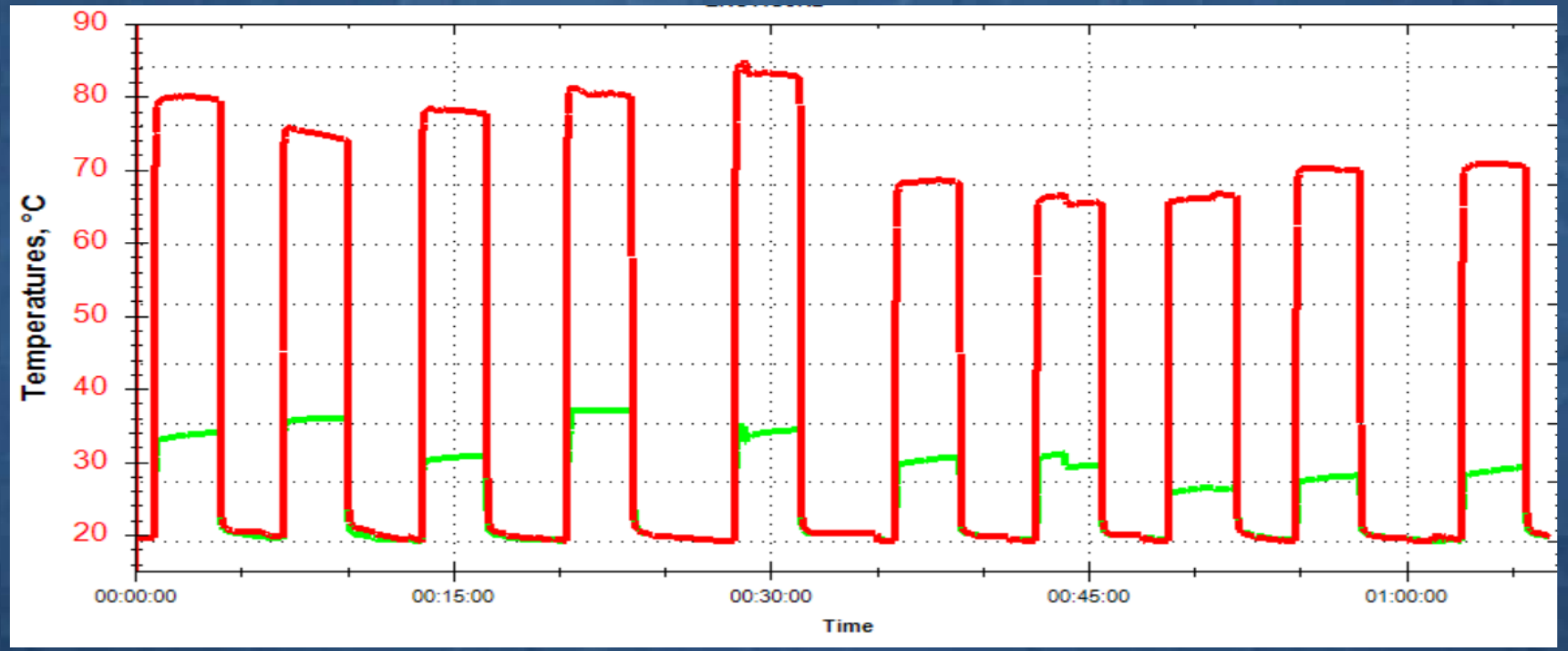
- Device Size: 12x12mm, Power 120W, Temperature +20°C, Liquid Cooled Chuck
- Directly on Chuck
- GaAn
- Si



k= 0,23 k= 0,625 k= 0,5

Comparision Different Chip Surfaces

- **Device Size: 15x15mm, Power 200W, Temperature +20°C, Liquid Cooled Chuck**



Dry

Liquid

Summary

- **Our method shows 3 advantageous features:**
  - No dependency on sensor position
  - Heater controlled temperature can react fast on power input
  - Concept can be used for air and liquid systems

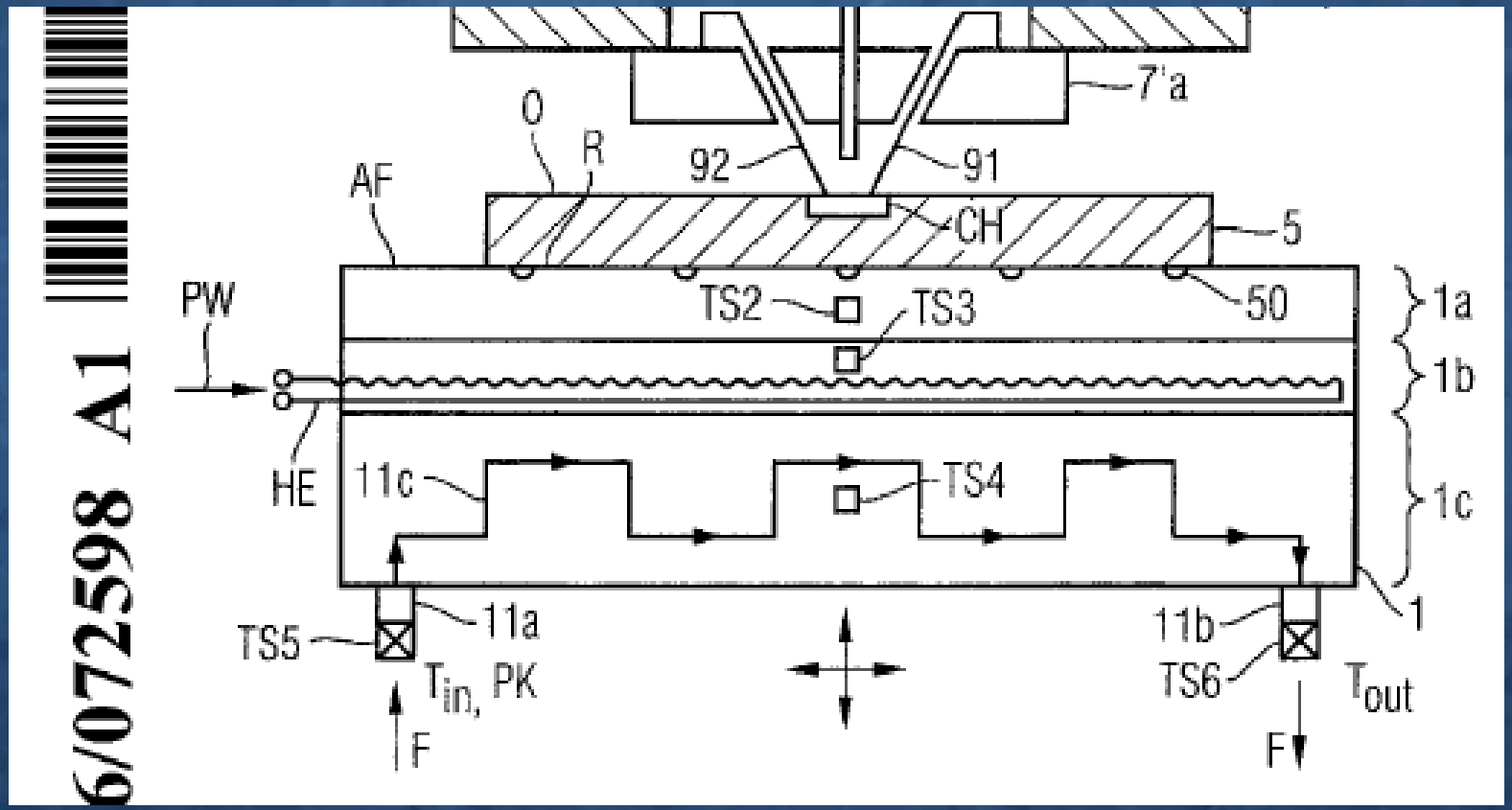
Summary

- Special chuck set-up is needed for power test in wafer test
- Sensor dependence must be avoided
- Air-cooled systems capable for larger areas of power induction and down to about 0°C
- Lower temperatures and higher wattage require liquid-cooled systems
- Thermal interface between wafer backside and chuck top surface is key
- Overpowering can help to reduce temperature offset and keep k-value constant over different wattage and test times

Outlook

- **Actual chip temperature monitoring becomes more important:**
  - Multiple Sensors in Chuck
  - Real Time monitoring with IR sensor in probe card
- **Parallel testing is increasing also in non-memory sector**
- **New products (e.g. silicon photonics) will require power dissipation at wafer test**
- **Demand for more accurate prediction of temperature for DUT is rising**

Monitoring Chip Temperature in Real Time



Credits

- Sophia Oldeide, Ibrahim Khwaja, Laurent Giai-Miniet (ERS)
- Patty Lei, Calvin Hsu (CLIC)
- Hector Lin (MPI)

Thank You!
Q&A

SWTEST ASIA 2019

Overview of Specialized Testing for MEMS Sensors: Wafer Probe and Final Test

RIKA DENSHI

Michael Ricci

Principal Engineer

Solutions Technology Center - West

Hsinchu, Taiwan, October 17-18, 2019

MEMS Device Testing

- Who we are
- MEMS device/sensors overview
- Description of popular and growing applications
- MEMS market = Show me the $
- Why is testing MEMS devices different?
- MEMS gyro test application
- On going work

Rika Denshi Group Introduction

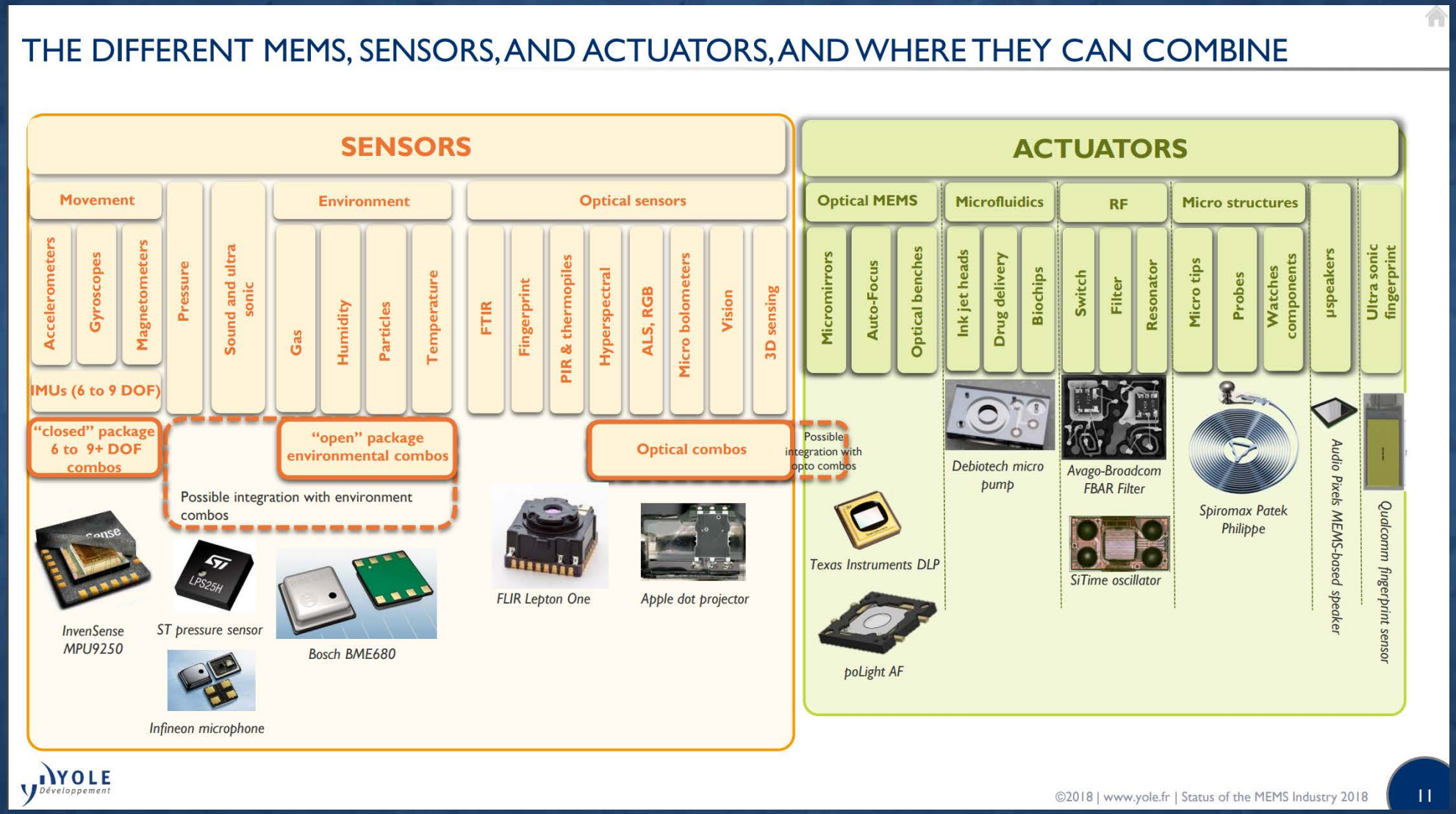
- 57 years in business as a spring probe manufacturer
- Third generation family ownership
- HQ in Tokyo with factories in USA, Thailand and Japan
- Focused on RF/mmWave, High Temperature, Tight Pitch and Non-magnetic spring probes used for packaged test sockets and wafer probe heads
- RF testing lab, thermal testing lab, metallurgical testing lab, plating testing lab, metrology testing lab.


RIKA DENSHI AMERICA INC.
Fujimi Plant
RIKA DENSHI CO., LTD.
West Sales Office /
Solution Technology Center (STC)
SHANGHAI RIKA DENSHI TRADING CO., LTD.
Osaka Sales Office
TAIWAN RIKA DENSHI CO., LTD.
Kyushu Sales Office / Kumamoto Plant
RIKA ELECTRONICS (THAILAND) CO., LTD.
RIKA DENSHI MALAYSIA SDN. BHD.
RIKA DENSHI SINGAPORE PTE. LTD.
RIKA ELECTRONICS INTERNATIONAL
ASIA PACIFIC PTE. LTD.

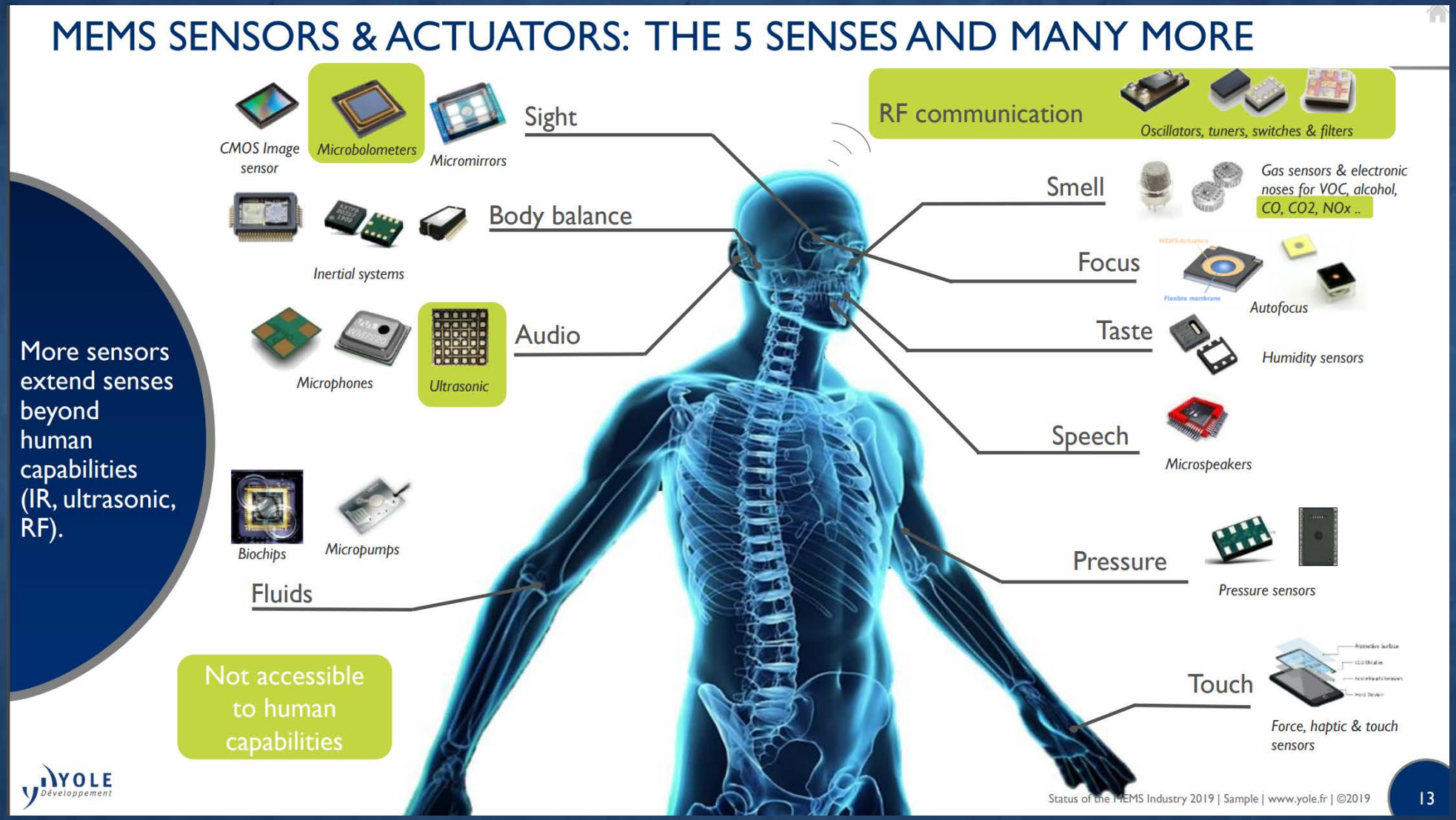
MEMS Device Overview

- Micro Electromechanical Systems have now proliferated into nearly all commercial markets via standard semiconductor package integration.
- Initially developed for military, aerospace and aviation applications, MEMS sensors for automotive applications are well understood; pressure, gas, gyro, inertia, G force, acceleration, microphones, HALL effect, magnetometers, photonics, piezo electrics…
- MEMS 2.0 or Sensor Fusion = multiple MEMS die combined into one semiconductor package and maturing firmware and software solutions to enable sensor fusion ecosystems.
- IoT, Industry 4.0, Smart City, Wearables, Autonomous Vehicles as well as other applications are driving growth in this space resulting in expanded MEMS wafer and package testing solutions.

Key MEMS Device Overview



Automotive MEMS Device Overview



MEMS Sensor Applications Overview

DEFINITIONS: MEMS APPLICATIONS TRACKED BY YOLE (1/3)

IJH		
Consumer and office	**Large/wide Format Printers - for graphics and technical**	**Industrial & printing (digital presse, label, ceramics, textile..)**
Thermal disposable heads Thermal permanent head Piezoelectric permanent head	Thermal permanent printhead Piezoelectric permanent head	Thermal permanent printhead Piezoelectric permanent head

Si Microphones			
Consumer	**Medical**	**Automotive**	**Others**
Cellphone Tablets Laptops Wearable Others (Home Automation, PMP, Laptop, handheld GPS, PC peripherals, toys…)	Medical (Hearing Aids)	Automotive	Indus, defense, high end

Pressure sensors				
Pressure sensors for automotive	**Pressure sensors for industrial**	**Pressure sensors for consumer**	**Pressure sensors for medical**	**Pressure sensors for aeronautics**
MAP Power Train BAP Power Train Particle filter (DPF, GPF) Power Train Fuel tank evaporation (EVAP) Power Train Exhaust gas recirculation (EGR) Power Train Engine Oil Power Train Automatic transmission oil Power Train TPMS Safety Brake Booster Safety Side airbags Safety Pedestrian protection Safety HVAC	Process control HVAC Transportation	Smart phones & tablets Drones Wearable Smart homes/building Electronic cigarette	Blood monitoring invasive Blood monitoring non invasive Respiratory Smart inhaler Others	Air Data FADEC Hydraulic & others

Accelerometers					
Single accelerometers for consumer	**Accelerometers for automotive**	**Accelerometers for Medical**	**Accelerometers for industrial**	**Accelerometers for aeronautics**	**Accelerometers for Defense**
Cellphone Tablets Gaming Remote controls Wearable Others (Home Automation, PMP, Laptop, handheld GPS, PC peripherals, toys…)	Standalone airbag front sensor Airbag peripheral sensor ESC acceleration sensor Roll over sensing TPMS Other: integrated GPS, active suspension, safety, vibration, EPB	Accelerometer for pacemaker Accelerometer for other healthcare applications	Seismic - Geophones Antenna stabilization Industrial vibration monitoring Inclinometers Offshore - Directional drilling + survey GPS aiding, agriculture / mobile mapping Other industrial applications	AHRS Navigation Other aero (vibration monitoring...)	Missiles, guided munitions, bombs Defense stabilization systems Navigation and other defense applications

YOLE Développement

MEMS Sensor Applications Overview

DEFINITIONS: MEMS APPLICATIONS TRACKED BY YOLE (2/3)

Gyroscopes					
Single Gyroscopes for Consumer	**Gyroscopes for Automotive**	**Gyroscopes for Industrial**	**Gyroscopes for medical**	**Gyroscopes for Aeronautics**	**Gyroscopes for Defense**
Mobile phone Mobile phone (OIS) Tablets Gaming Remote controls Wearable Others (DSC, pmp, laptop, handheld GPS, PC peripherals, toys…)	Roll over ESC gyroscope GPS navigation	Stabilization systems GPS aiding - Mobile mapping ROVs / AUVs navigation for offshore First responder systems Drilling Fall detection Other commercial applications	Wearables	AHRS for general aviation / backup instrument Flight control for civil helicopters and aircrafts / navigation for civil & paramilitary UAVs / Others Space satellites, spacecraft & skyrockets	Platform stabilization Missiles guidance, Guided munitions / bombs Defense UAV & UGV navigation / control , Others

Inertial combos			
Consumer Accel Gyro combos	**Consumer Accel Magneto combos**	**Consumer 9 DOF combos**	**Auto combos Accel Gyro**
Mobile phone Tablets Others	Mobile phone Tablets Others	Mobile phone Tablets Medical Others (Wearables, Home Automation, PMP, Laptop…)	ESC combo, rollover Robotic cars

Inertial combos			
Consumer Accel Gyro combos	**Consumer Accel Magneto combos**	**Consumer 9 DOF combos**	**Auto combos Accel Gyro**
Mobile phone Tablets Others	Mobile phone Tablets Others	Mobile phone Tablets Medical Others (Wearables, Home Automation, PMP, Laptop…)	ESC combo, rollover Robotic cars

Magnetometers	
Single Magnetometers for consumer	**Magnetometers for automotive**
Cell phones Tablets Other consumer applications (wearables)	Auto

Optical MEMS						
Optical MEMS for Telecom	**Optical MEMS for Medical**	**Optical MEMS for Industrial**	**Optical MEMS for Automotive**	**Optical MEMS for Aeronautics**	**Optical MEMS for Consumer**	**Optical MEMS for Defense**
Switches VOAs Others (tunable filters, optical benches, transceivers)	Microspectrometers HMDs	Adaptive Optics Digital Cinema	HUDs Lidars	HUDs	Home cinema projector (including laser TV) Pico projector (stand alone and embedded) Office projector Autofocus	HMDs

YOLE Développement

10

MEMS Sensor Applications Overview

DEFINITIONS: MEMS APPLICATIONS TRACKED BY YOLE (3/3)

Micro bolometers				
Microbolometers for Automotive	Microbolometers for Industrial	Microbolometers for Defense	Microbolometers for Consumer	Microbolometers for Industrial
Night Vision	Firefighting, maritime, surveillance, thermography, PVS	Night Vision	Mobiles & tablets & other commercial (UAV, EVS, etc)	Predictive maintenance, building, process control

PIR, thermodiodes & thermopiles				
Thermodiodes for Industrial	PIR arrays (1x8 to 64x64) thin films or CMOS based	Thermopiles arrays high end	Thermopiles low end	Thermopiles arrays (1x8 to 64x80)
Predictive maintenance, building, process control	People counting, spectrometry	Industrial T measure, gas & fire detection	Wearable (spot thermometer) Medical	HVAC, smart buildings

Microfluidics	
Microdispensers & Drug Delivery	Si biochips
Inhalers MEMS Micropumps & Microvalves Microneedles	POC testing Next Gen Sequencing & Sample Preparation

RF MEMS				
RF switches for telecom	RF switches for industrial	Switch for Space	RF switches for defense	RF MEMS for cellphones
RF switches for base stations RF switches for small cells	RF switches for ATE & RF Instrumentation	Redundant Matrix Commutation Matrix Radars & Communications	RF switches for communications RF switches for radars	BAW Filters & Duplexers RF Switches (antenna) Antenna tuners

Oscillators and resonators			
Consumer	Industrial	Automotive	Infrastructure & telecom
TV, DSLR Mobile, wearable, IoT	IIoT	Automotive	Base stations, servers, routers,…

Micro tips
Micro tips & probes
Micro tips for AFM Probes for ATE

Flowmeter
Flow meter
flow meter for medical and Diagnostics flow meter for industrial

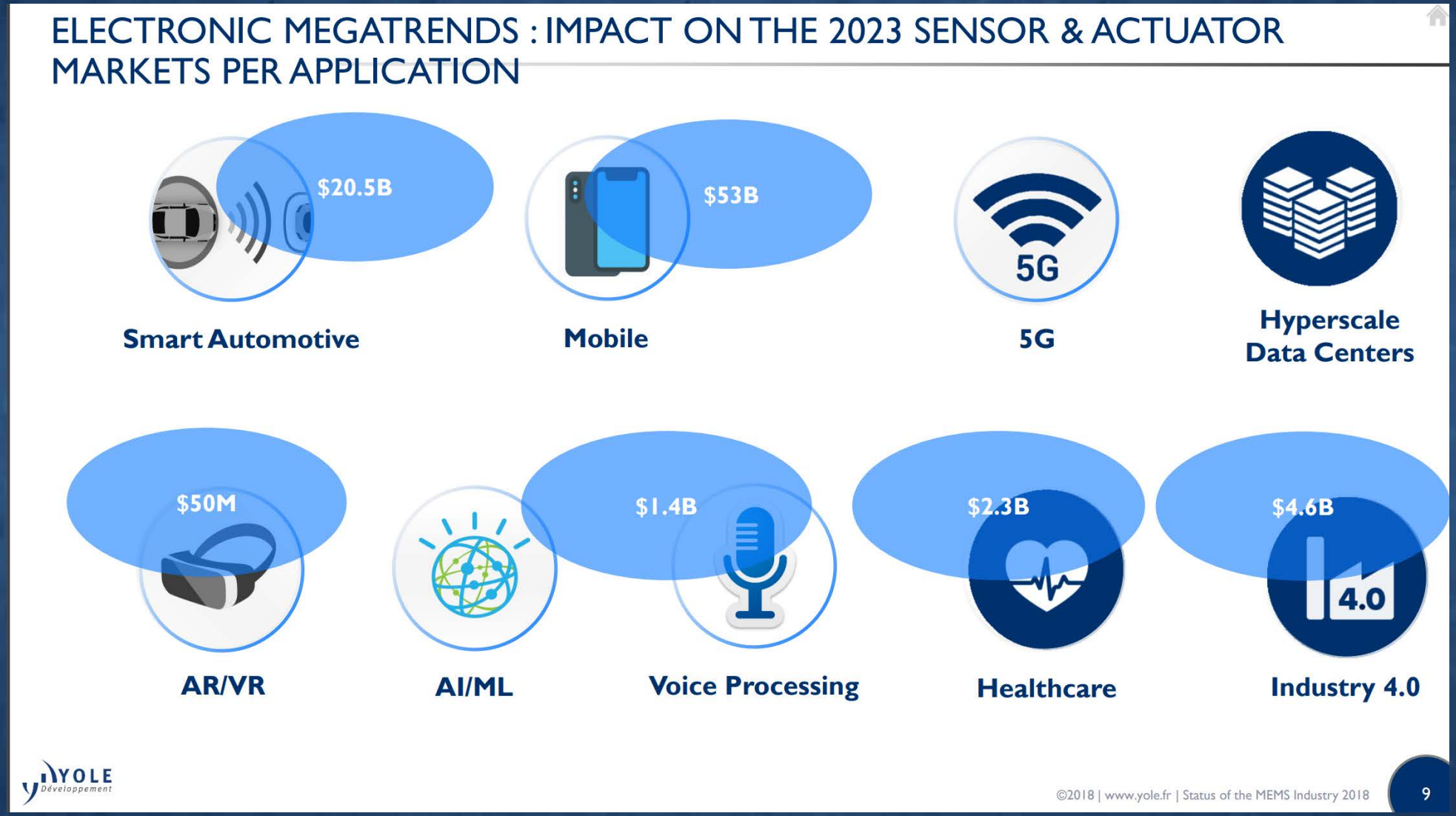
Environmental MEMS		
Humidity	Gas	Combos (multi-gas, humidity, temperature, pressure)
Humidity for automotive Humidity for consumer Humidity for industrial	Chemical MEMS / Gas sensor	Environmental hub

Others
Micro structures, micro valves Ultra sonic finger print Micro speaker

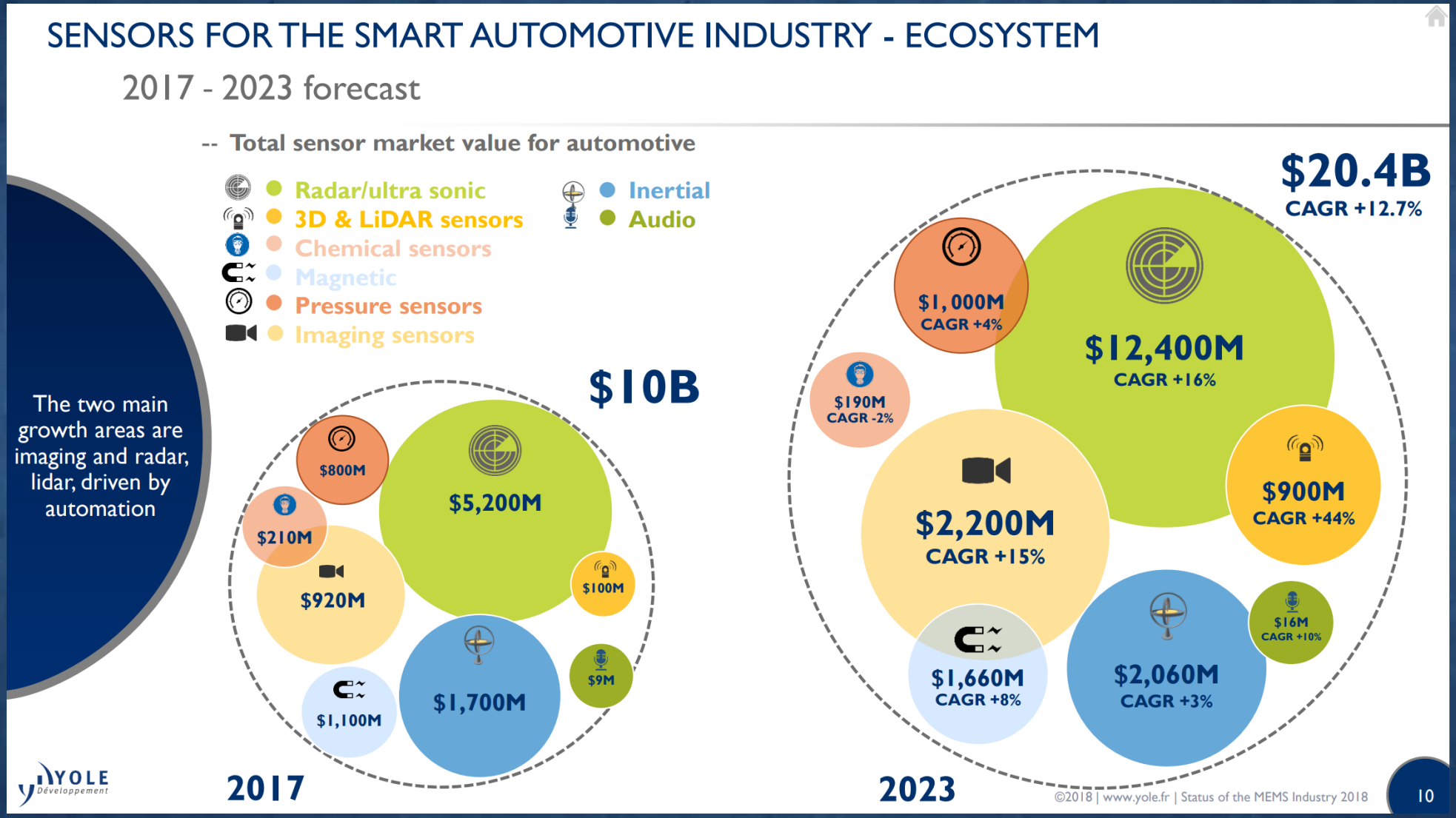
YOLE Développement

11

Key MEMS Device Applications



Automotive MEMS Device Overview



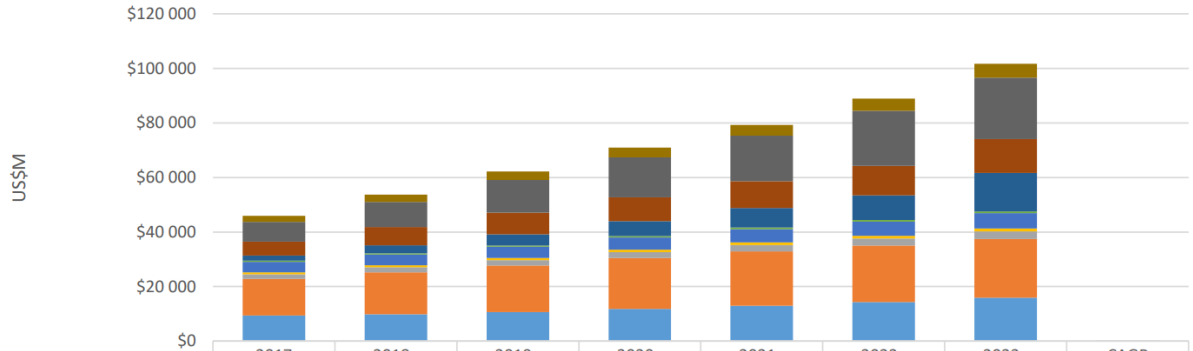
Automotive MEMS Device Overview

SEMICONDUCTOR-BASED SENSORS AND ACTUATORS FORECAST, BY DEVICE IN US$M

The MEMS and sensors market will reach $100B in 2023

From $50+B in 2018 to $100+B in 2023!

MEMS & Sensors forecast 2017-2023

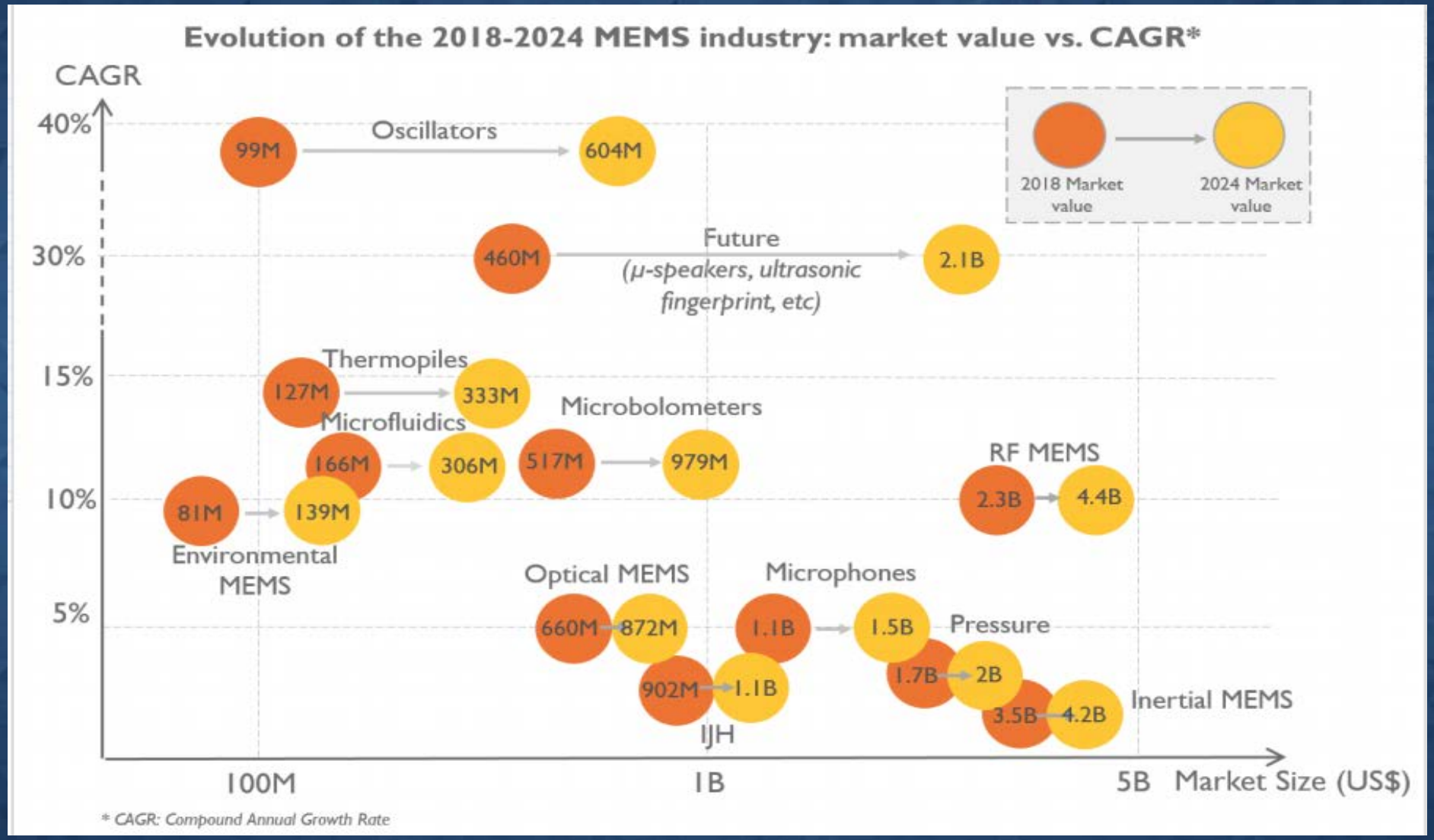


	2017	2018e	2019e	2020e	2021e	2022e	2023e	CAGR
OTHERS	$2 299	$2 687	$3 110	$3 548	$3 965	$4 444	$5 086	14%
RF	$7 191	$9 231	$11 932	$14 678	$16 669	$20 190	$22 537	21%
RADARS	$5 137	$6 671	$8 023	$8 801	$9 830	$10 753	$12 465	16%
3D SENSORS	$1 873	$2 911	$4 045	$5 446	$7 215	$9 034	$14 034	40%
SPECTRAL SENSORS	$399	$446	$490	$538	$587	$640	$698	10%
FINGERPRINT SENSORS	$3 867	$3 977	$4 075	$4 431	$4 847	$5 204	$5 587	6%
GAS SENSORS	$698	$751	$809	$863	$932	$1 017	$1 113	8%
MAGNETIC SENSORS	$1 756	$1 880	$2 016	$2 167	$2 335	$2 522	$2 724	8%
CIS	$13 362	$15 285	$17 033	$18 705	$19 978	$20 737	$21 524	8%
MEMS (excl. BAW)	$9 407	$9 893	$10 660	$11 787	$12 948	$14 336	$15 952	9%

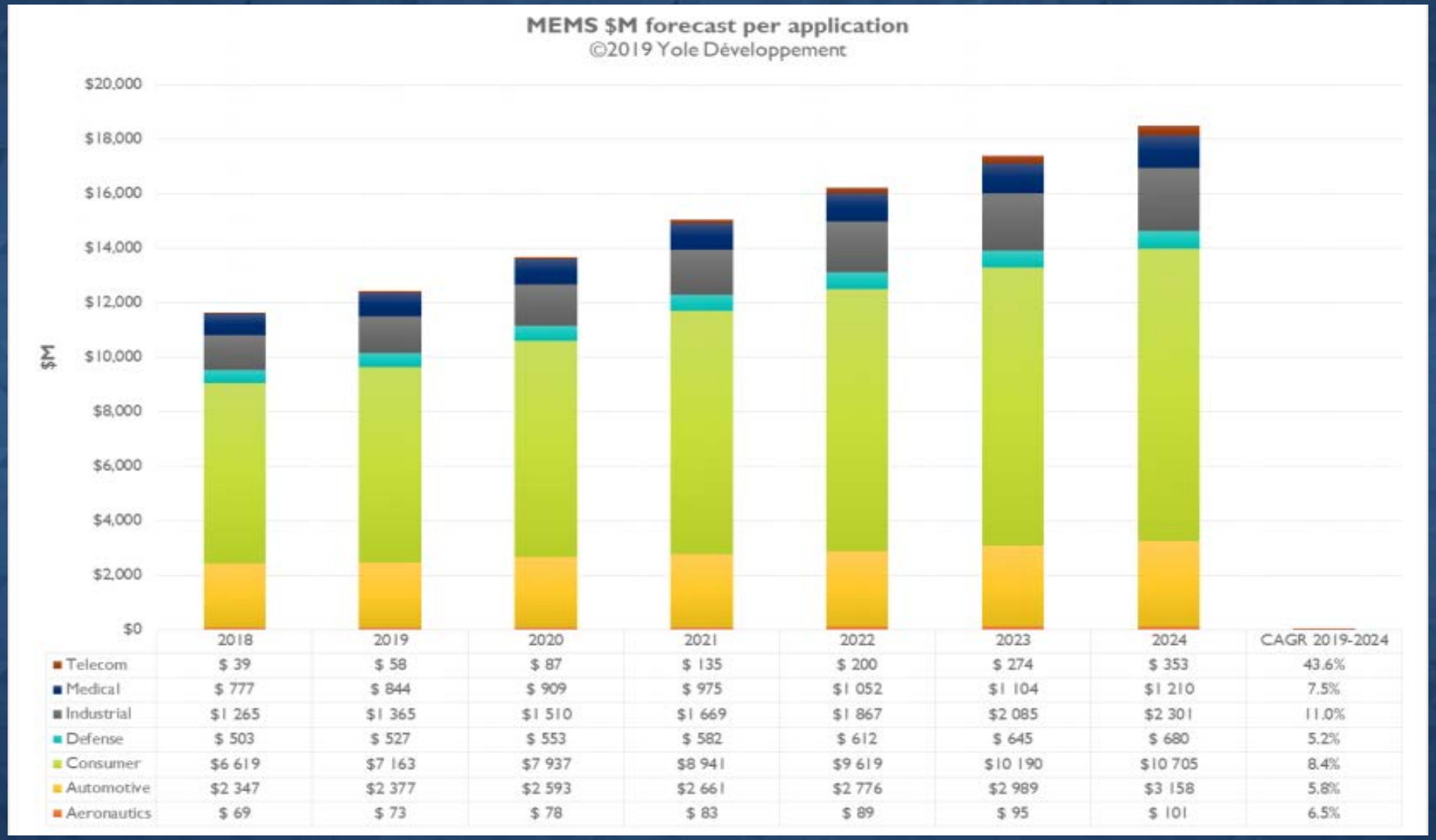
"Others" includes fiber-optic sensors, particle sensors, new sensor developments (such as NEMS)

YOLE Développement

Automotive MEMS Device Overview



Automotive MEMS Device Overview

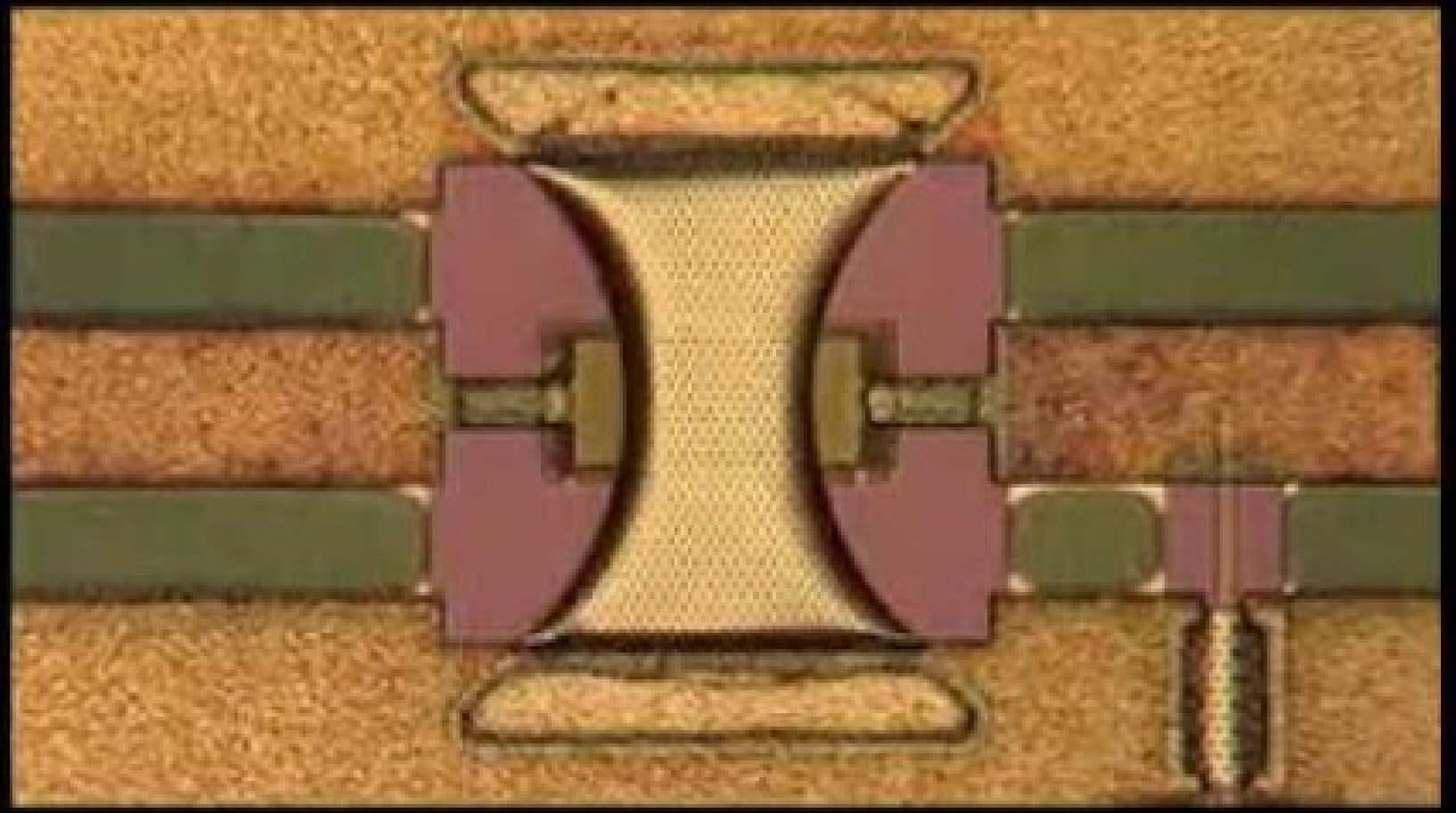


	2018	2019	2020	2021	2022	2023	2024	CAGR 2019-2024
Telecom	$ 39	$ 58	$ 87	$ 135	$ 200	$ 274	$ 353	43.6%
Medical	$ 777	$ 844	$ 909	$ 975	$1 052	$1 104	$1 210	7.5%
Industrial	$1 265	$1 365	$1 510	$1 669	$1 867	$2 085	$2 301	11.0%
Defense	$ 503	$ 527	$ 553	$ 582	$ 612	$ 645	$ 680	5.2%
Consumer	$6 619	$7 163	$7 937	$8 941	$9 619	$10 190	$10 705	8.4%
Automotive	$2 347	$2 377	$2 593	$2 661	$2 776	$2 989	$3 158	5.8%
Aeronautics	$ 69	$ 73	$ 78	$ 83	$ 89	$ 95	$ 101	6.5%

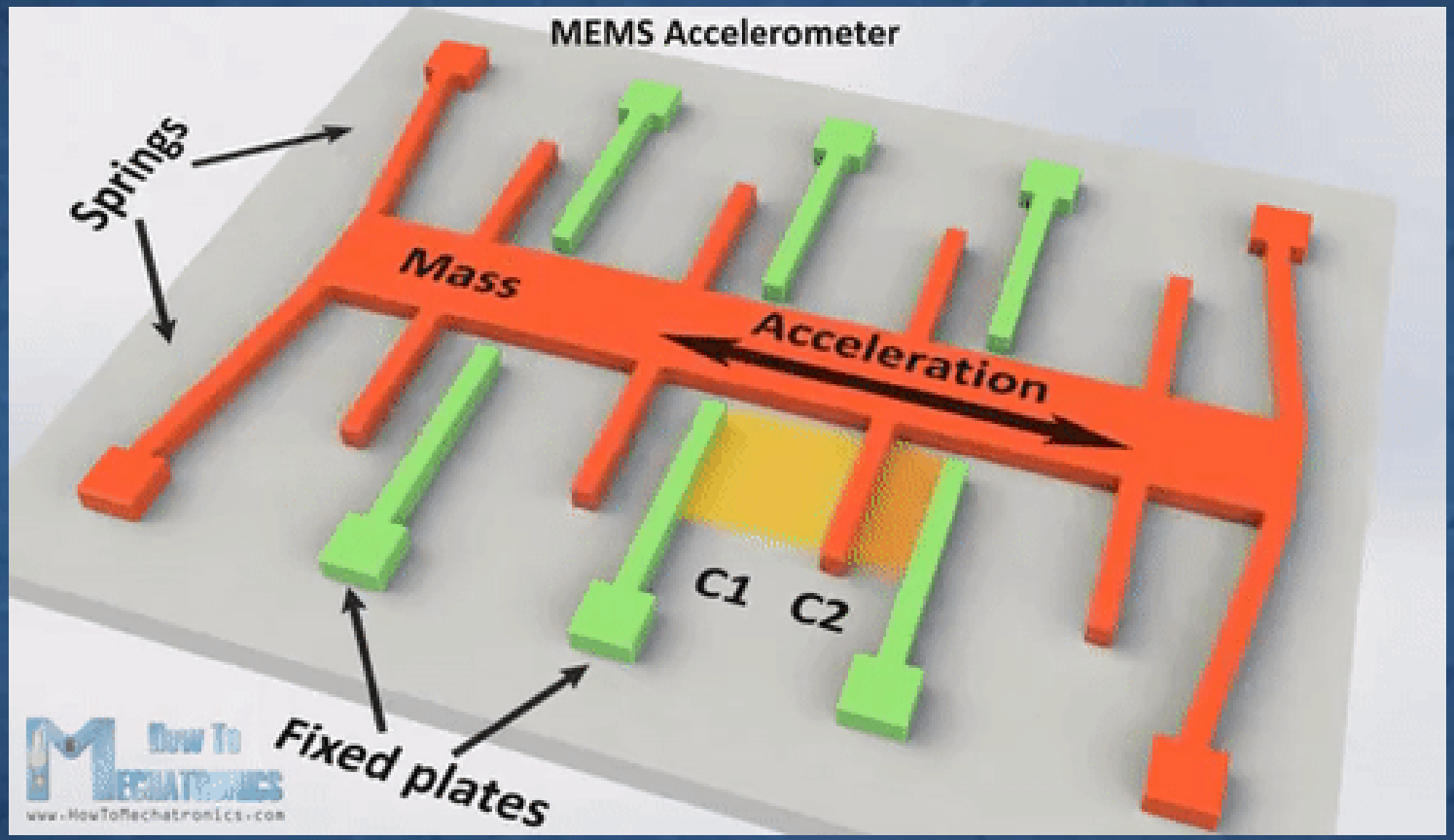
MEMS Device Testing Overview

- MEMS die have mechanical structures fabricated into them requiring additional physical and environmental stimulus beyond traditional electrical and thermal cycling testing. Henceforth, legacy ATE solutions were not designed to provide these unique test stimulus; induced motion, induced magnetic fields, induced pressure, induced gasses, induced sound…
- New test solution were required and companies such as AFORE, Multitest, Solidus, SPEA, FocusTest, Tessec, Rasco/Coho, Tel and others developed ATE solutions that provide the additional stimulus to activate the MEMS structures during electrical measurements.
- In the case of IMUs, Gyros, Accelerometers and combi-sensors, directional movement, multi-axis rotation, infinite position angles, cycle magnetic fields are required to transduce the analog stimulus inputs to digital outputs.

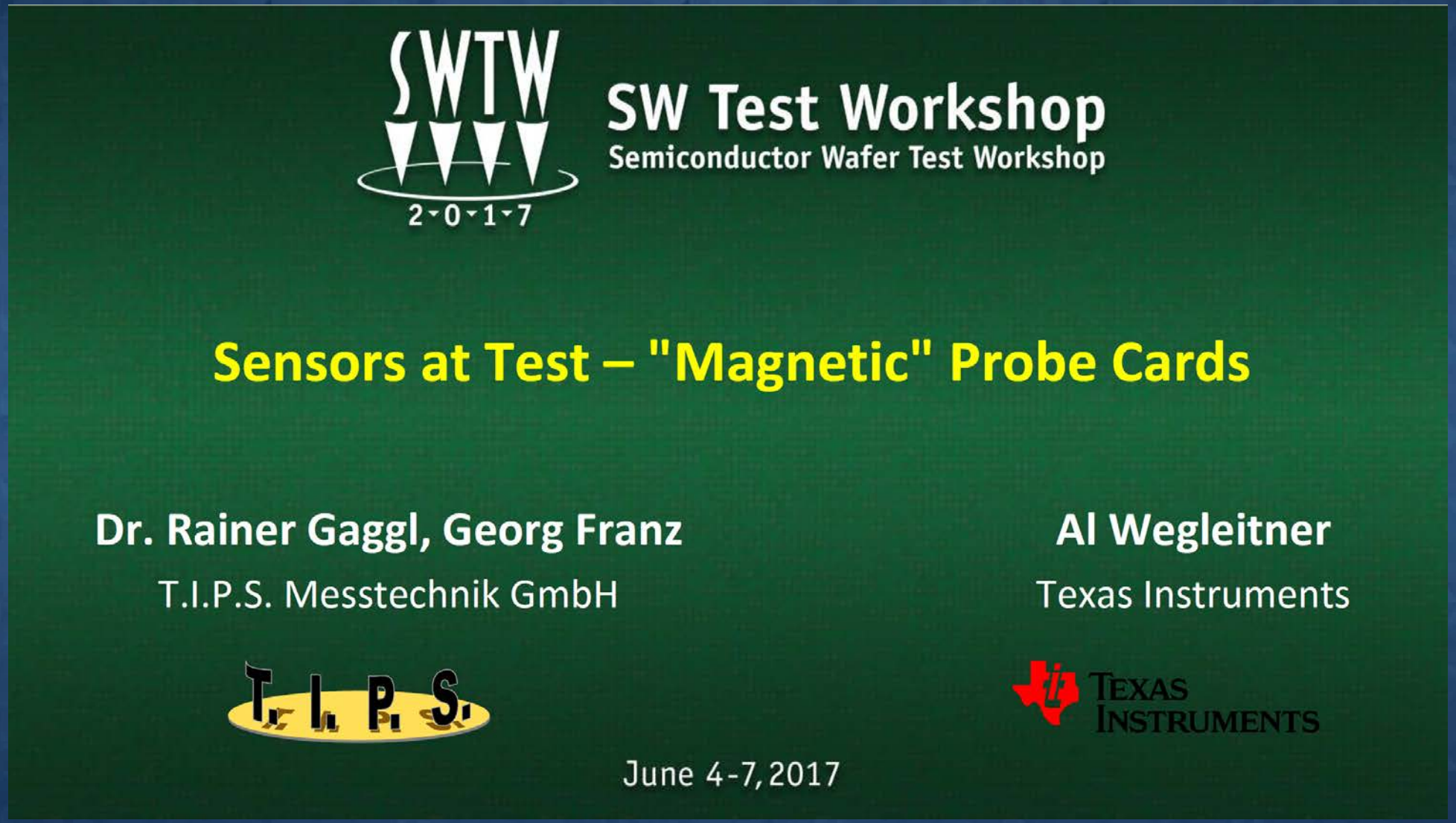
MEMS RF Switch



Example Of MEMS Structures



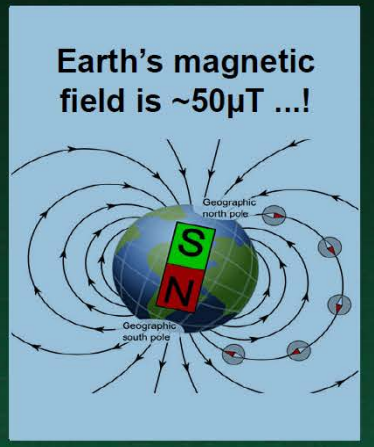
Reference Of Previous SWTW Work

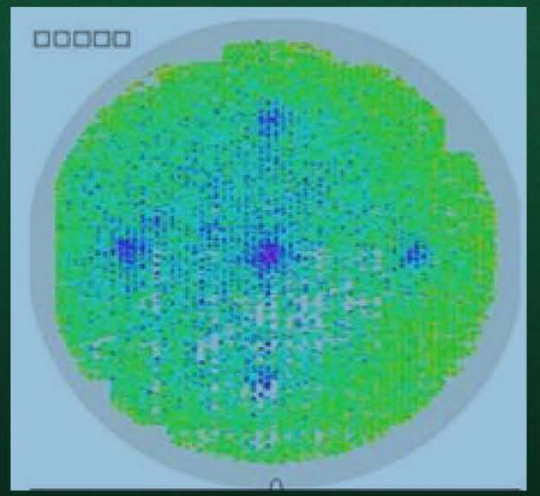


Reference Of Previous SWTW Work

Stray Magnetic Fields

- **Expect no external magnetic fields at the DUT for offset measurements**
- **Gauss meter used to quantify stray fields in prober**
  - Sharp corners on casing produce ~400µT
  - Permanent magnets used for scrub pad and position switches up to 20mT (outside of DUT)
  - Fields vary ±30µT at DUT level (probe head powered off)



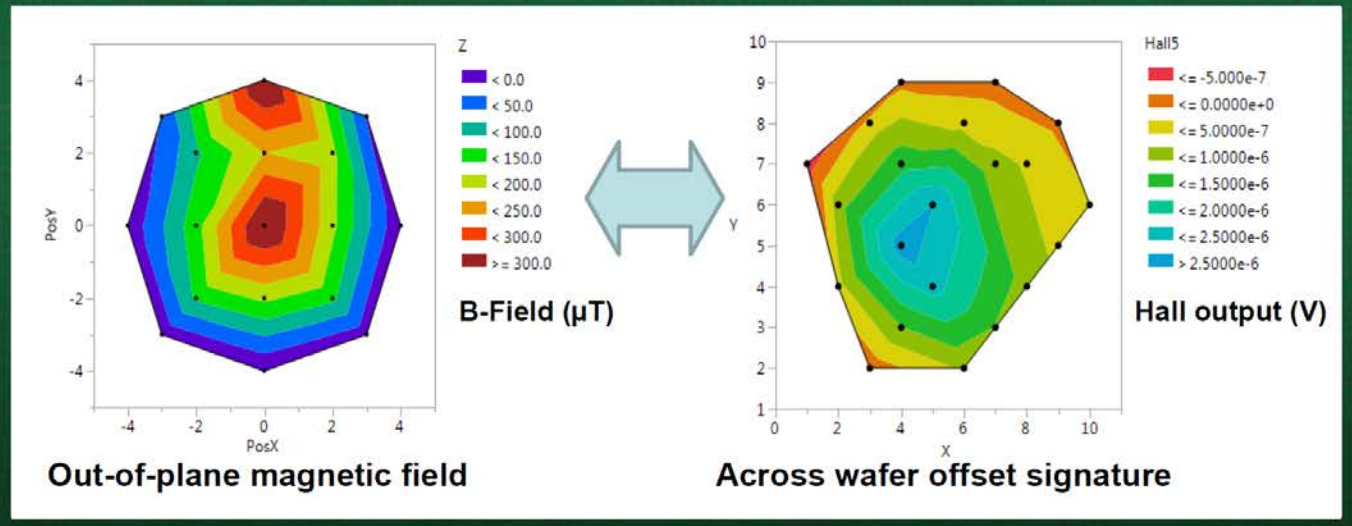


Gaggl et al. SW Test Workshop | June 4-7, 2017 10

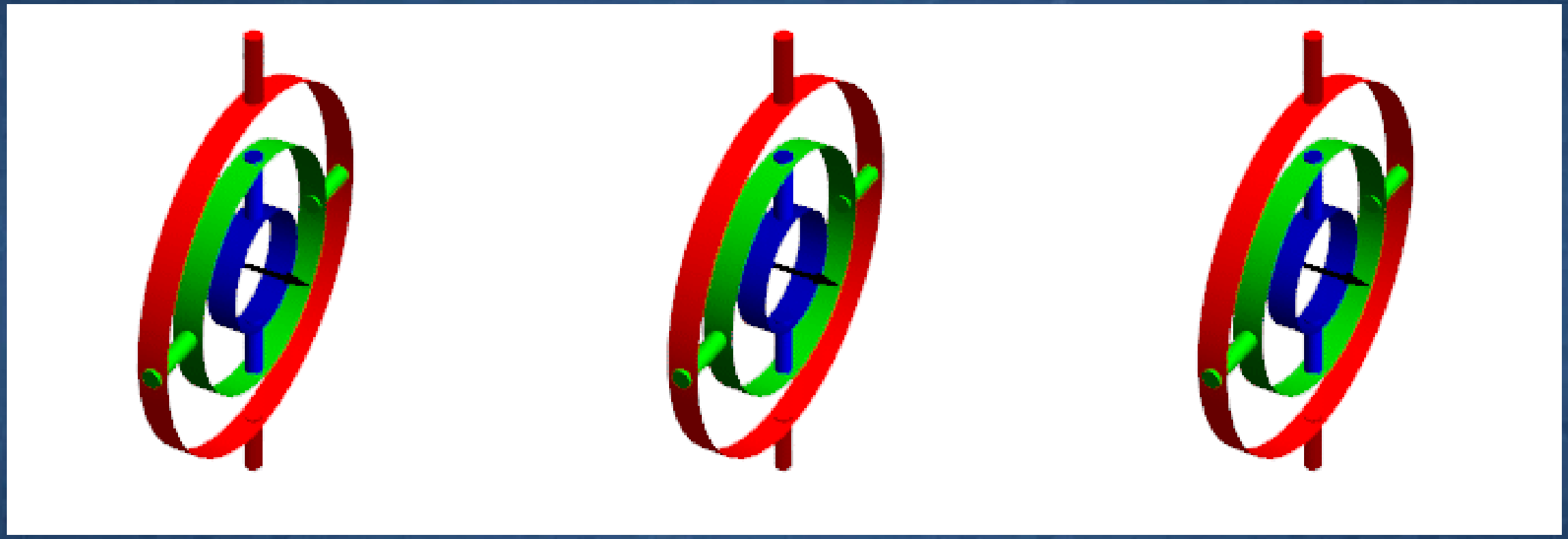
Reference Of Previous SWTW Work

Thermal Chuck Influence

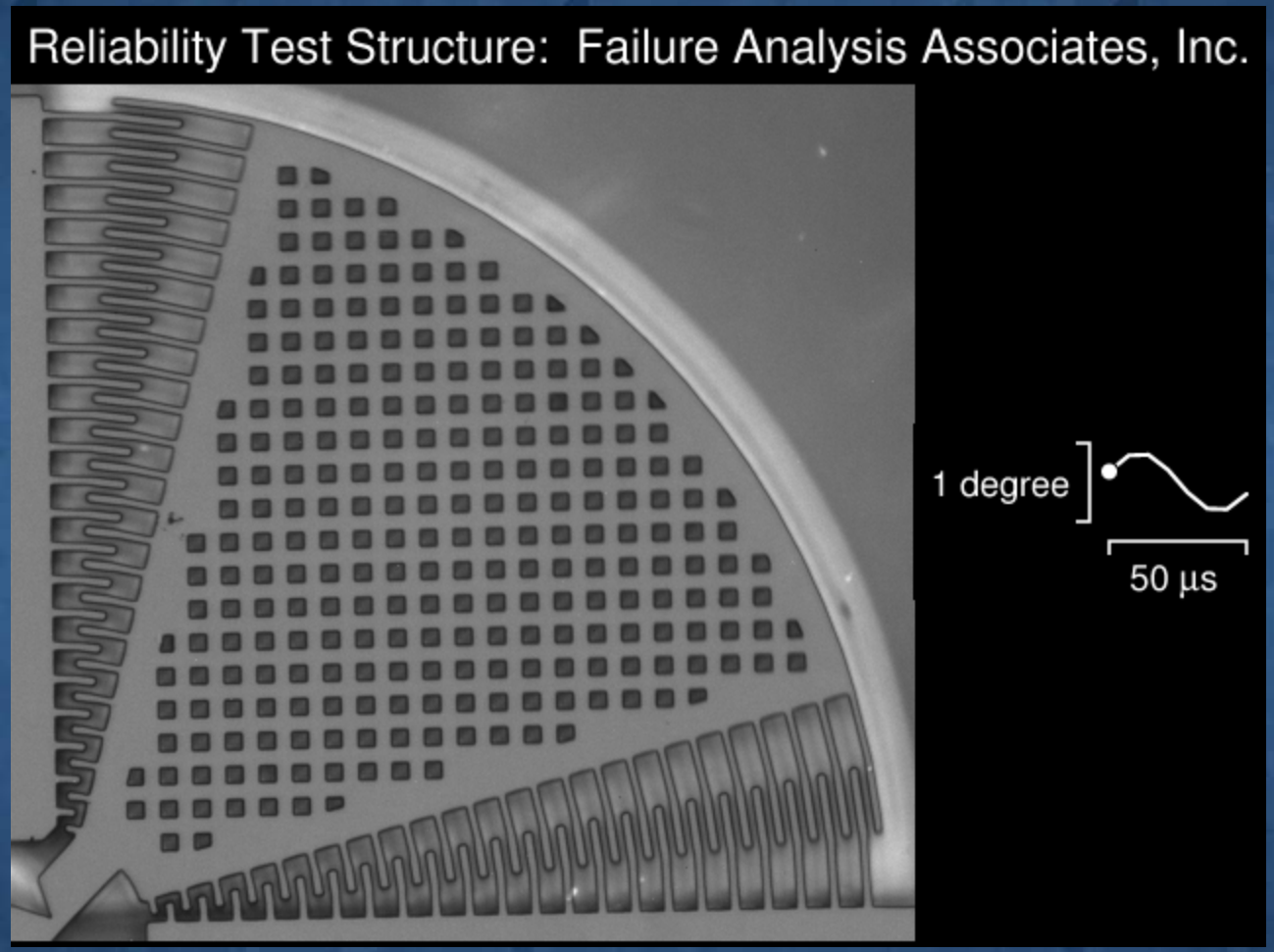
- **Initial testing over temperature displayed variation proportional to increasing chuck temperature**
  - Chuck vendor measured magnetic fields >300µT
  - Heating current is not constant – varies to achieve temperature set point
- **"Anti-Magnetic" probe chucks developed by ERS**
- **Further improvement: Turn off temperature control during probing for more accurate results**



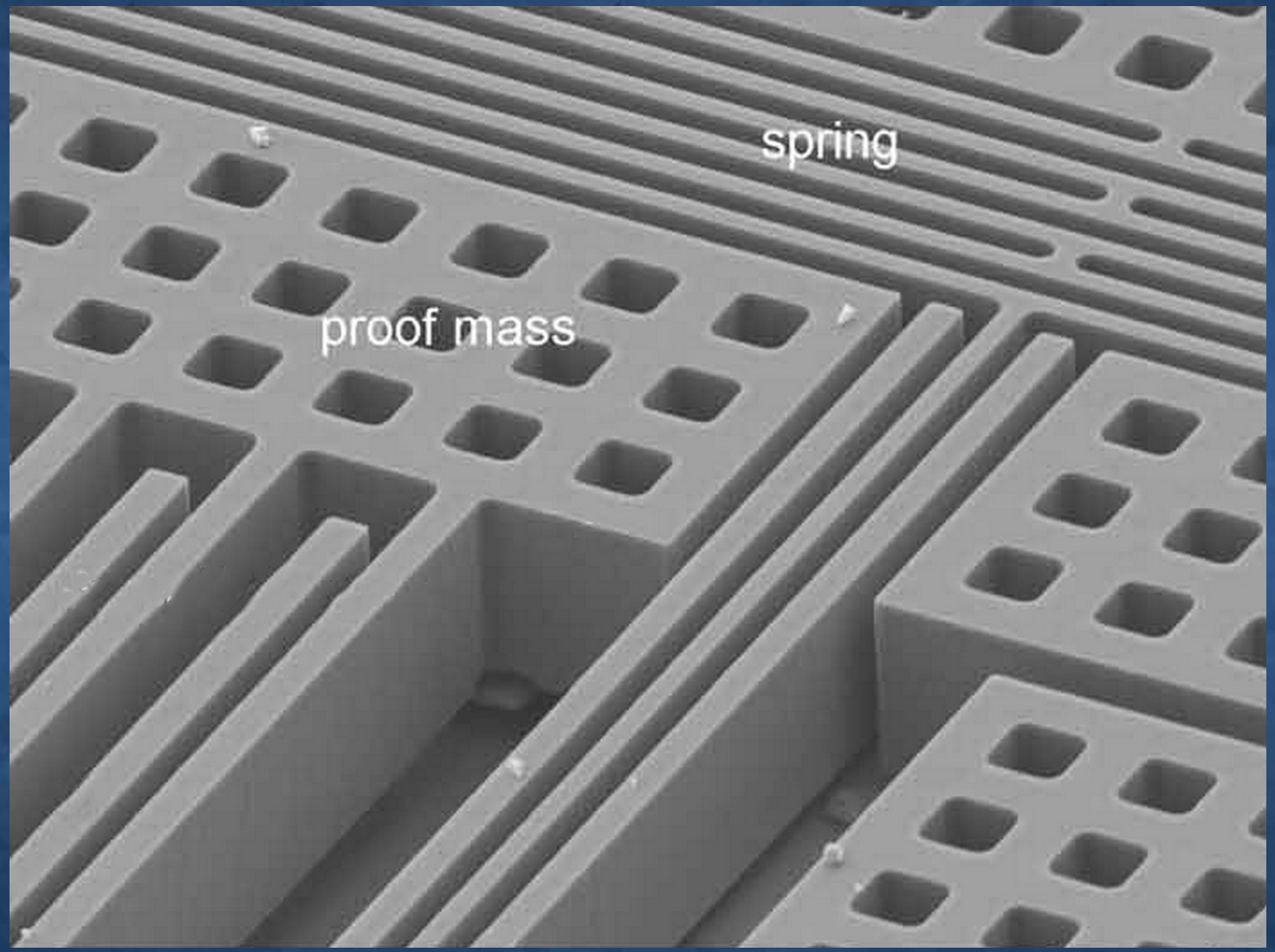
Example - Axis Of Motion



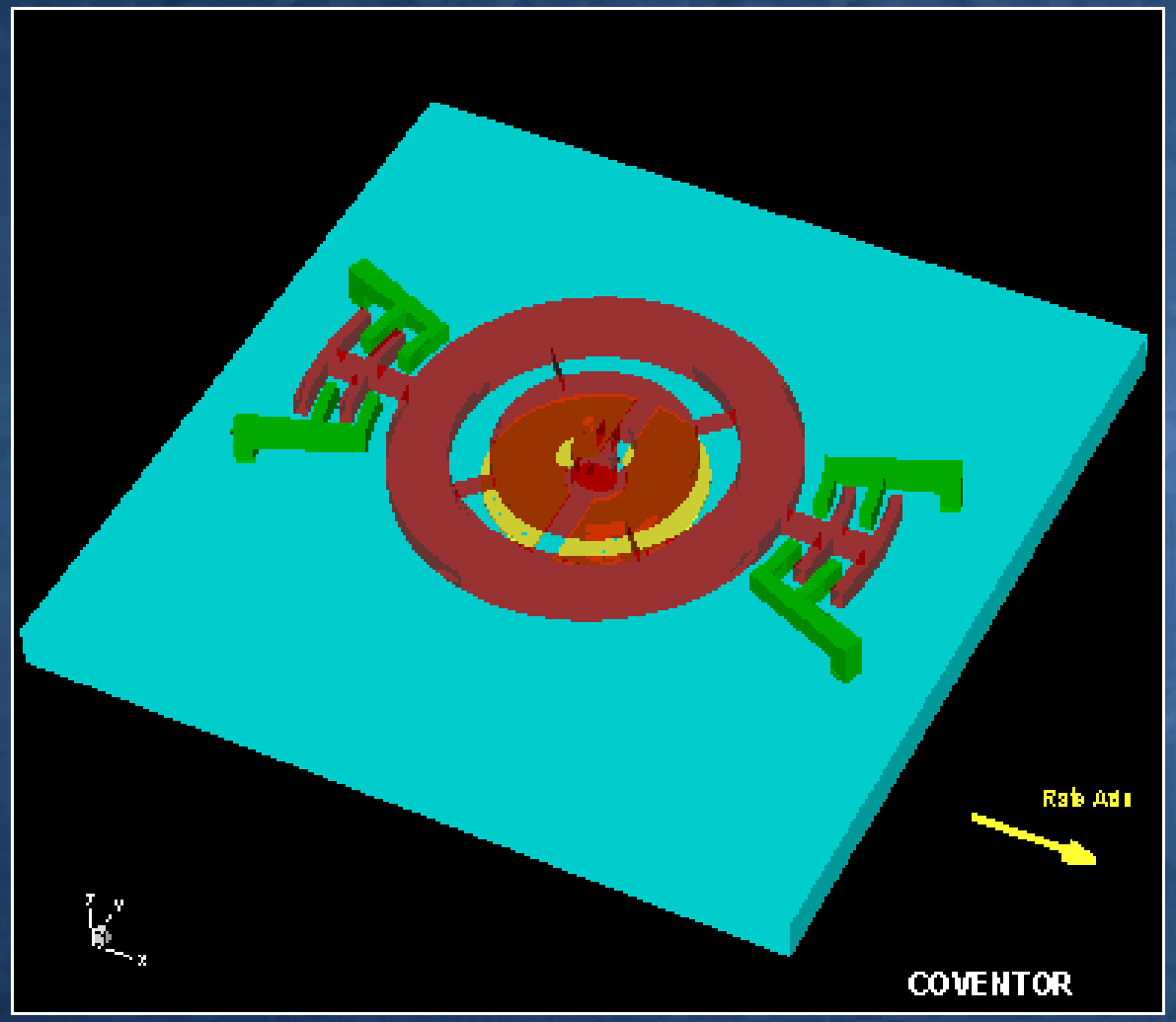
Example Of G-Cell MEMS Structures

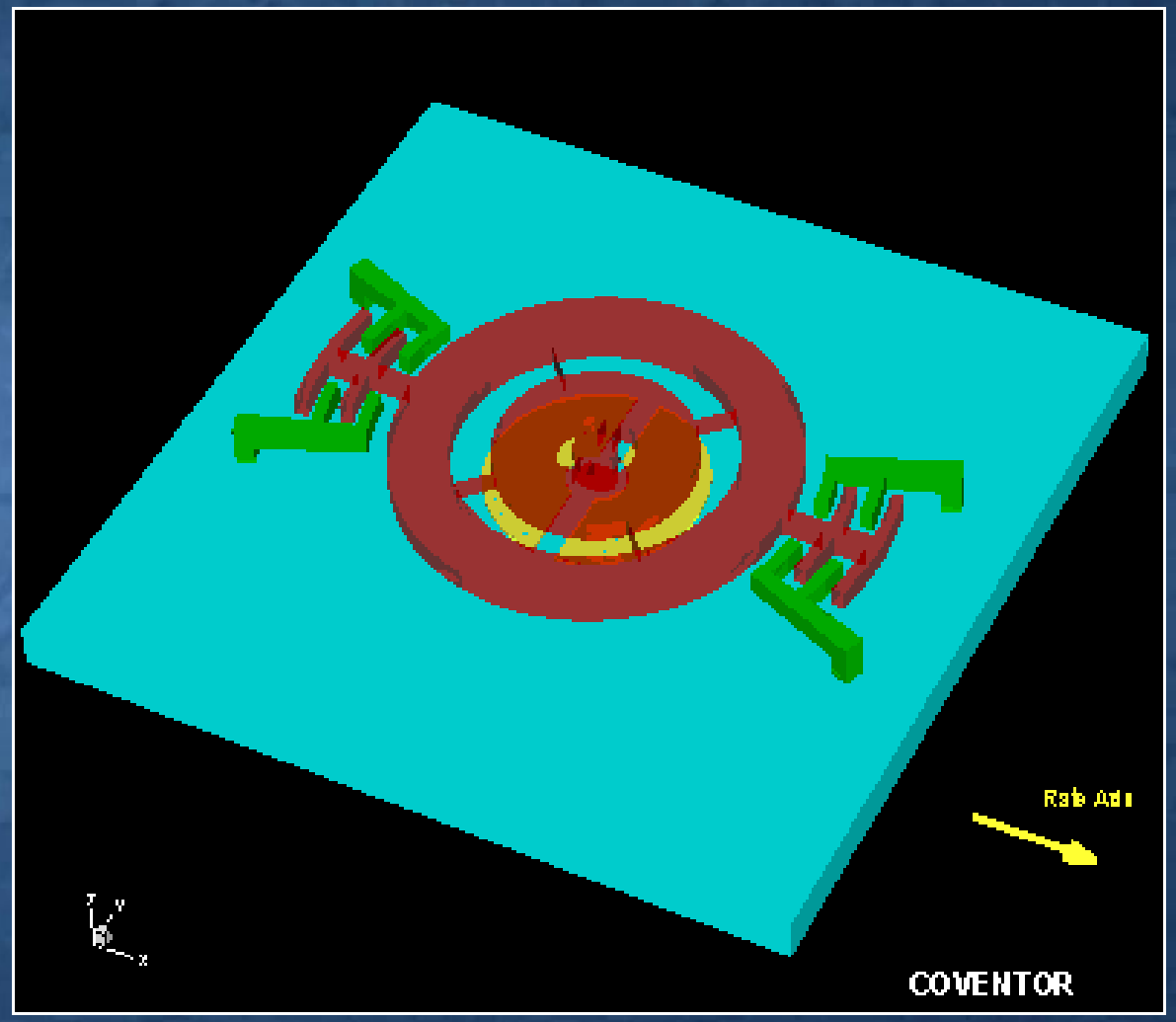


Example Of IMU MEMS Structures

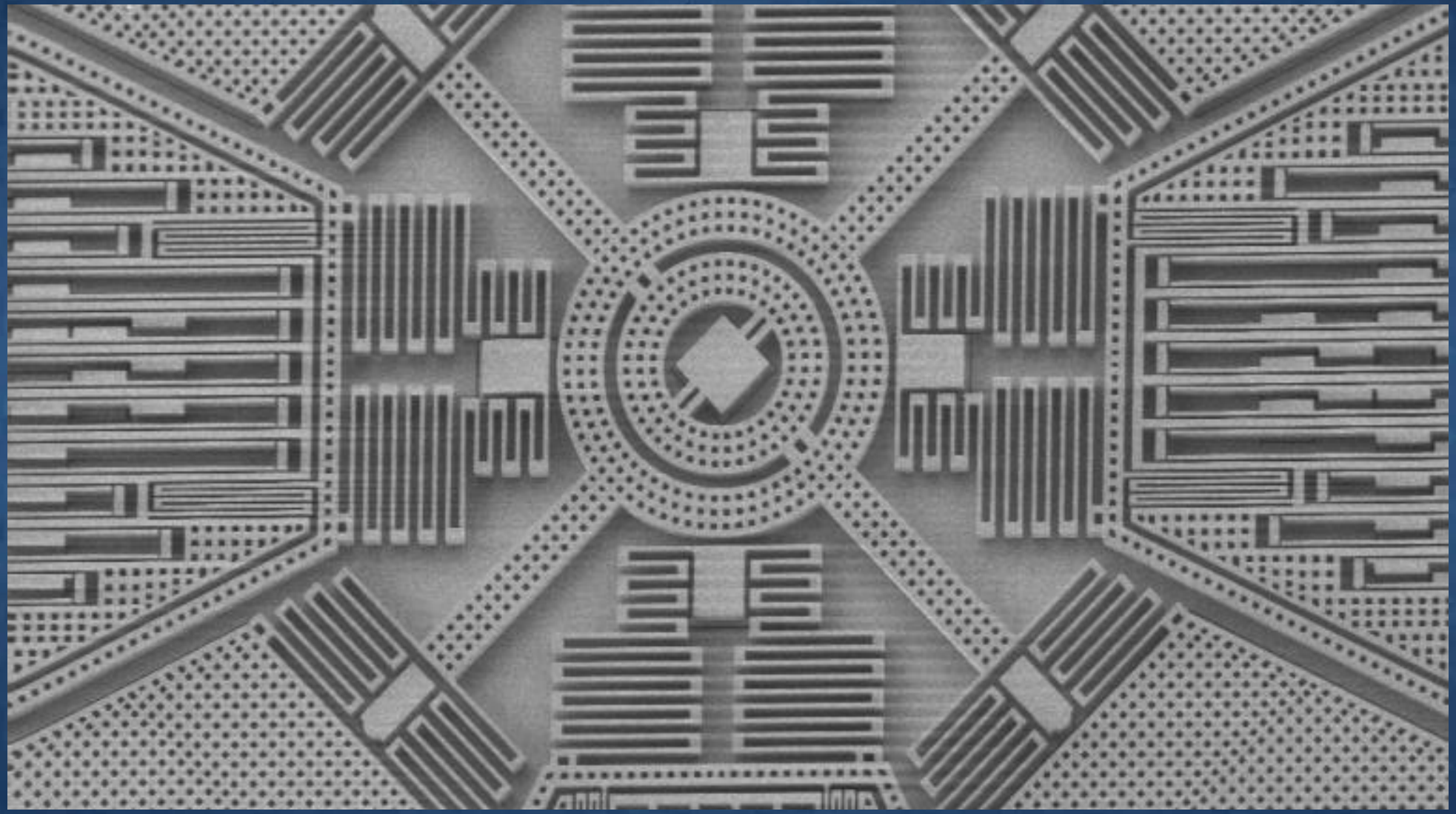


Example Of 2 Axis Gyro MEMS Structures





Example Of Gyro MEMS Structure



Non-Ferrous Metals For Probes

Relative Permeability Of 1.00 = Non-magnetic Properties

RIKA DENSHI

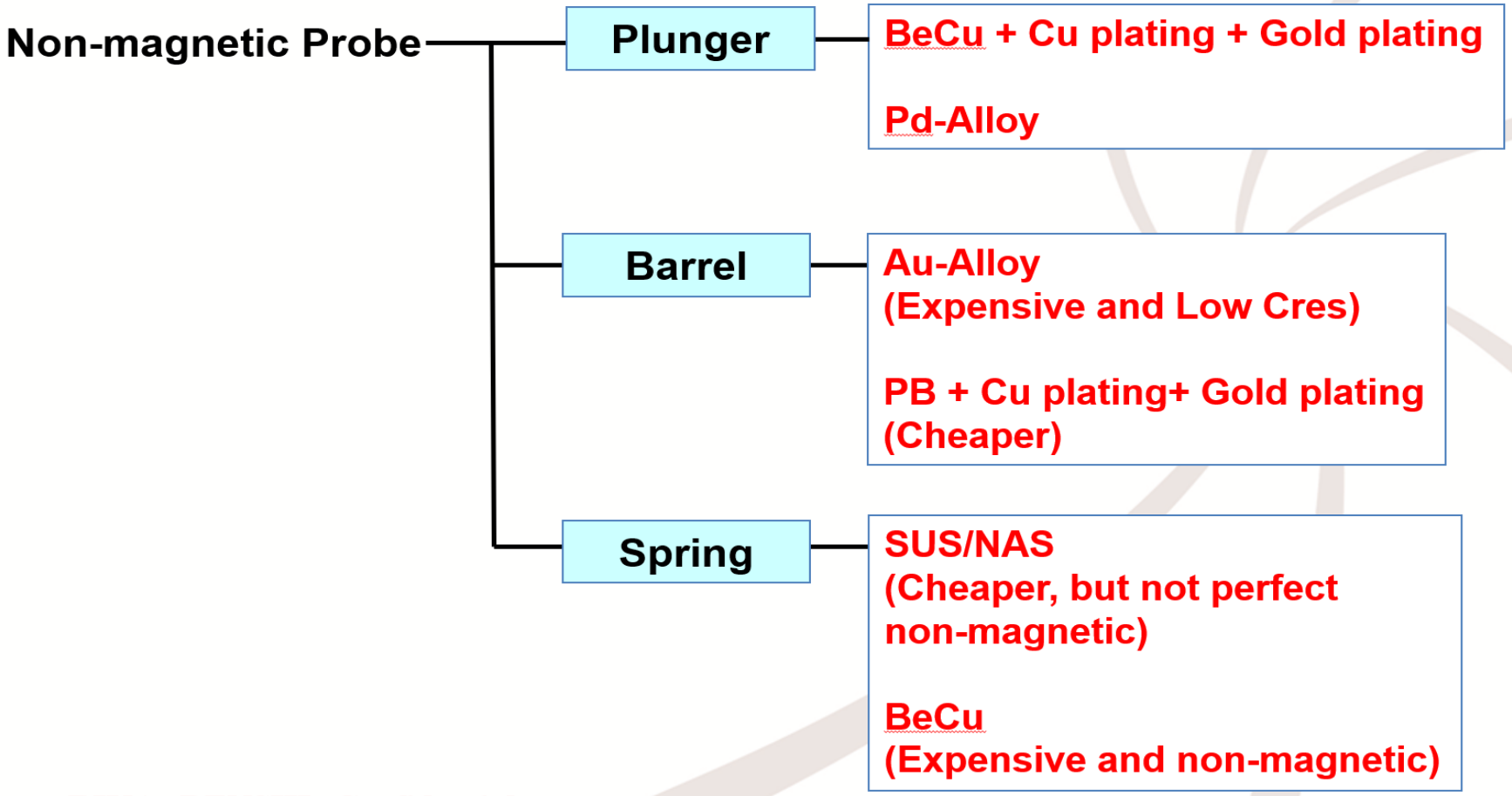
	Material	Relative Permeability
①	BeCu	1.00
②	PDM(Pd-Alloy)	1.00
③	NAS604PH	1.01
④	G4(Gold-Alloy)	1.00
⑤	Electroless Ni plating	1.02
⑥	Gold plating	1.00
⑦	Cu plating	1.00
⑧	PB	1.00

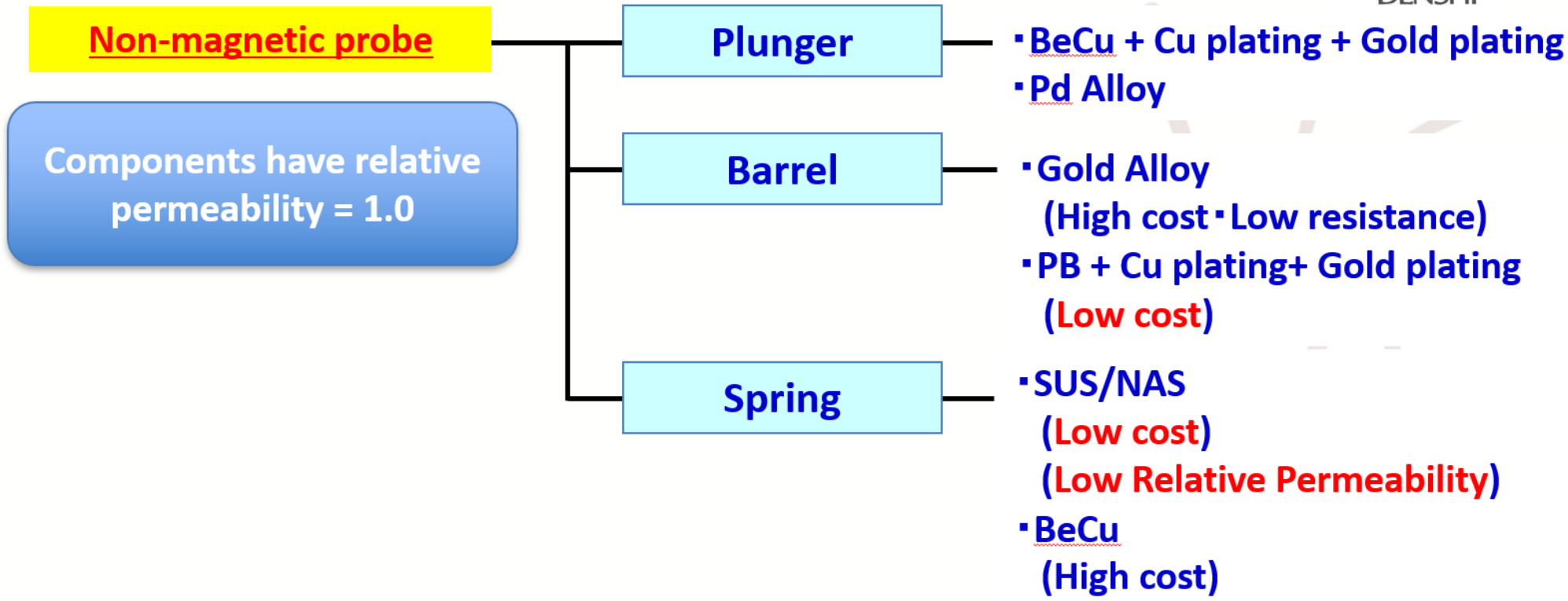
※①～⑤ are our measured values

Spring Probe Materials

Components for Non-magnetic Probe

RIKA DENSHI

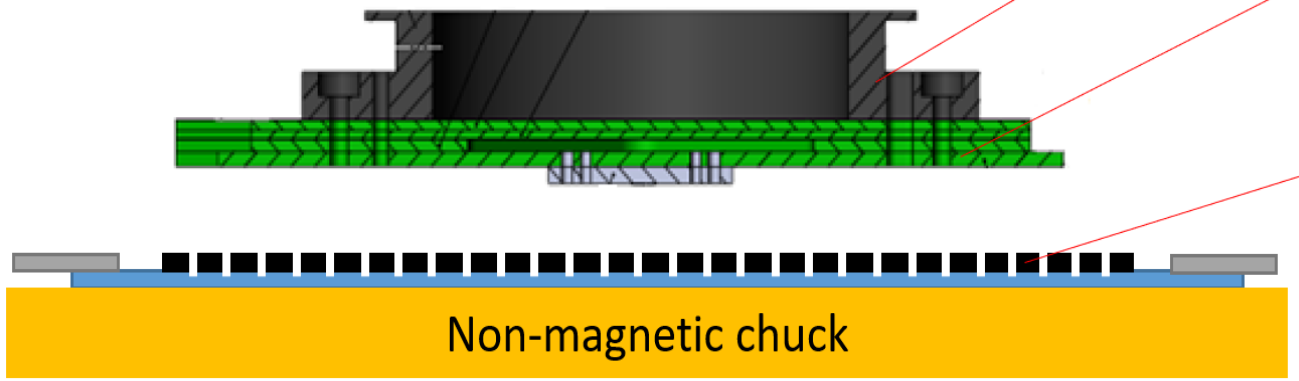




Material	BeCu	Pd alloy	NAS	Au alloy	PB	Gold	Cu
Component	Plunger		Spring	Barrel		Plating	
Relative permeability	1.00	1.00	1.01	1.00	1.00	1.00	1.00

MEMS Gyro Test Application

Test setup



Coil setup to create ±XYZ magnetic field

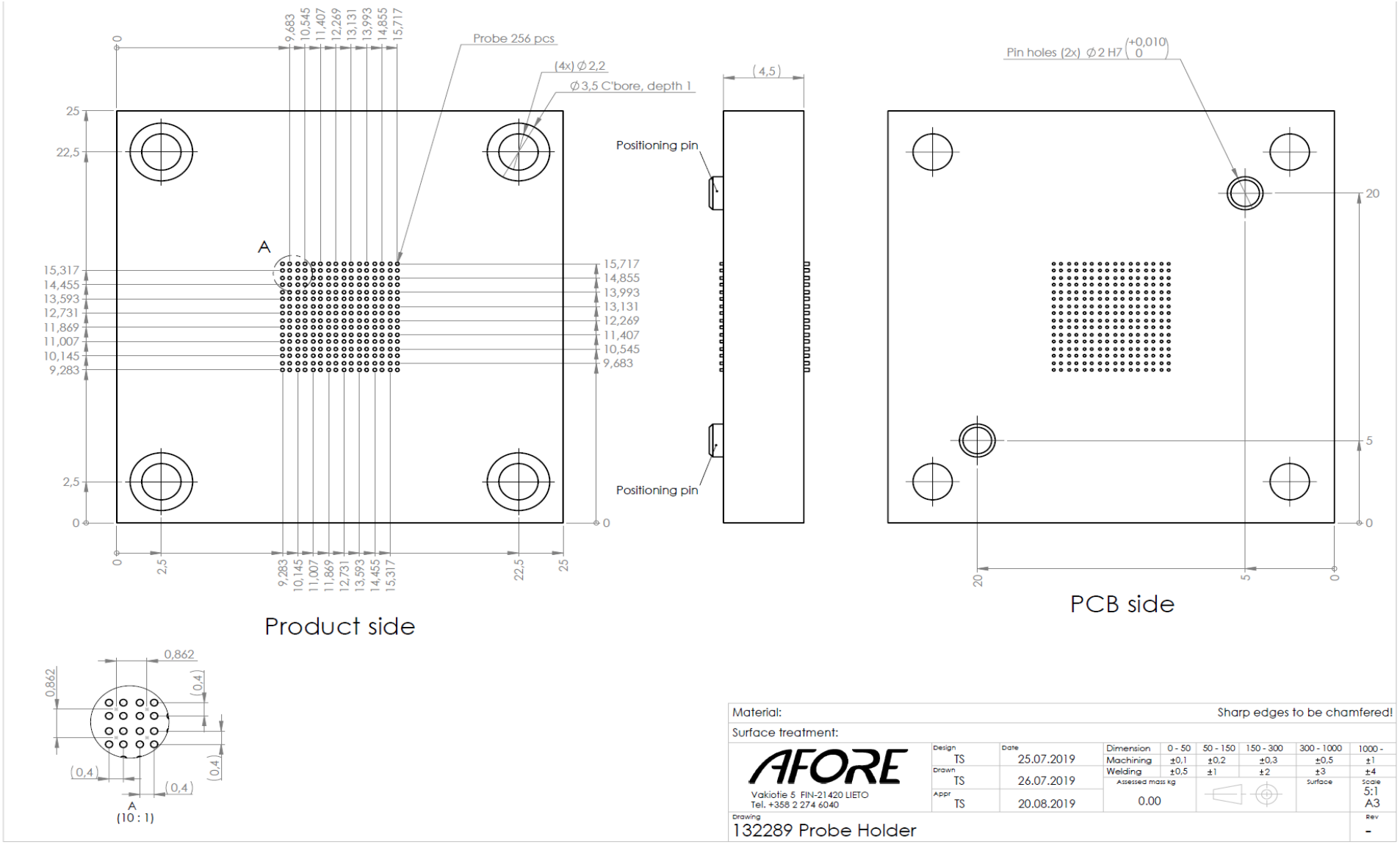
Probe card

Singulated CSP magnetometer wafer on blue tape

Prober: Afore KRONOS rotating frame prober
Magnetic Stimulus Unit (**MSU**) control: National Instruments PXI-based SMU setup

MSU Specification
800 µT stimulus for +/- XYZ axes.
Homogenous area 10 mm x 10 mm
Accuracy in homogenous area +/- 10 µT

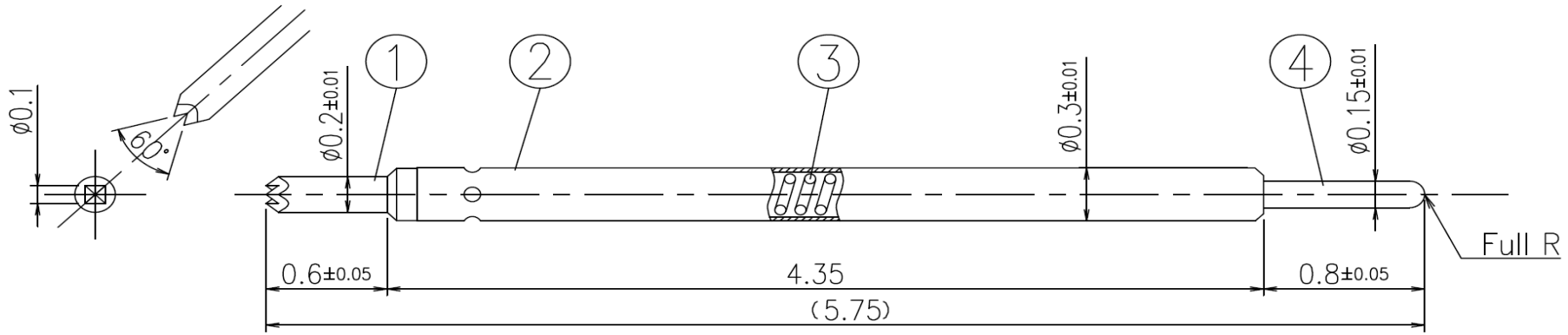
Non-Magnetic Probe Head



300um Non-Magnetic Probe

RIKA DENSHI

Tolerance	±0.1	Angle Tolerance	±1°	Roughness	▽▽▽



This is a marketing drawing.

Stroke	Maximum : 0.65 mm Operating position: 0.5 mm
Spring Force	Initial : 0.088 N (9 g) Operating position: 0.245 N (25 g)

	Product	Material	Finish plating
1	Plunger	Pd–Alloy	–
2	Barrel	Au–Alloy	–
3	Spring	BeCu	Au
4	Plunger	Pd–Alloy	–

Mark	Date	Revision	Approved	Description
1				

Probe name: RZ–030EA–03–PDH

Drawing No.: 19082601

Design	'19.08.26	Drawing	'19.08.26	Approved	'19.08.26	Scale	NTS
	M.SAKAGUCHI		H.KANEO		T.YAMADA	Units	mm

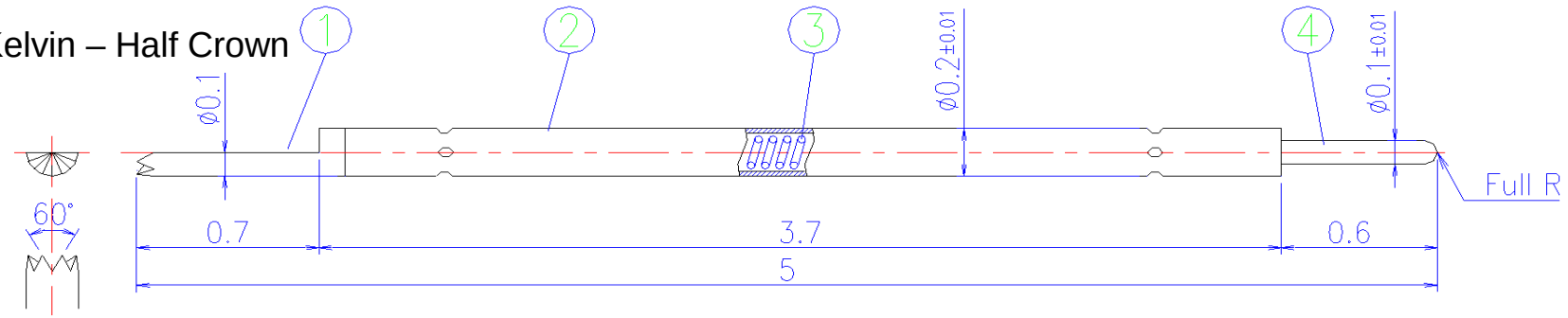
RIKA DENSHI CO.,LTD.

200um Non-Magnetic Probe

RI-020ZA-09-PDH

Tolerance	±0.1	Angle Tolerance	±1°	Roughness	▽▽▽

Kelvin – Half Crown



This is a marketing drawing.

Stroke	Maximum : 0.6 mm	
	Operating position: 0.4 mm	
Spring Force	Initial : 0.039 N (4 g)	
	Operating position: 0.112 N (11.5g)	

	Product	Material	Finish plating
1	Plunger	Pd–Alloy	–
2	Barrel	Au–Alloy	–
3	Spring	BeCu	Au
4	Plunger	BeCu	Au

Mark	Date	Revision	Approved	Description
1				

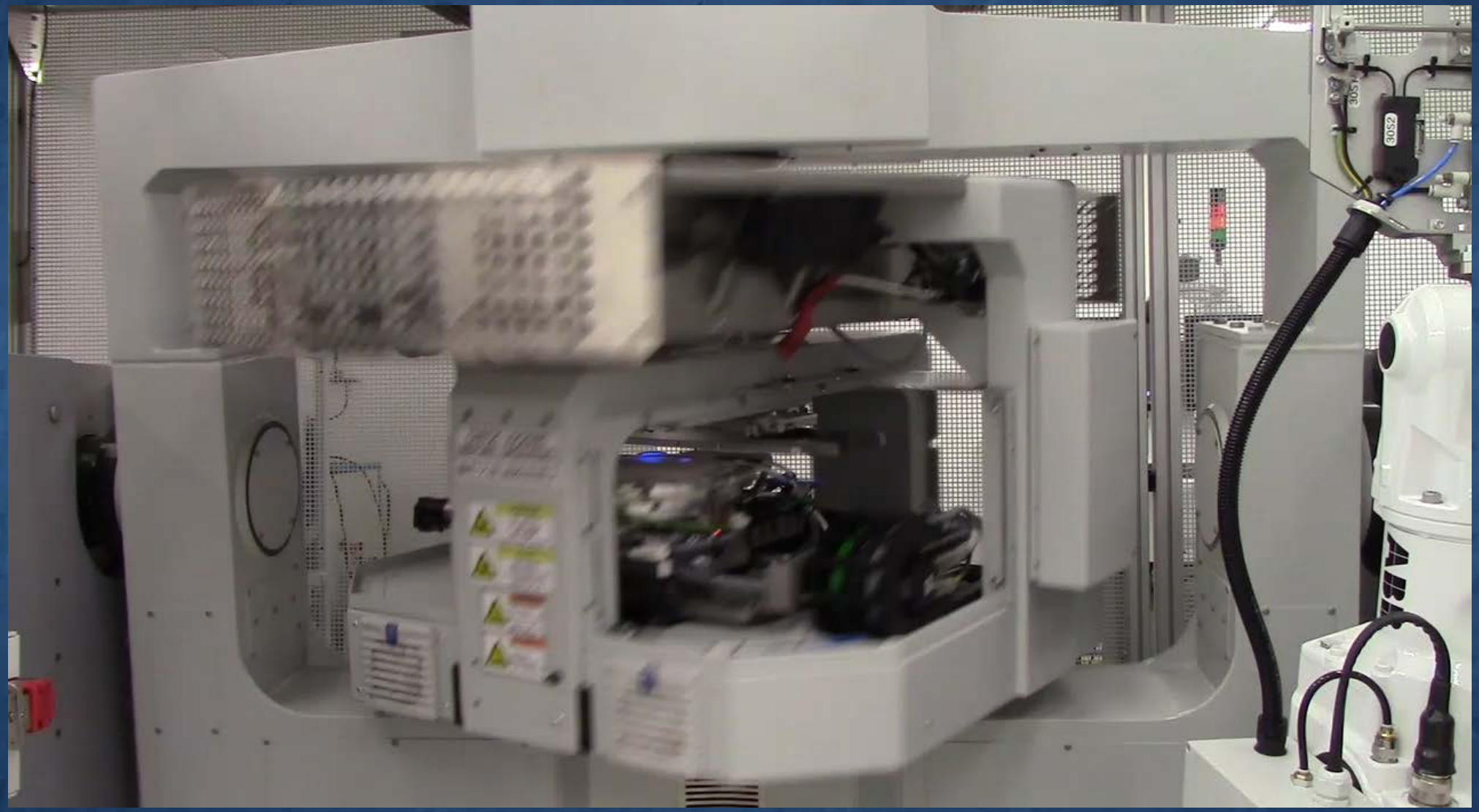
Probe name: RI–020ZA–09–PDH

Drawing No.: 14052901

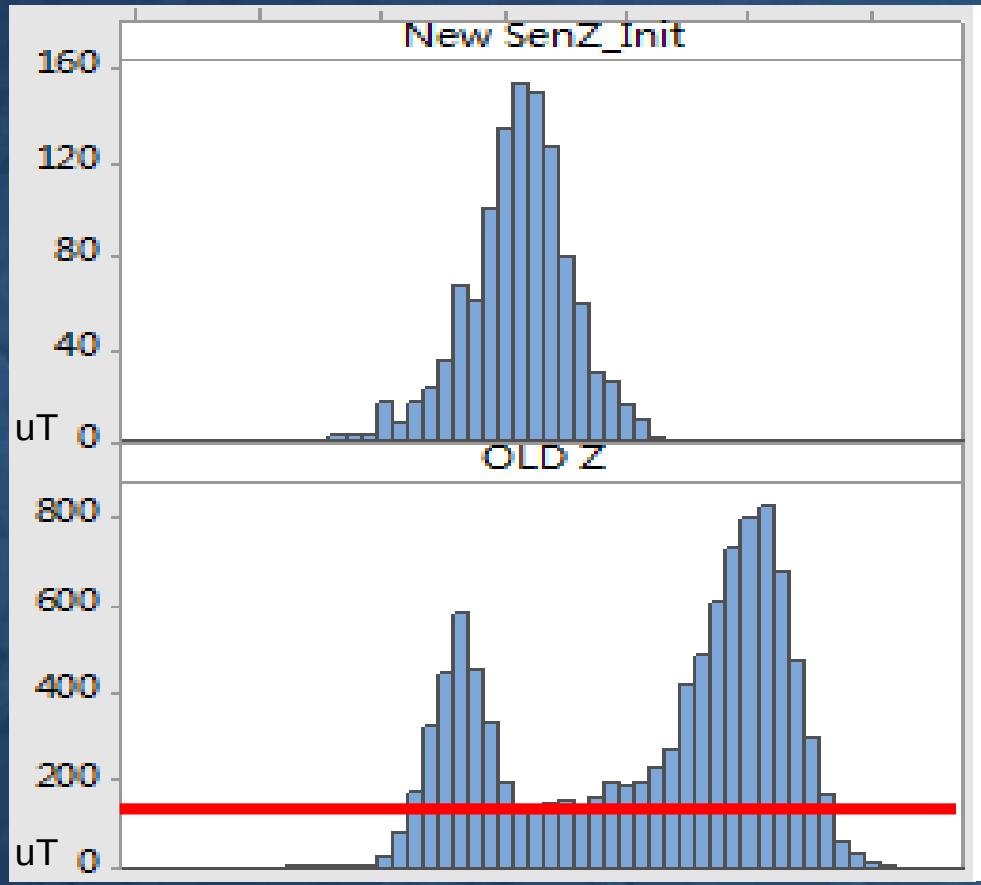
Design	Drawing	Approved	Scale	NTS
'14.05.29 M.SAKAGUCHI	'14.05.29 M.SAKAGUCHI	'14.05.29 K.ITOU	Units	mm

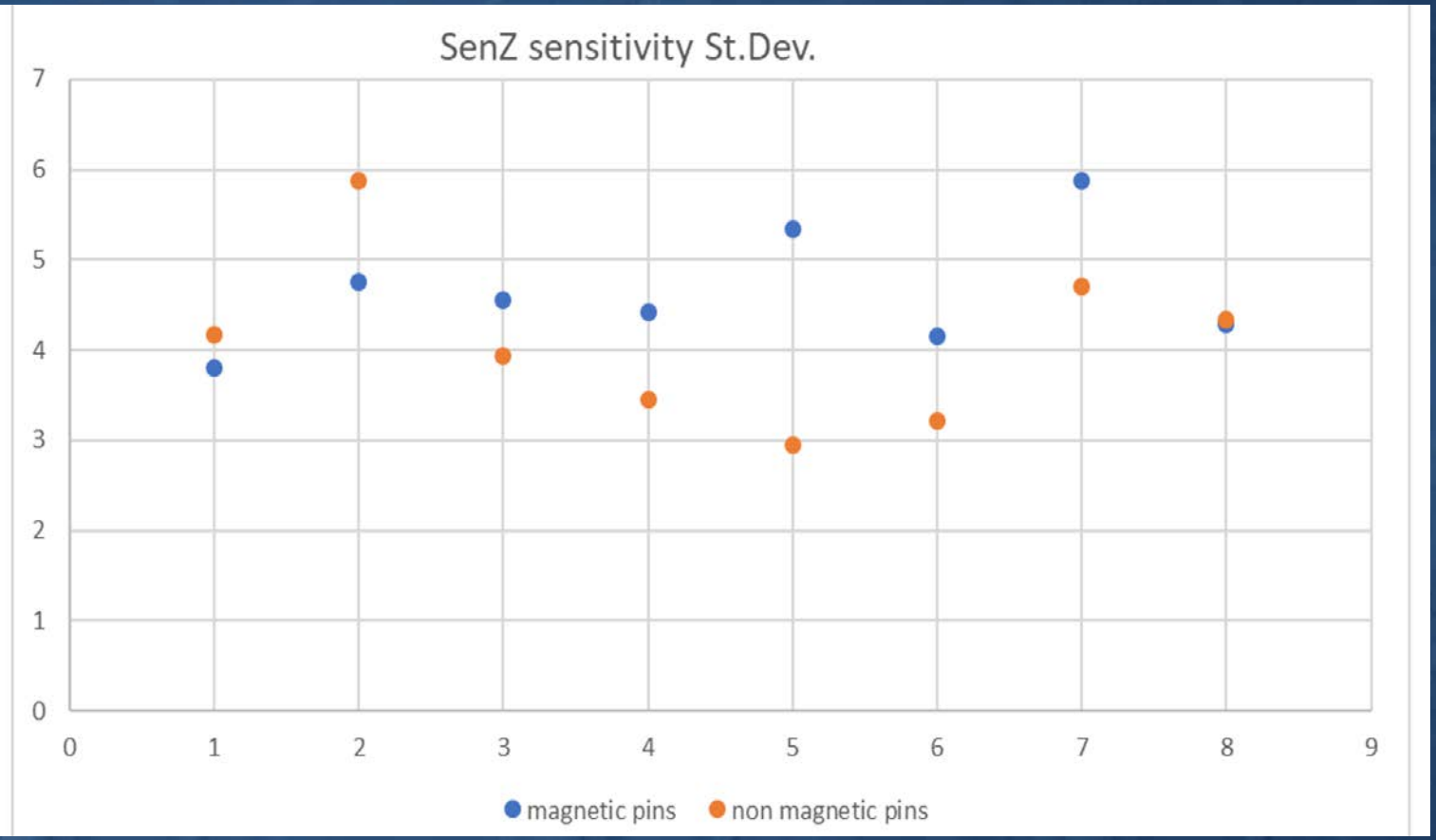
RIKA DENSHI CO.,LTD.

Courtesy Of Afore Oy - Stimulus Tester



Test Results – Sensitivity to Magnetizing

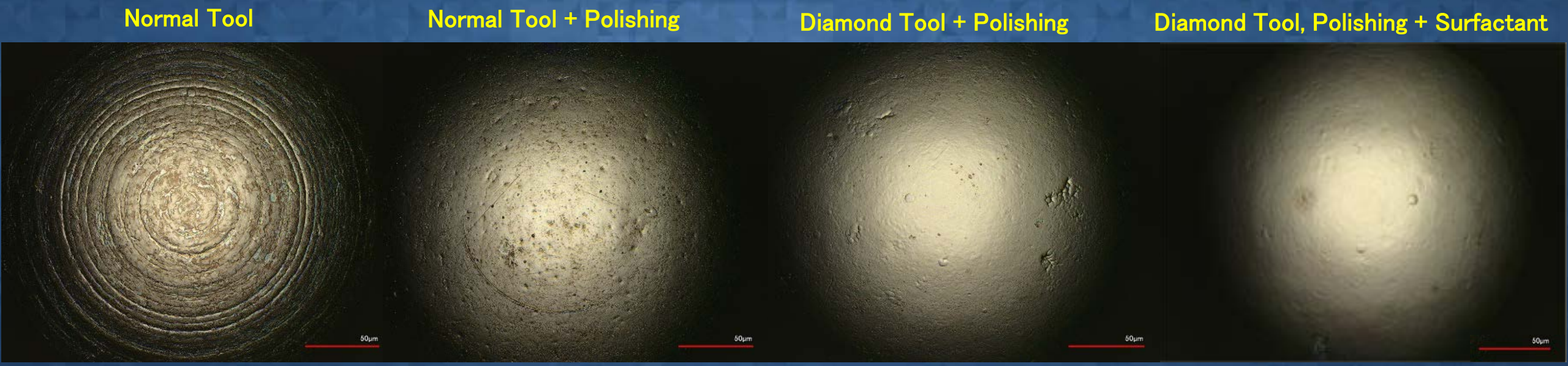




On Going Work

- **Surface uniformity may be a contributing factor to deviation in sensitivity to relative permeability results.**

  > Post processing of the probe barrels and plungers



On Going Work

- Location and geometries of the probed in an array may be a contributing factor to deviation in sensitivity to relative permeability results.

  > Pitch of the probes
  > Dimensions of the probes

- Direction of flux axis may be a contributing factor to deviation in sensitivity to relative permeability results.

  > X, Y axis magnetic flux direction = probe cross sectional area
  > Z axis magnetic flux direction = probe longitudinal area

- Additional experiments will be conducted by changing these parameters as well as with various spring materials for even lower relative permeability.

Thank You

- **Ari Kuukkala, Director of Sales**
  Afore Oy
  Lieto, Finland

- **Takahiro Okinaka, Director of R&D**
  Rika Denshi Group
  Kumamoto, Japan

- **Kohei Nakamura, Staff Engineer, Probe Designer**
  Rika Denshi USA
  Attleboro, Massachusetts USA

Welcome to the Sheraton, Hsinchu !

A New Framework to Measure Interface Complexity

Steve Ledford
Teradyne

TERADYNE

Hsinchu, Taiwan, October 17-18, 2019

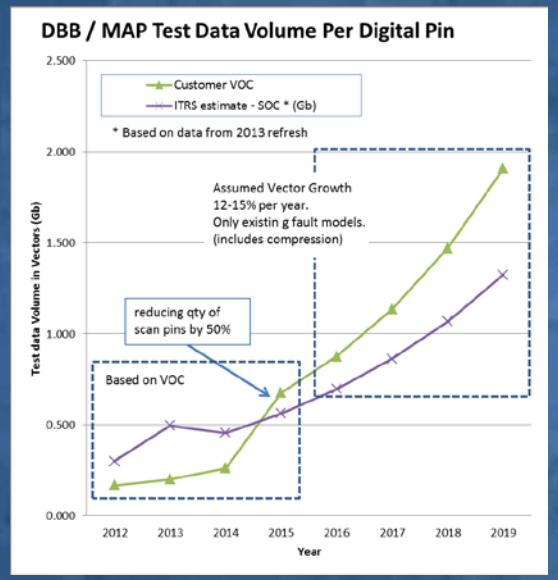
Outline

- **Industry Trends Impacting Probe**
  - Device Complexity
  - Convergence of technical performance & delivery on complexity
- **Interface Complexity: “2 x 4 scaling”**
  - Design & Manufacturing Complexity Scale: DMC Scale
  - Breaking down the DMC Scale
- **Complexity examples**
  - AP probe card vs AP final test
  - Two different construction for the same application

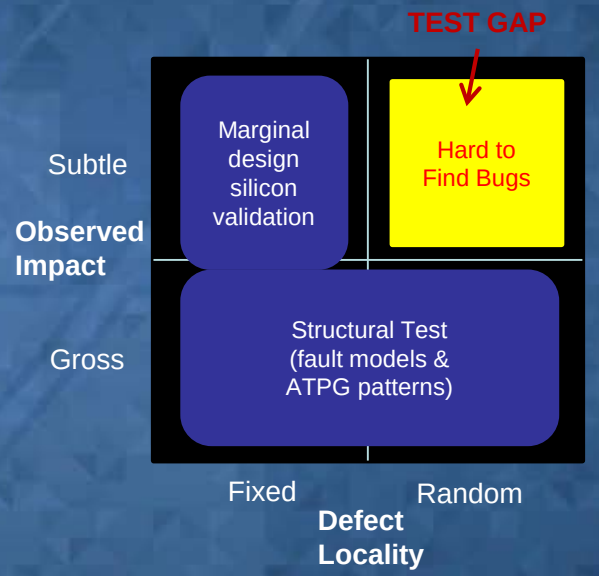
Device Complexity Impact on Test

Nanometer process nodes accelerating device complexity

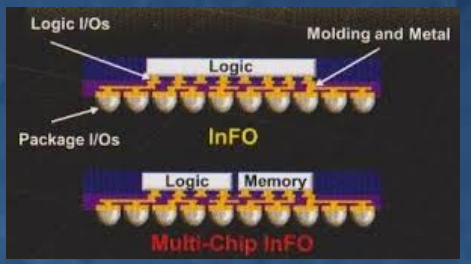
1. Test Cost:
ATE test time increase

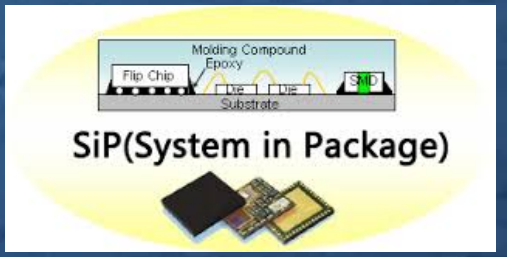


2. Device Quality:
ATE test coverage



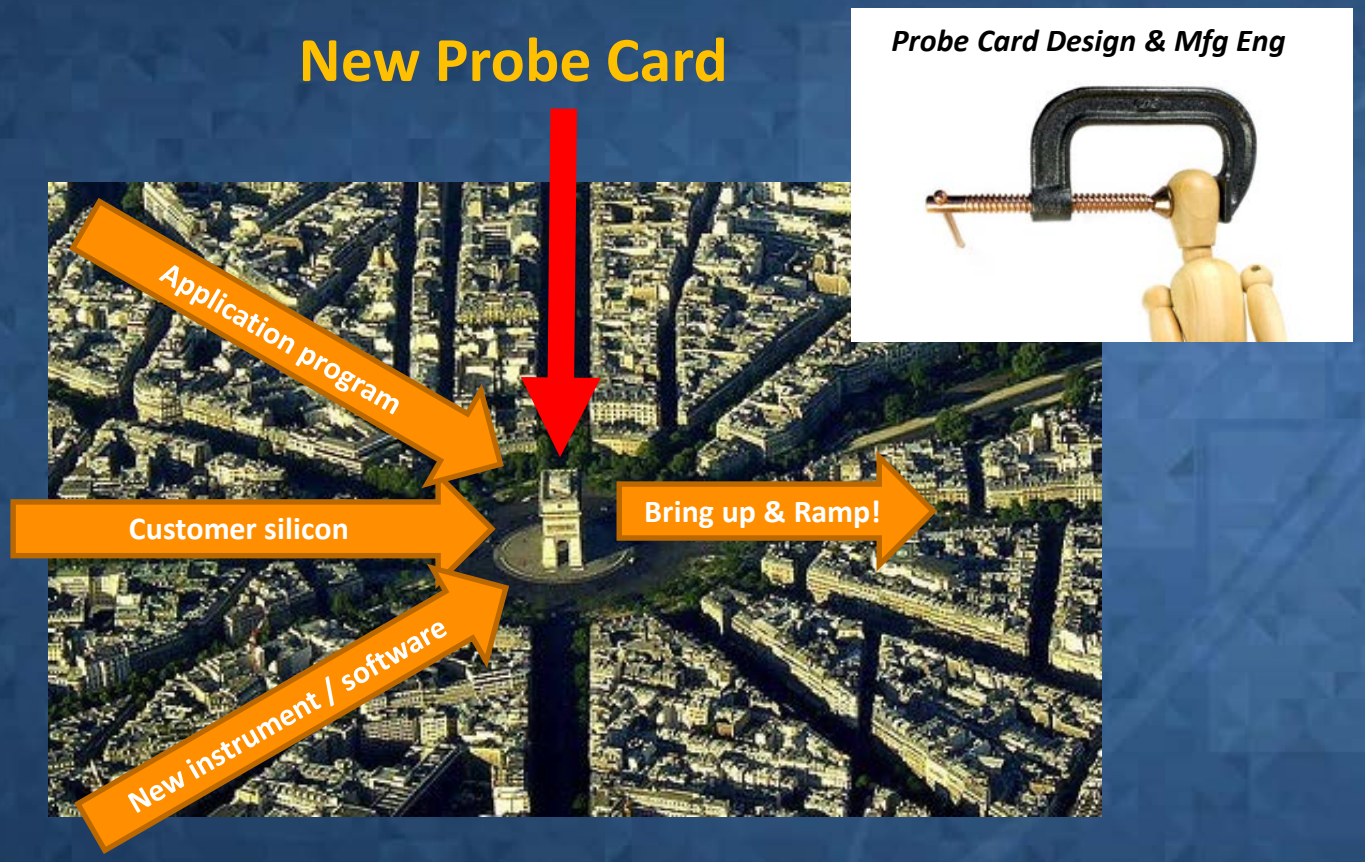
3. New Packaging:
Deemphasize final test





- **Increasing ATE test cost adds pressure for an alternative/complementary approach**
- **New package types and heterogeneous integration eliminate IP access at final test**

Complexity Challenges



To meet the customer technical performance requires:

- New materials
- New manufacturing processes

With:

- Tighter tolerance
- More requirements
- No margin for failure to deliver

On:

- A shorter timeline

Results in rapidly increasing complexity

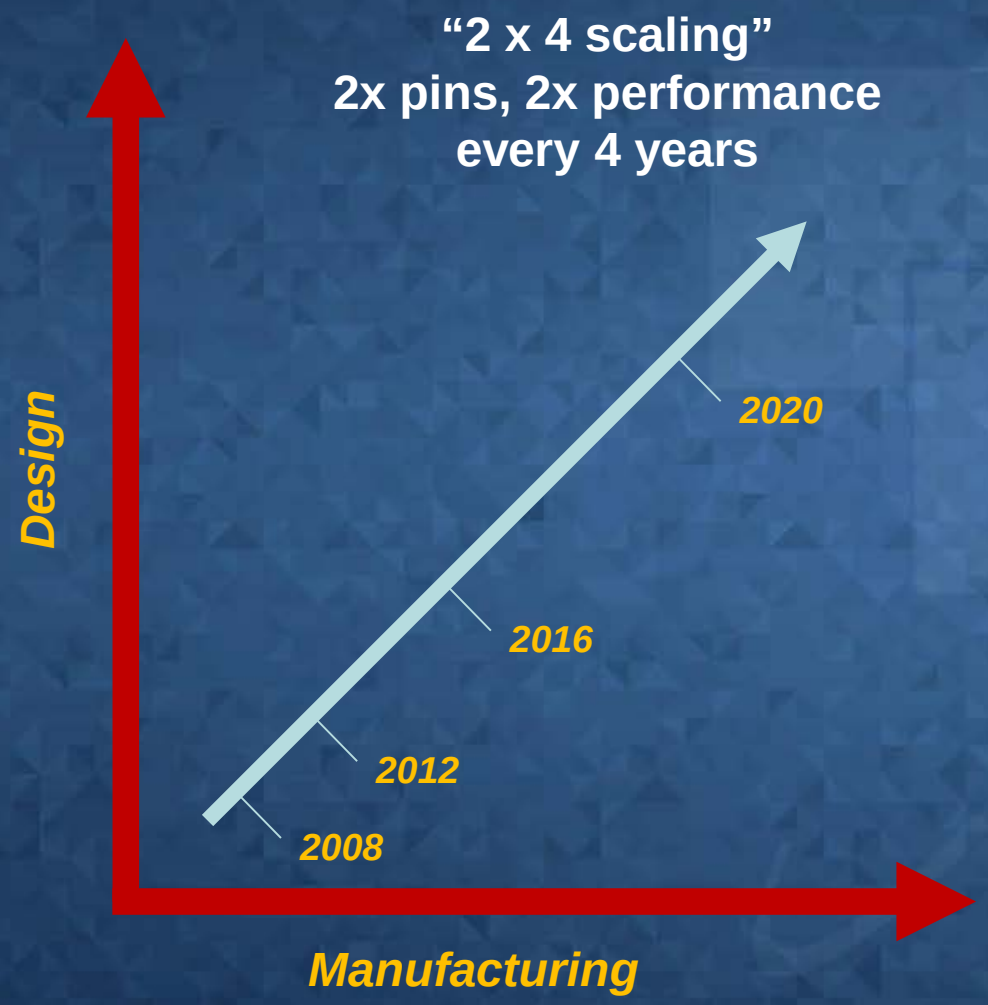
Interface Complexity – Attribute Interaction

- **Just because a design or fab can produce a single attribute, doesn't mean they can do all max capability attributes in combination for a single design.**

- **Human analogy**
  - How many miles can you run without stopping? -> 10 Km
  - How much weight can you lift above your head? -> 50 Kg
  - Can you whistle? -> Yes
  - ***Now, run 10 kilometers with 50 Kg above your head while whistling.***

- **Need a means to manage Interface design total attribute risk using an objective, fact based methodology**

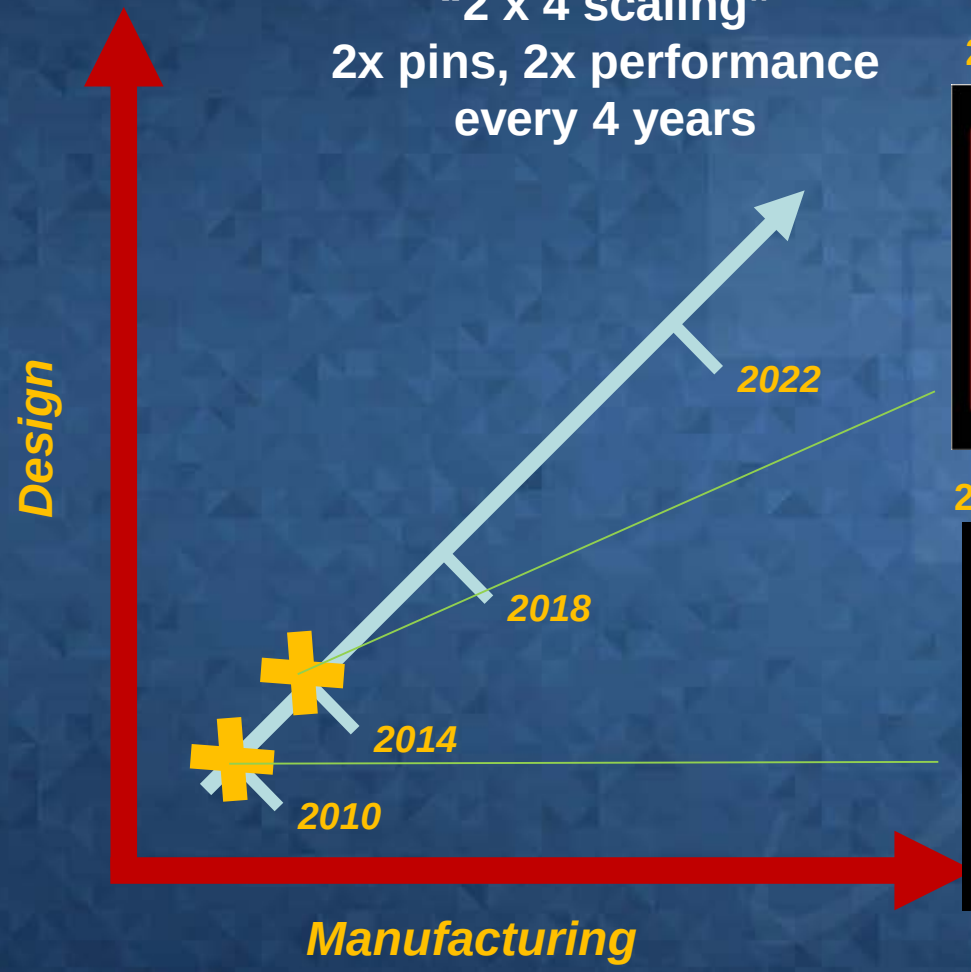
Design & Manufacturing Complexity Scale



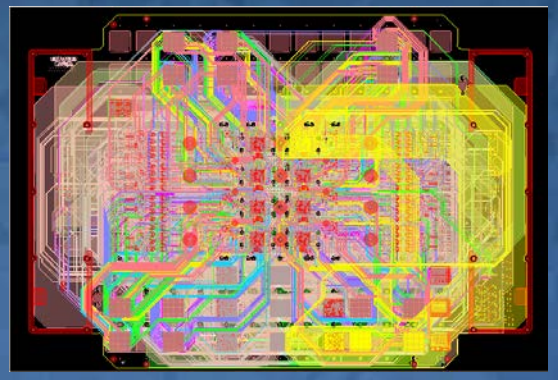
Interface Design & Manufacturing Complexity Scale objectives:

- Quantify the interface complexity
- Identify difficult combinations
- Contrast options and alternatives that achieve the best balanced outcome
- Develop risk mitigation options to:
  - Achieve reliable products
  - Deliver on-time

Design & Manufacturing Complexity Scale

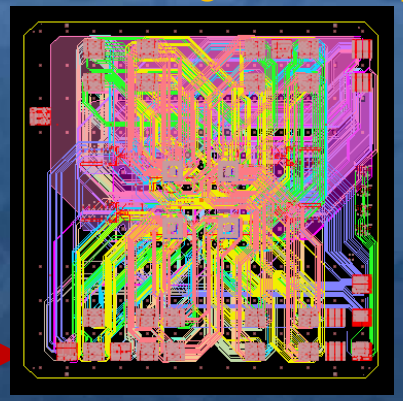


2014 - Design "B" 356 pin BGA x8



		Increase:
Site count:	8 sites	2x
Layers:	54 layers	1.9x
Filled vias:	~15,000	5x
Panel Size:	15.9" x 22.6"	1.5x
Total Components:	2,972	7.8x
Connection Points:	10,766	2.3x

2010 - Design "A" 324 pin PBGA x4



Site count:	4 sites
Layers:	28 layers
Filled vias:	~3,000
Panel Size:	15.9" x 15.9"
Total Components:	385
Connection Points:	4,707

Interface Complexity: “2 x 4 scaling”

Emerging paradigm: “It is a complex system problem at the test cell level”

- **Engineer the full path taking into account everything from Instrument to DUT contact**
- **Sustainable pin scaling curve: “2 x 4 scaling” – 2x pins, 2x performance every 4 years**

		2018 (today)	2028 (future)
Pin density	The number of DUT sites and DUT pin count in the same or smaller area drive up the pin area density. **Challenge**: Routing out the signals to the instruments and power supplies becomes increasingly difficult.	4,000 I/O per sq in 80um C4 pitch	16,000 I/O per sq in 40 um C4 pitch
I/O Performance	Increased challenges with high speed I/O (PCIe, DDR Interfaces, mmWave) to support BW intensive end products. **Challenge**: Increasing test standards (signal integrity, eye opening) including safety to insure quality for the end applications.	32 Gbps (dig) 6 GHz (RF) 1 kVA (power)	128 Gbps (dig) +100 GHz (RF) 10 kVA (power)
Power Performance	Device Supplies < 700mV require excellent accuracy. Increasing power rails per DUT consumes high PCB layer count. **Challenge:** Increasing test standards (power impedance curve) to insure quality for the end applications.	4 power rails / layer @10% VDD droop	16 power rails / layer @5% VDD droop
Components	Application circuit complexity increases component count per DUT site. **Challenge:** Use of smaller foot print components make diagnosing and repairing defects increasingly difficult to detect and time consuming	70 comp per sq in 1st time BIN1: 50%	200 comp per sq in 1st time BIN1: +95%
Execution	Delivery of the device interface from pin-out freeze to wafer out for first probe contact with full performance **Challenge:** Increasing DI complexity increases effort & risk of design or mfg defects. Complex mfg processes take longer.	75% OTD 6 week leadtime	95% OTD 3 week leadtime

Since June 2018 SW Test:

New instrument introduction

- UltraSerial60G – high speed serial
- MX44 – 44 GHz 5G mmWave
- ETS 88TH & ETS 88UHV

New quality & diagnostic tools deployed to eliminate assembly and mechanical defects

Leadtime reduction by optimized CAM / release process

Design Complexity

Leveraging design complexity models used for IC design:

$$Di = \frac{1}{\rho} \times \sum_{i=0}^{n} (wk \times Sk)$$

Where:

- **Di = Design Index**
- **w_k= weighting factor**
- **S_k = attribute difficulty (see table)**
- **ρ = Design team proficiency**

1	Board / MLO Outer dimensions
2	Total wiring requirements – traces and shapes
3	Layer count
4	Active component count
5	Passive component count (2 lead capacity / resistor)
6	Relay component count
7	Pin density – Application / DUT area
8	Digital data rate – high speed serial or digital bus (DDR)
9	RF/mmWave – carrier frequency
10	Power integrity – highest frequency for PDN optimization

Assembly Complexity

Agilent (now Keysight) introduced an Assembly complexity index[1]:

Ci = ((#C + #J)/100)) * D * M

Complexity type	Complexity index
Low complexity	< 25
Medium complexity	>= 25 and < 75
High complexity	>= 75

Where:

- **Ci = Complexity Index**
- **#C = Number components**
- **#J = Number of joints**
- **D = Double sided D = 1 and Single sided D = 0.5**
- **M = High Mix M = 1 for high mix and M = 0.5 for low mix.**

Yield = [1 – (DPMO / 1E6)]^{N}

Where:

- **DPMO is Defects Per Million Opportunities**
- **N = Defect Opportunities**

[1] A NEW TEST STRATEGY FOR COMPLEX PRINTED CIRCUIT BOARD ASSEMBLIES. Stig Oresjo, Agilent Technologies, Inc.

Fab Complexity

Based on the observations that attributes interact with each other to create complexity, this is best represented as a weighted matrix:

$$Mi = \sum_{i=0}^{m} \left(\begin{bmatrix} a_{11} & \cdots & a_{1n} \\ \vdots & \ddots & \vdots \\ a_{m1} & \cdots & a_{mn} \end{bmatrix} \times \begin{bmatrix} S_1 \\ S_2 \\ S_m \end{bmatrix} \right)$$

Where:

Mi = Manufacturing Index

a_{mn} = Interactive attribute weight

S_m = Category difficulty

PCB Complexity	Registration	Mechanical drill - 4 mil	Mechanical drill - 5 mil	Mechanical drill - 5.9 mil	Mechanical drill - 8 mil	Mechanical drill - 10 mil	Microvia	Mechanical	Impedance control	Category difficulty	Interactive Complexity
Registration	1	2	1.7	1.3	1	0.8	2	0.5			0
Mechanical drill - 4 mil		2									0
Mechanical drill - 5 mil			1.8								0
Mechanical drill - 5.9 mil				1.5							0
Mechanical drill - 8 mil					1						0
Mechanical drill - 10 mil						0.7					0
Microvia							2				0
Mechanical								1			0
Impedance control									1		0
Interactive Complexity											**0**
										Total Complexity	

Fab Complexity

Each Category of a PCB complexity is it's own matrix of interactions that then "rolls up" to the PCB complexity matrix:

$$Ri = \sum_{i=0}^{m} \left(\begin{bmatrix} w_{11} & \cdots & w_{1n} \\ \vdots & \ddots & \vdots \\ w_{m1} & \cdots & w_{mn} \end{bmatrix} \times \begin{bmatrix} A_1 \\ A_2 \\ A_m \end{bmatrix} \right)$$

Where:

- **Ri = Registration Index**
- **w_{mn} = Interactive attribute weight**
- **A_m = Single attribute difficulty**

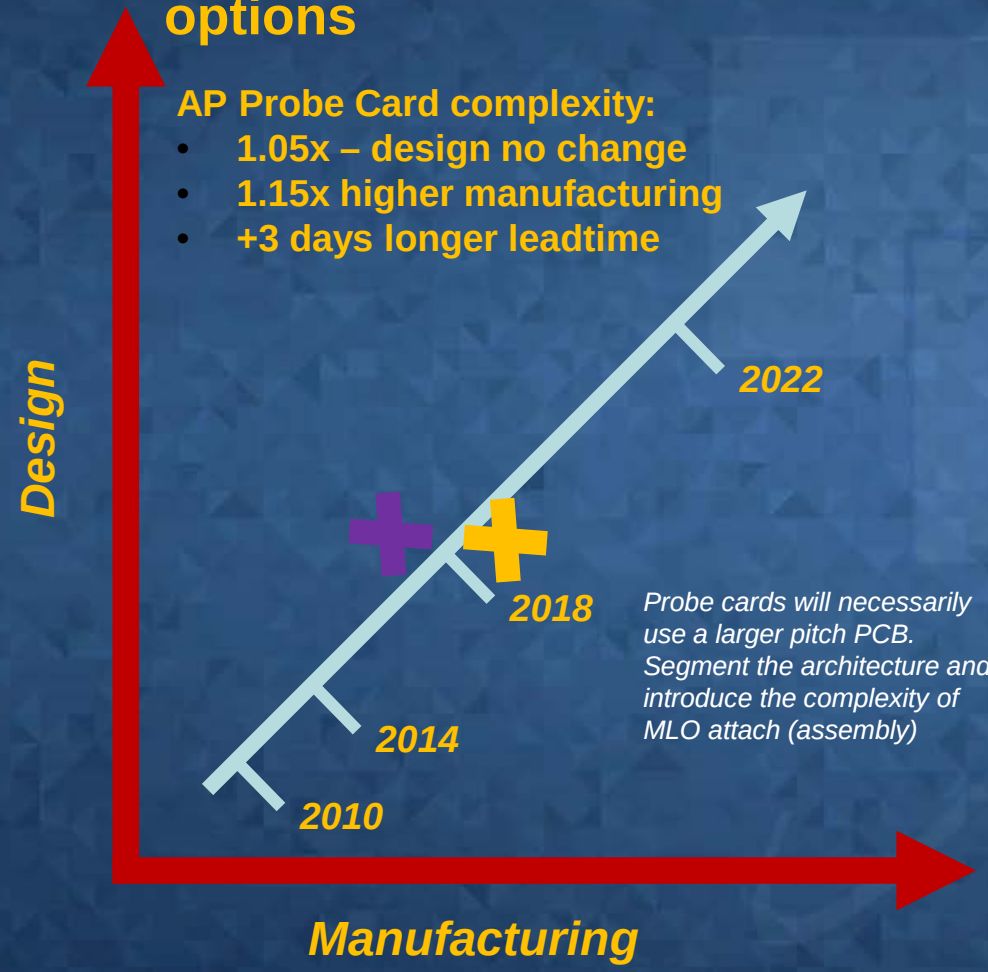
Registration	Board Size	Total Layer count	Drill to trace spacing - min	Materials - Basic (eg, FR408HR)	Materials - Advanced (eg, Meg6)	Materials - Exotic (eg, Rogers)	Dielectric thickness	Balanced Stackup		Project Value	Attribute difficulty	Interactive Complexity
Board Size	2	1		0.5	1	2	1.5	1.5				0
Total Layer count		2		0.5	1	2						0
Drill to trace spacing - min			2		1	2						0
Materials - Basic (eg, FR408HR)				0.5	2	4						0
Materials - Advanced (eg, Meg6)					1	3						0
Materials - Exotic (eg, Rogers)						2	2	2				0
Dielectric thickness							2					0
Balanced Stackup								1				0
Interactive Complexity												**0**
												Total Complexity

DMC Scale: Examples

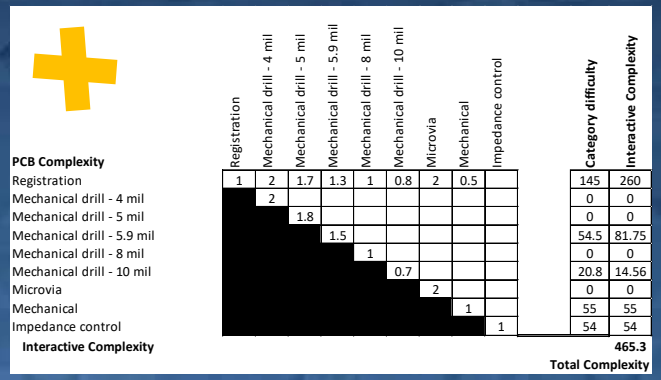
Compare similar application but different designs & manufacturing options

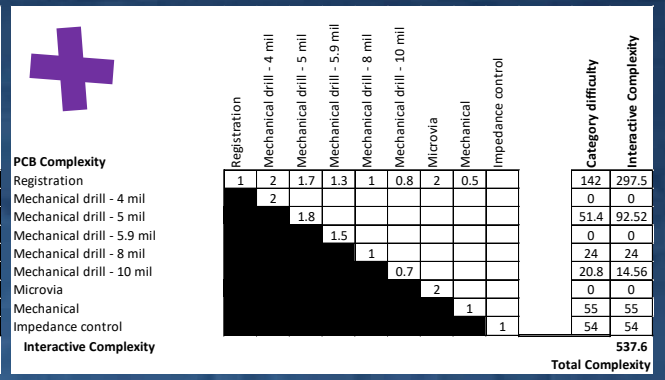
AP Probe Card complexity:

- **1.05x – design no change**
- **1.15x higher manufacturing**
- **+3 days longer leadtime**



Probe cards will necessarily use a larger pitch PCB. Segment the architecture and introduce the complexity of MLO attach (assembly)



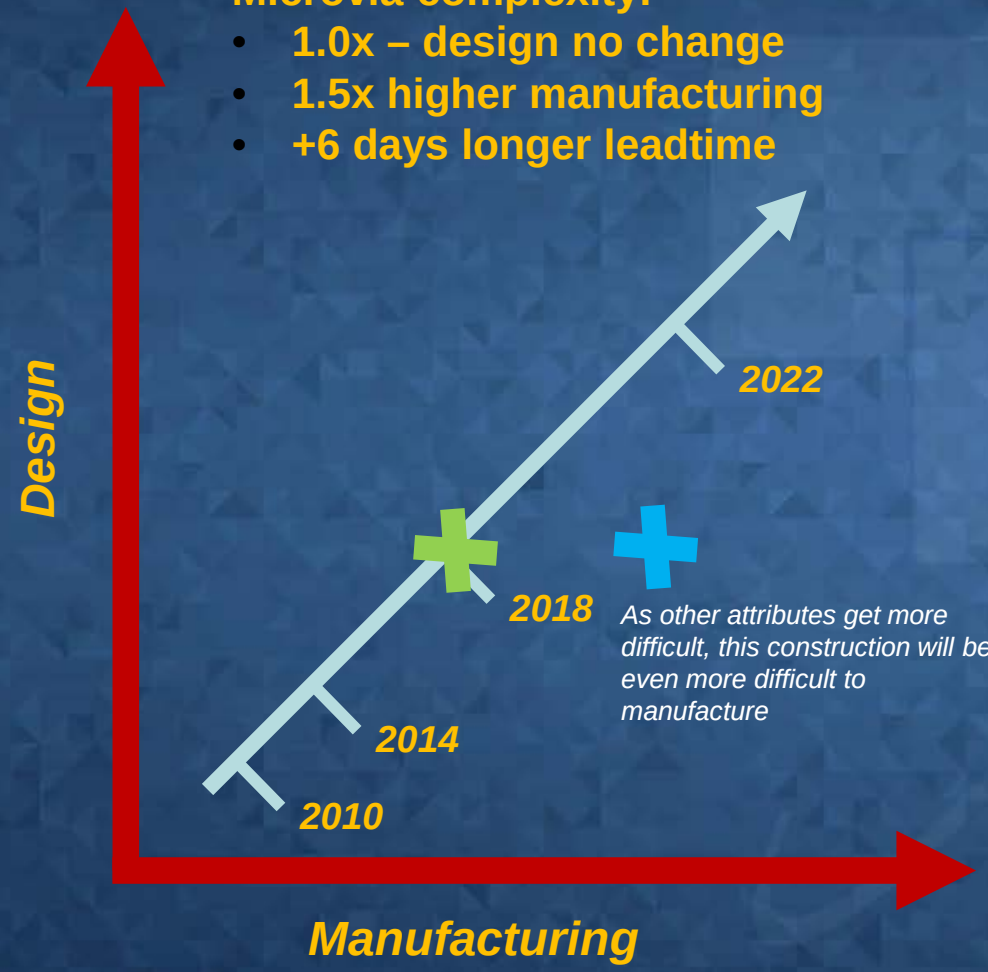


	AP Probe Card 8//	AP Final Test 16//
Board Size	16 x 16”	16 x 16”
Materials	Megtron 6	Megtron 6
Thickness	0.260”	0.250”
Layers	62	56
Pin Pitch (min)	0.5mm	0.4mm
Drill (min)	5.9 mil (PTH)	5.0 mil (BVH)
Aspect Ratio	44 : 1	30 : 1
Laminations	1	2
Components	7,700	5,772
Body size	0201	0201
Trace density	30,050	43,956
Flatness	+/- 1 mil (DUT area)	3 mils / in
Design Complexity	2842	2956
Mfg Complexity	465 (Fab) + 351 (Assy)	537 (Fab) + 173 (Assy)

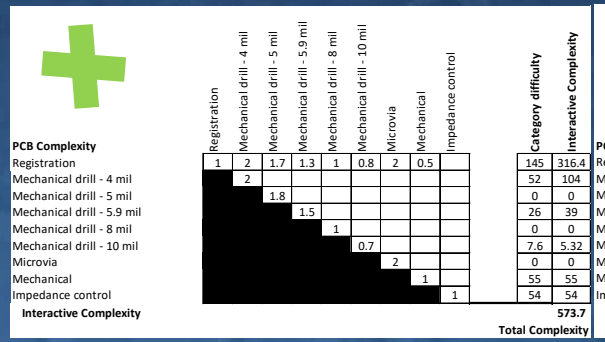
DMC Scale: Tradeoffs

Microvia complexity:

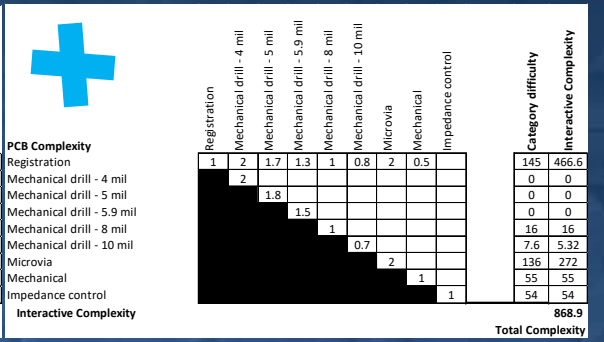
- **1.0x – design no change**
- **1.5x higher manufacturing**
- **+6 days longer leadtime**



As other attributes get more difficult, this construction will be even more difficult to manufacture



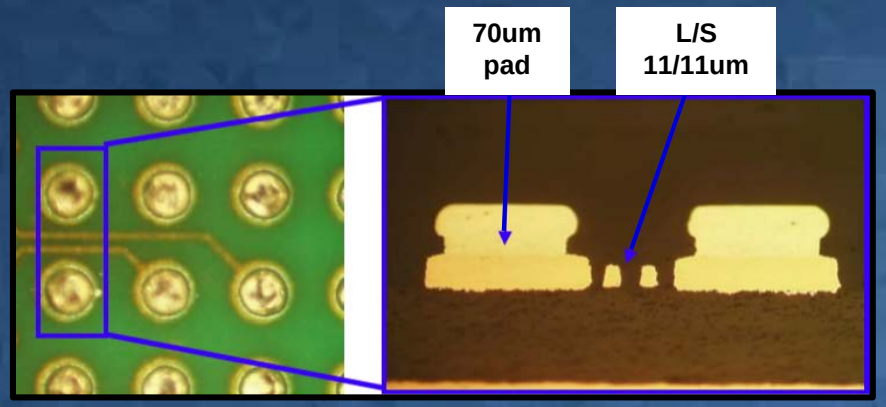
PCB Complexity	Registration	Mechanical drill - 4 mil	Mechanical drill - 5 mil	Mechanical drill - 5.9 mil	Mechanical drill - 8 mil	Mechanical drill - 10 mil	Microvia	Mechanical	Impedance control	Category difficulty	Interactive Complexity
Registration	1	2	1.7	1.3	1	0.8	2	0.5		145	316.4
Mechanical drill - 4 mil		2								52	104
Mechanical drill - 5 mil			1.8							0	0
Mechanical drill - 5.9 mil				1.5						26	39
Mechanical drill - 8 mil					1					0	0
Mechanical drill - 10 mil						0.7				7.6	5.32
Microvia							2			0	0
Mechanical								1		55	55
Impedance control									1	54	54
Interactive Complexity										573.7	
										Total Complexity	



PCB Complexity	Registration	Mechanical drill - 4 mil	Mechanical drill - 5 mil	Mechanical drill - 5.9 mil	Mechanical drill - 8 mil	Mechanical drill - 10 mil	Microvia	Mechanical	Impedance control	Category difficulty	Interactive Complexity
Registration	1	2	1.7	1.3	1	0.8	2	0.5		145	466.6
Mechanical drill - 4 mil		2								0	0
Mechanical drill - 5 mil			1.8							0	0
Mechanical drill - 5.9 mil				1.5						0	0
Mechanical drill - 8 mil					1					16	16
Mechanical drill - 10 mil						0.7				7.6	5.32
Microvia							2			136	272
Mechanical								1		55	55
Impedance control									1	54	54
Interactive Complexity										868.9	
										Total Complexity	

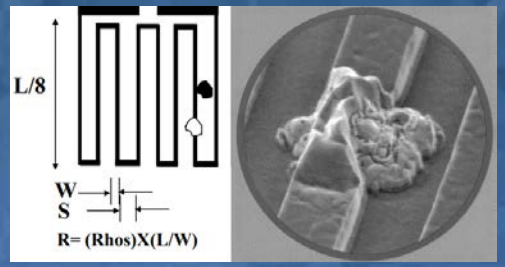
	Option “A”	Option “B”
Board Size	16 x 16”	16 x 16”
Materials	Megtron 6	Megtron 6
Thickness	0.250”	0.250”
Layers	62	60
Pin Pitch (min)	0.35mm	0.35mm
Drill (min)	4.0 mil (BVH)	8 mil (PTH)
Microvia	None	3 layers
Laminations	2	4
Trace density	23,000	24,000
Flatness	+/- 1 mil (DUT area)	+/- 1 mil (DUT area)
Design Complexity	2612	2680
Mfg Complexity	573	869
Mfg Leadtime	15 days	21 days

Complexity: Capabilities Needed



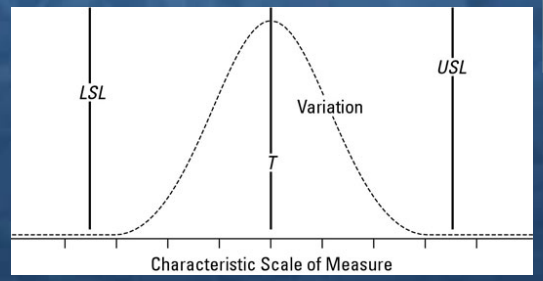
- **Fine pitch DUT area routing escape is an enabler to increase I/O density**
- **Smaller line / space enables more than one signal to escape on a single layer requiring fewer total layers**
- **As pin pitch decreases the L/S becomes smaller, requiring sub-micron scale process capability and control**

Defect Density
Size and frequency of a random defect that can cause a short / open



- **Cleanliness is a function of all critical inputs: people, process, tools.**
  - Requires a wholistic yield management system.
- **Characterization & testing is required to set process targets and drive continuous improvement**
  - DIB TTM & quality standards don't allow experimentation on a live project
- **To achieve a viable yield**
  - < 0.1 defects / DIB @ 400x400mm
  - A 10um process requires Class 100

Process Capability
The ability of a process to produce output within specification limits



- **For a 11/11um L/S feature, to maintain impedance control:**
  - +/- 5% = +/- 2.5um
  - To meet a Cpk of 1.67 requires measured std deviation of *0.5um!*
- **L/S control is the outcome of process capability of photo & etch**
  - Since the processes are sequential the individual process capability must be even better!

SWTEST ASIA 2019

Intelligent Method for Retesting a Wafer

TESLENCE
Achieve Test Excellence

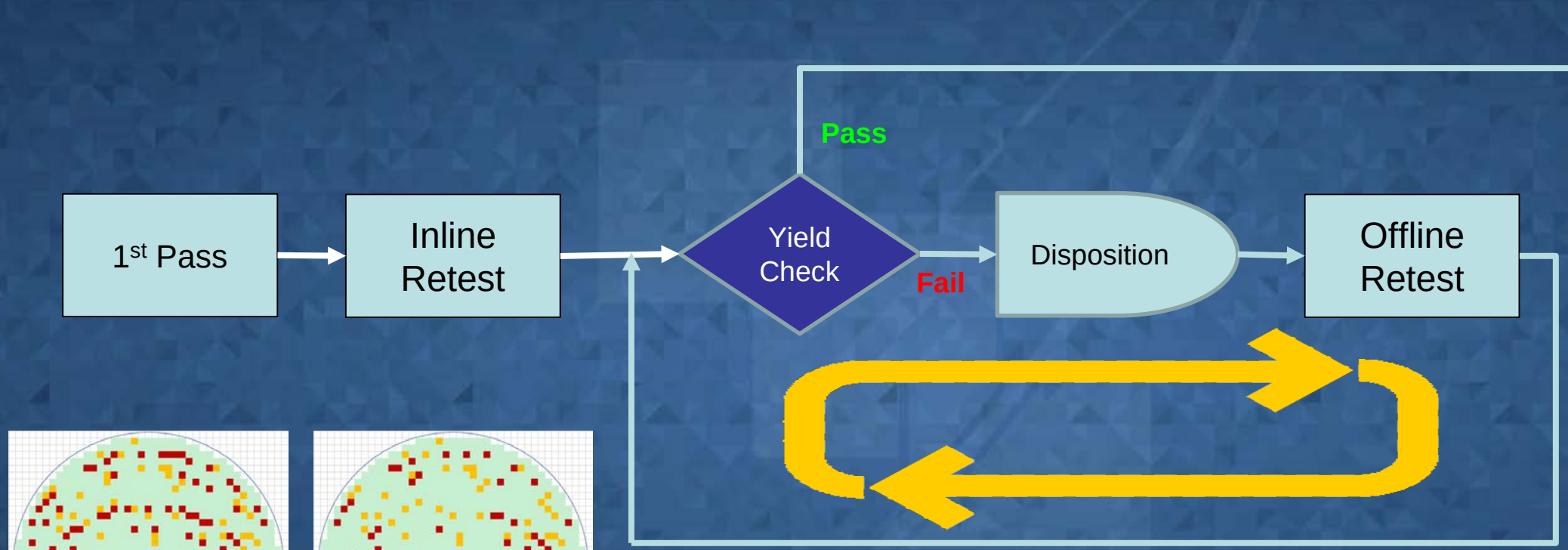
YC Wang / YK Huang
Teslence Technology Co., Ltd

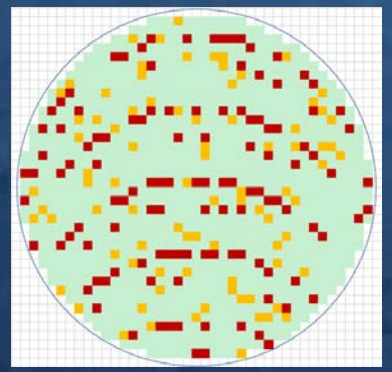
Hsinchu, Taiwan, October 17-18, 2019

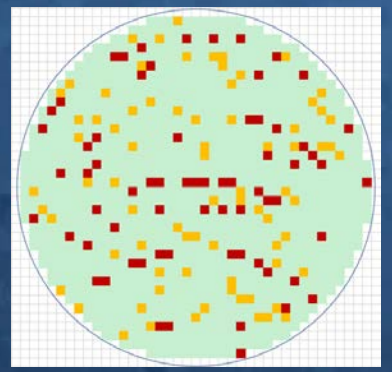
Overview

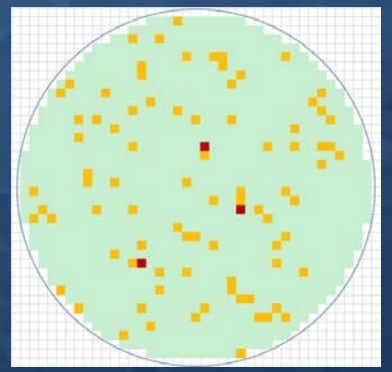
- Probe Production Issues
- Concept of an intelligent retest
- Methodology
- Result analysis
- Other capability
- Summary

Probe Production Flow









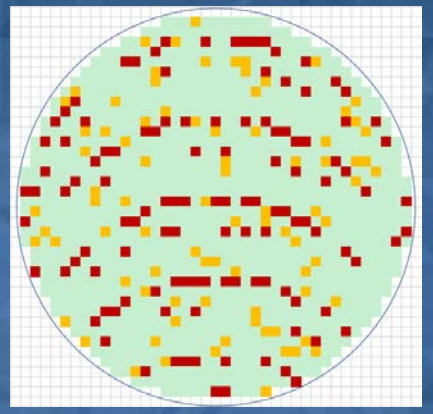
- **How long would it take to get yield right?**

What happened?

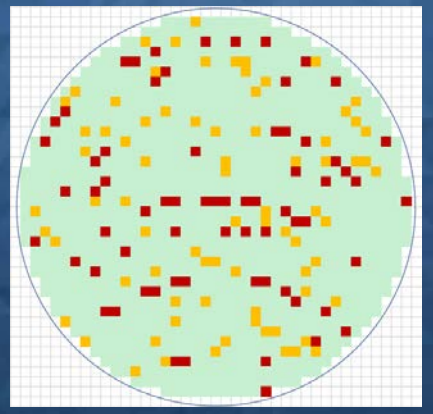
- **Low site to site yield from first pass to inline retest**

Site	FirstPass	Inline Retest
All	82.63%	87.60%
0	91.93%	91.93%
1	92.45%	92.45%
2	37.25%	62.75%
3	96.03%	96.03%
4	89.66%	89.66%
5	72.41%	85.52%
6	92.19%	92.19%
7	91.34%	91.34%

First Pass:



Inline Retest:

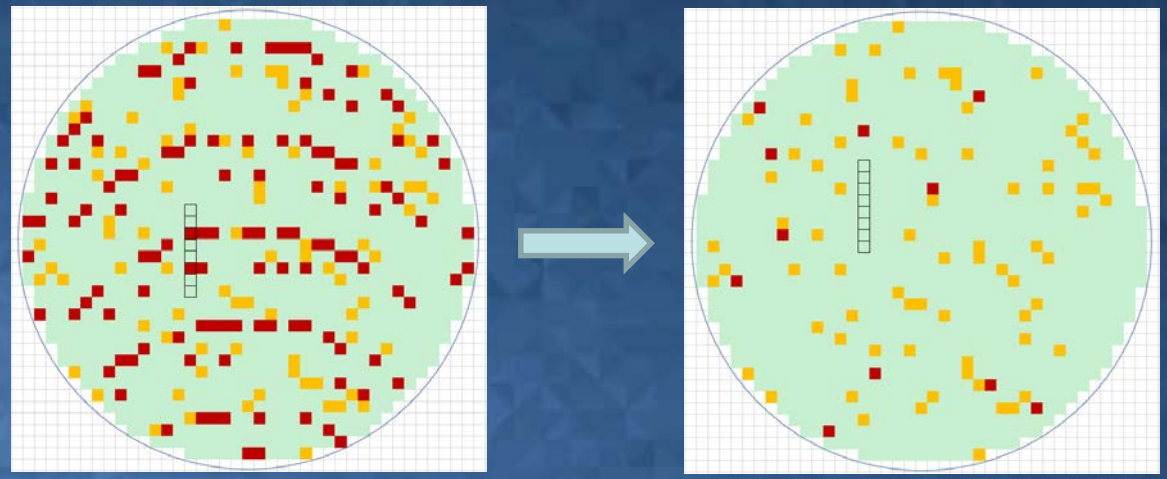


- **Probe head?**
- **Tester?**
- **Prober?**
- **Program?**
- **Probe Card?**
- **PIB?**
- **Docking?**
- **Alignment?**

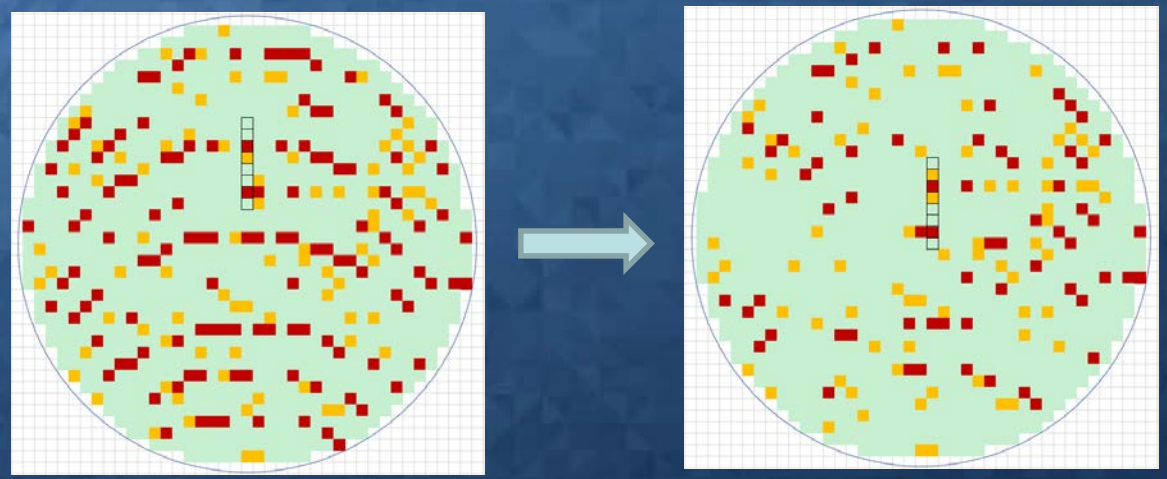
Current way to improve

- **Blind shift site reprobe on prober**
  - Pre-defined 2nd step map
  - Fixed shift site location
- **Cons:**
  - Need to setup for each device
  - Wafer stepping optimization lost
  - Performance may differ base on low yield site locations

Non-overlapping: Low Yield S2 & S5, retested with S6 & S0

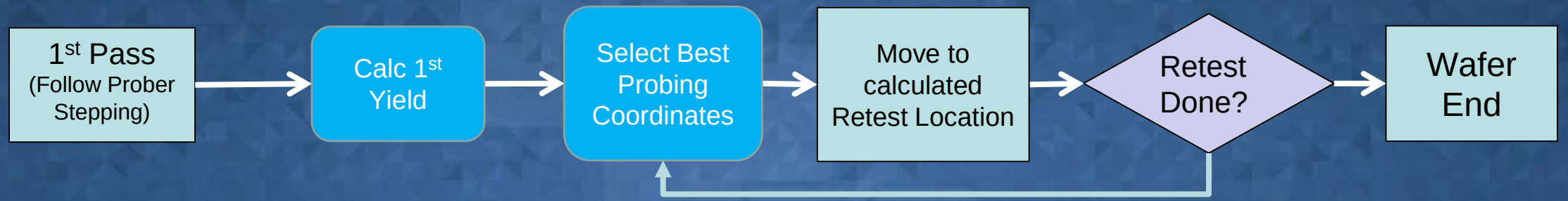


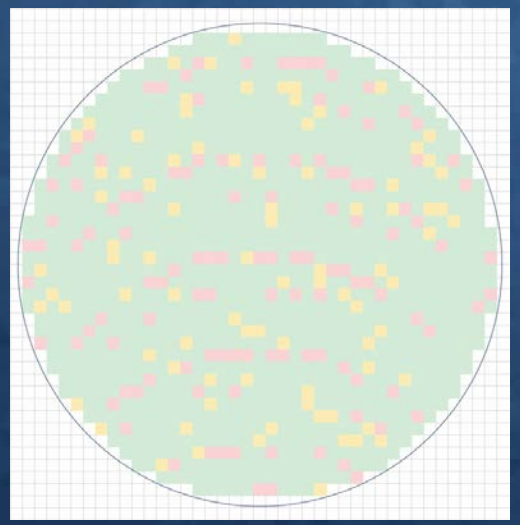
Overlapping: Low Yield S2 & S6, retested with S6 & S2



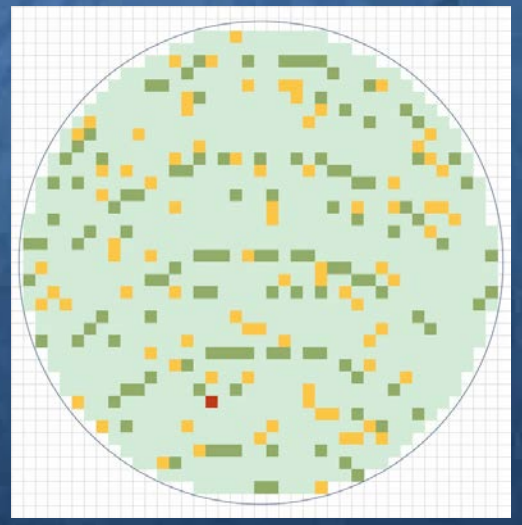
Or… Intelligent Reprobe

- **We called xREPROBE, use best yielding sites**
- **Patented : TW I639846 ; Pending in US and others**





	FirstPass
Yield	82.63%
Site 0	91.93%
Site 1	92.45%
Site 2	37.25%
Site 3	96.03%
Site 4	89.66%
Site 5	72.41%
Site 6	92.19%
Site 7	91.34%



Methodology

1st step: Optimize for retest time

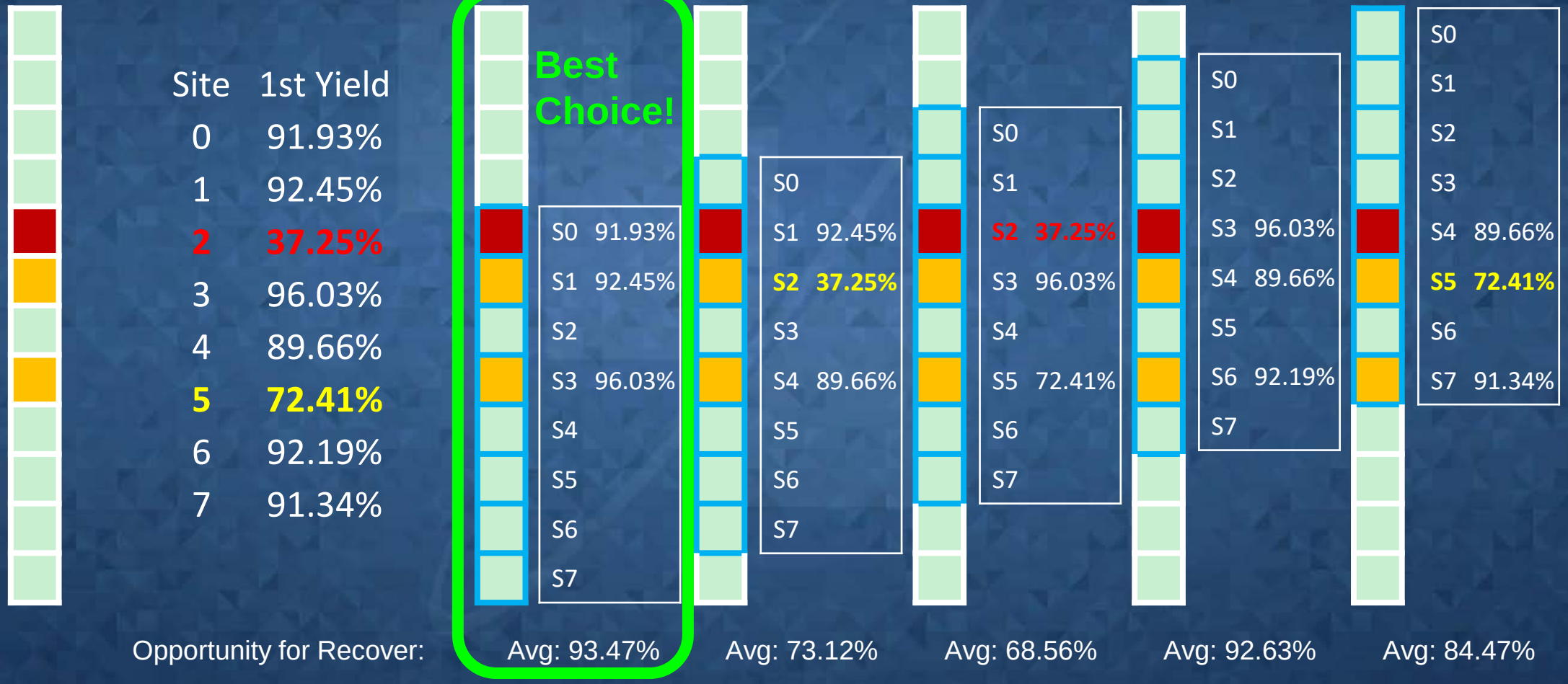
- Find location to test as many as rejects as possible
- Among the possible shifts, pick the best sites to retest

2nd step: Optimize for retest yield

- If chances to recover are low, look for other shift testing fewer rejects
- Rules include:
  - Possible recovery yield control
  - Retested with bad site

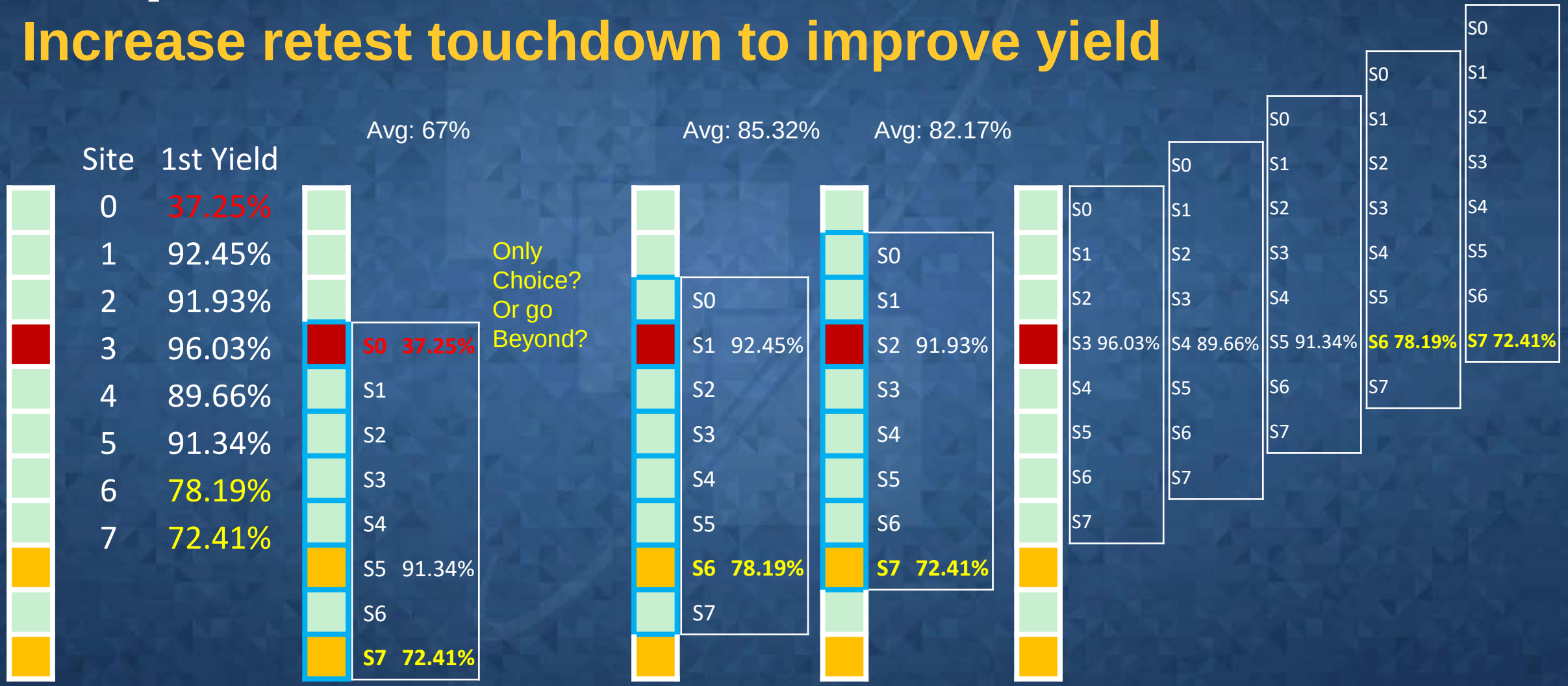
How We Decide?
Optimize Retest Time

- **Options we have for retest on example (1x8 PH), to test all rejects**



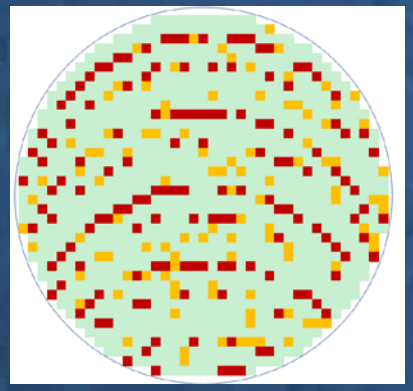
How We Decide?
Optimize Retest Yield

- **Increase retest touchdown to improve yield**



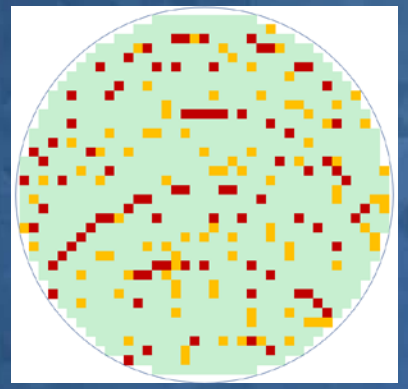
Result Comparison – Low Yield on none overlap sites

First Pass

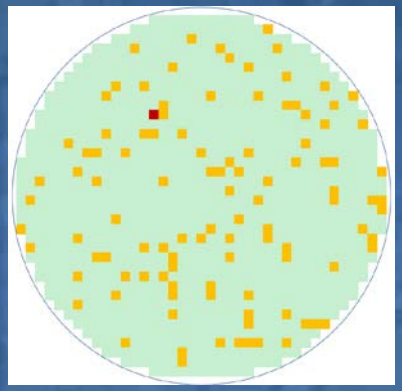


Retest Options

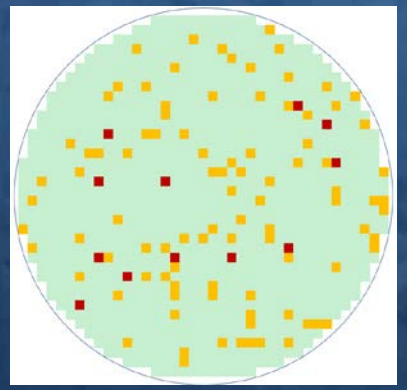
Traditional



xREPROBE



Blind Shift



xREPROBE vs Traditional:

Yield 6.08%↑

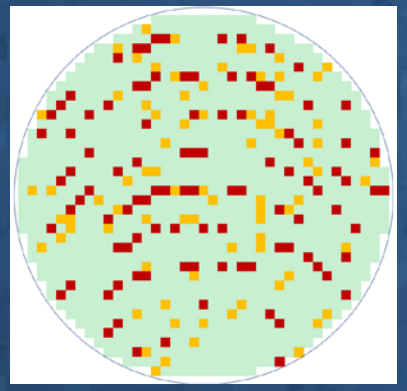
	FirstPass	Retest Options		
		Traditional	Blind Shift	xREPROBE
Yield	78.36%	84.77%	90.93%	90.85%
0	92.55%	12 ①	16	59
1	93.08%	11	62	80
2	26.80%	112	12	0
3	92.05%	12	16	47
4	88.97%	16	12	19
5	57.24%	62	11	3
6	90.63%	12	112	29
7	87.40%	16	12	16
TD	161	141②	160	128
RedCnt	147	85	12	1
RedPct	12.57%	7.27%	1.03%	0.09%

①: Number represents number of rejects tested
②: Number represents number of touch downs

Test Time 4.3%↓

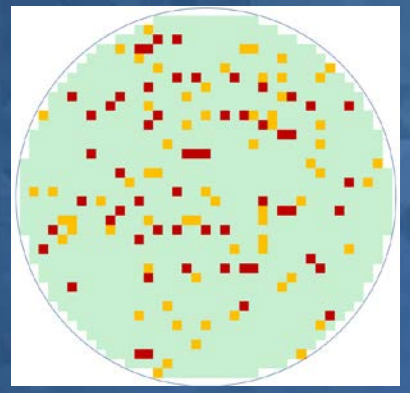
Result Comparison – Low Yield on overlap sites

First Pass

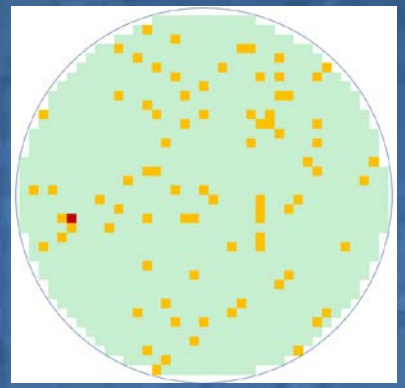


Retest Options

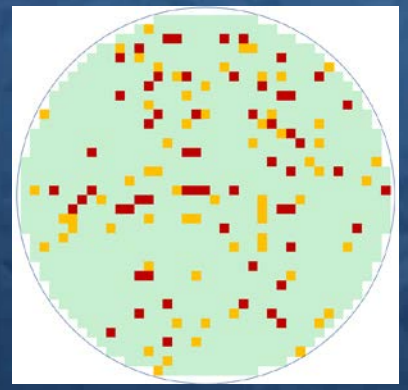
Traditional



xREPROBE



Blind Shift



xREPROBE vs Traditional:

Yield 3.6%↑

	FirstPass	Retest Options		
		Traditional	Blind Shift	xREPROBE
Yield	84.26%	89.39%	89.39%	92.99%
0	91.30%	14①	7	14
1	96.23%	6	8	83
2	53.59%	71	61	3
3	94.04%	9	8	11
4	95.17%	7	14	12
5	94.48%	8	6	38
6	52.34%	61	71	2
7	93.70%	8	9	21
TD	161	112②	121	99
RedCnt	102	57	59	1
RedPct	8.73%	4.88%	5.05%	0.09%

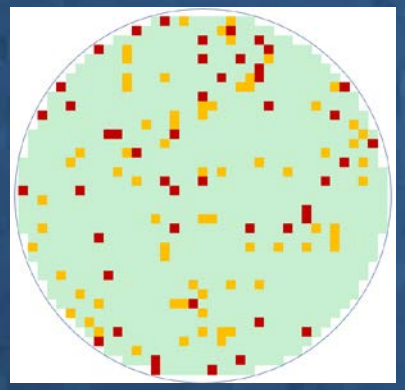
①: Number represents number of rejects tested
②: Number represents number of touch downs

Test Time 4.7%↓

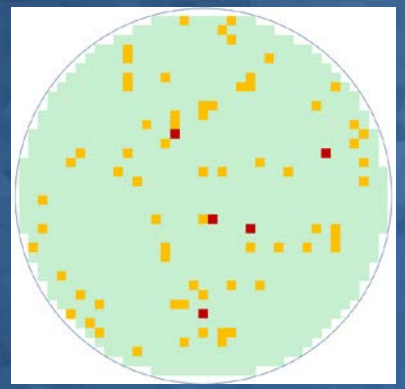
Result Comparison – Normal Yield Across Sites

Retest Options

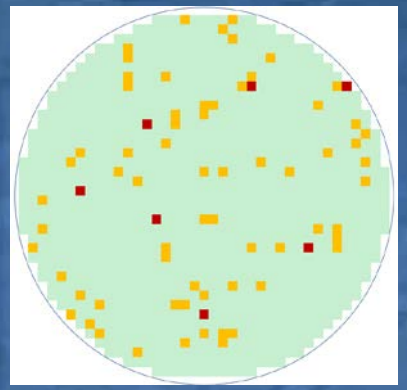
First Pass



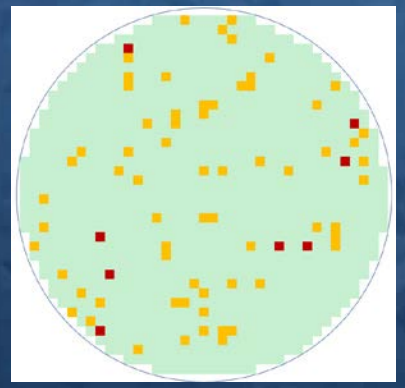
Traditional



xREPROBE



Blind Shift



	FirstPass	Retest Options		
		Traditional	Blind Shift	xREPROBE
Yield	89.91%	93.76%	93.67%	93.76%
0	88.20%	19	18	3
1	86.16%	22	15	4
2	89.54%	16	14	10
3	95.36%	7	7	56
4	87.59%	18	19	2
5	89.66%	15	22	8
6	89.06%	14	16	12
7	94.49%	7	7	23
TD	161	78	87	69
RedCnt	47	5	8	7
RedPct	4.02%	0.43%	0.68%	0.60%

①: Number represents number of rejects tested
②: Number represents number of touch downs

Test Time 3.8%↓

Result Comparison

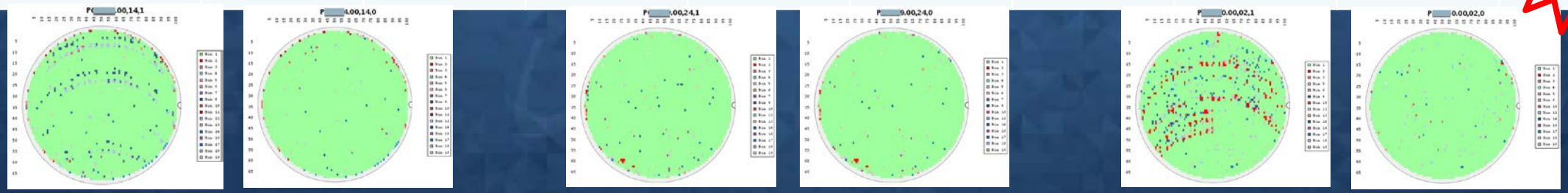
Retest Method	Traditional	Blind Shift Site	xREPROBE
Retest Yield	• Uses same site to retest • Worst recovery on site to site issue	• Recovery rate is hard to predict depending on low yield site location • Resulting in continued false fails from low yielding sites	• Best recovery yield with accurate binning
Retest Time	• Standard retest TD	• Increase of TD because change site away from optimized stepping • Retest time increased due to increase of TD	• Optimized and use fewest TD to retest • Calculated for each wafer so every retest is optimized

Case I:
C customer with 16 site setup, high retest rate due to setup

Result on 16 sites

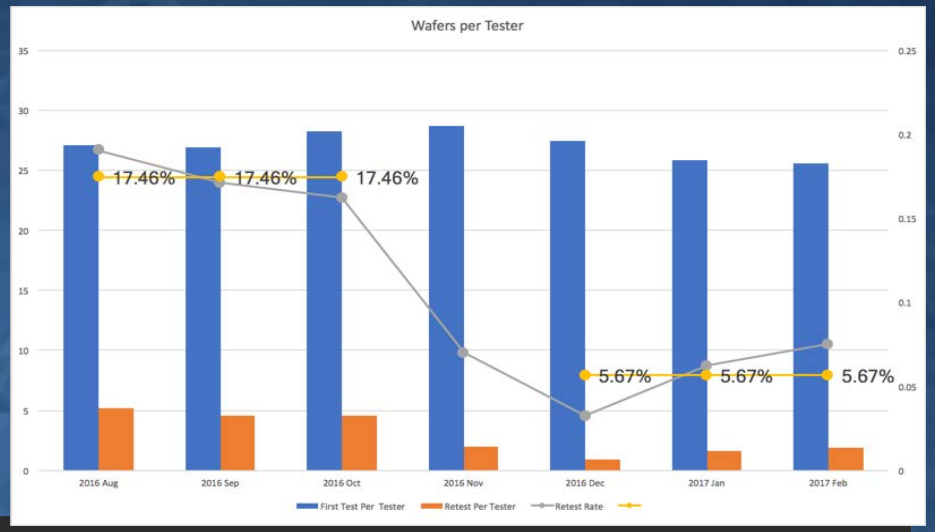
- **Ran 3 wafers to review results**
- **Saved 2% on test time and wafer show no sign of site to site fail pattern after retest**

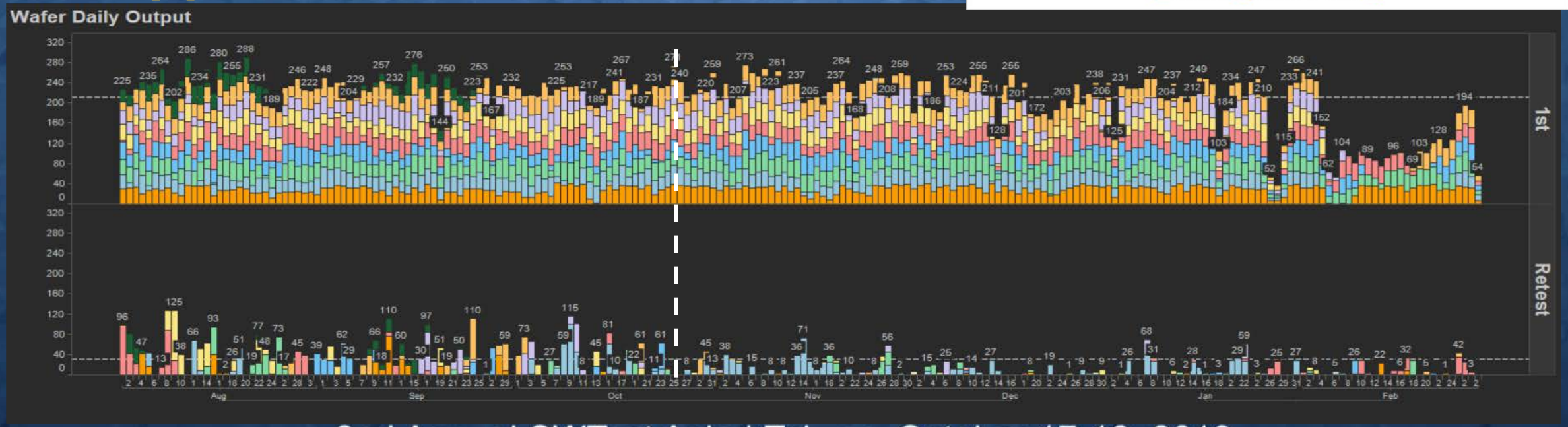
Wafers	First Yld	Final Yld	Total TD	Traditional Rsc TD	xREPROBE Rsc TD	Rsc % Save	Traditional Total TD	xREPROBE Total TD	Save %
AXXXX4_14	93.97%	98.04%	396	206	**192**	**6.80%**	602	**588**	**2.33%**
AXXXX9_24	97.83%	98.28%	396	61	**53**	**13.11%**	457	**449**	**1.75%**
AXXXX0_02	89.75%	98.11%	396	226	**214**	**5.31%**	622	**610**	**1.97%**
Average	93.85%	98.14%	396	164.33	**153**	**6.89%**	560.33	**549**	**2.02%**



High Volume Production Result

- Collected from 4 months, more than 20k wafers
- Wafers needing offline retest dropped from 17.4% to 5.67%



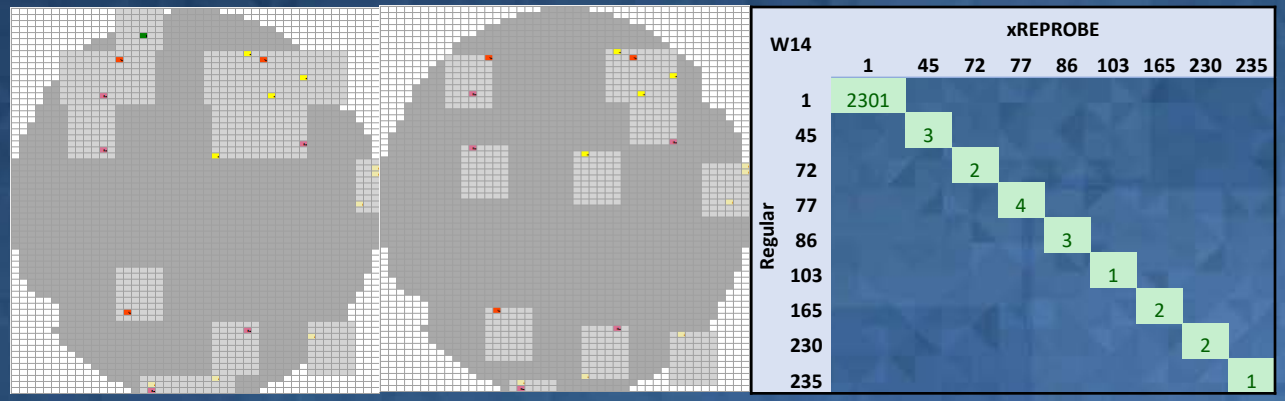


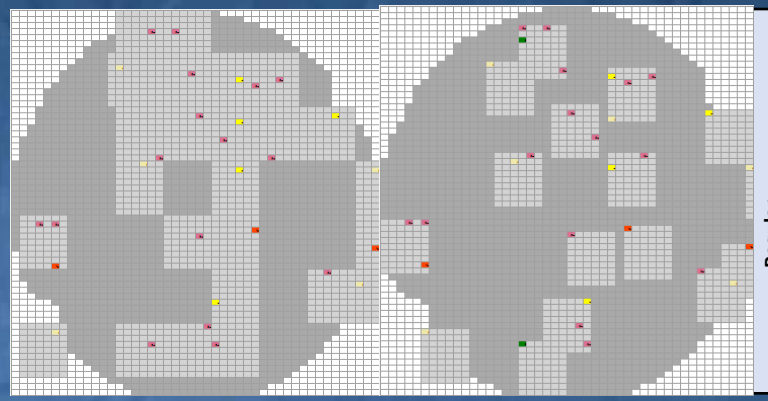
Case II:

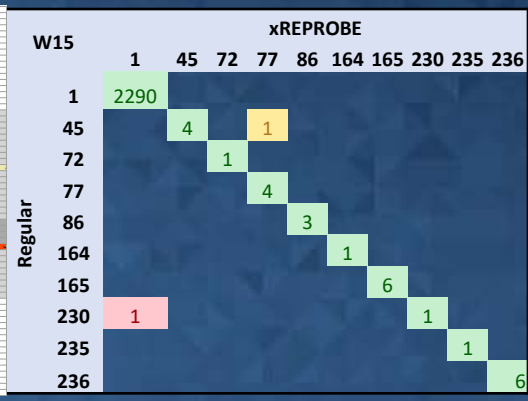
S customer with 54 site setup, long retest time from site efficiency

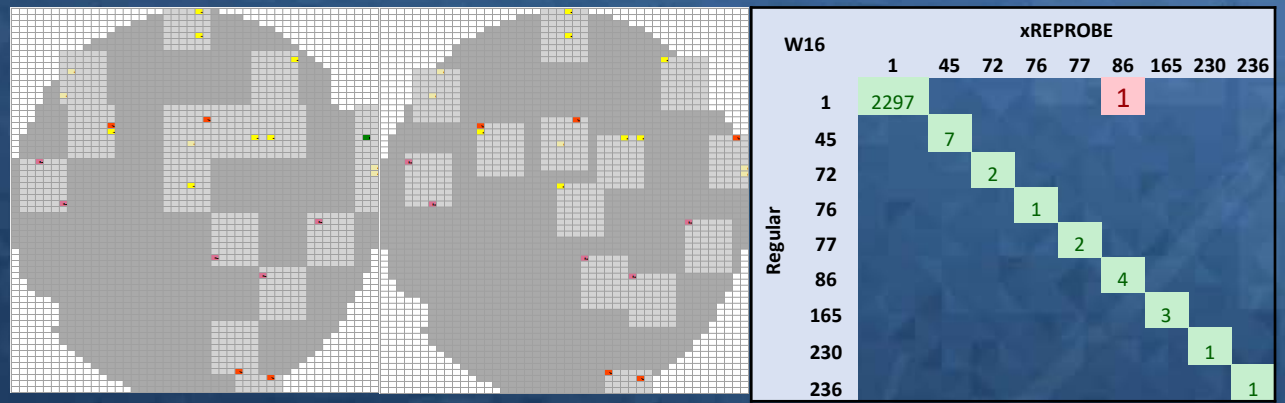
Wafer Result (Traditional -> xREPROBE)

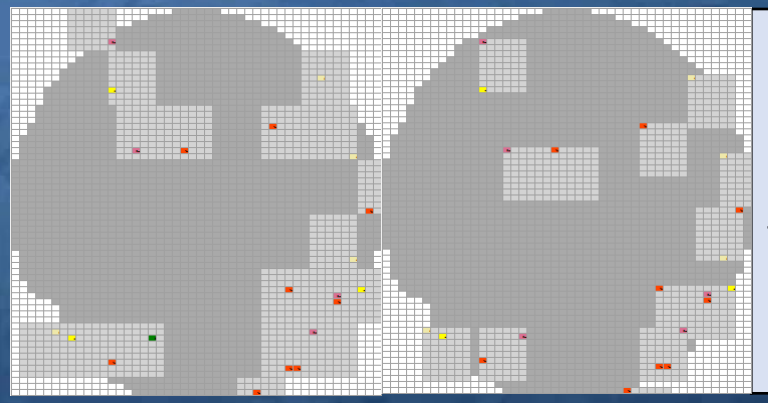
Traditional xReprobe Bin 2 Bin Traditional xReprobe Bin 2 Bin

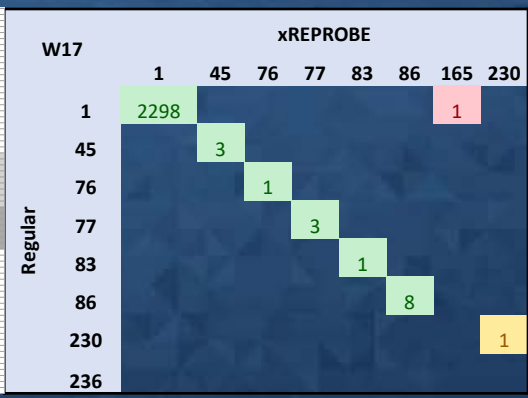












- **Probe path created differently to reduce test time**

Test Time Summary

		Touch Down	1st Retest Index	Index	Test Time	Index+Test	Total	Diff %
W14_Reg	1st Pass	54	N/A	1.14	6.17	7.32	591.16	
	Reprobe	15	1.61	0.78	2.53	3.30		
W14_xTest	1st Pass	54	N/A	1.01	6.12	7.14	520.64	11.93%
	Reprobe	11	1.54	0.64	2.85	3.49		
W19_Reg	1st Pass	54	N/A	1.21	6.20	7.41	663.42	
	Reprobe	27	1.60	0.68	2.19	2.86		
W19_xTest	1st Pass	54	N/A	1.01	6.18	7.19	548.33	17.35%
	Reprobe	18	2.52	0.58	2.69	3.26		
W15_Reg	1st Pass	54	N/A	1.13	6.12	7.25	608.51	
	Reprobe	25	1.61	0.87	2.26	3.13		
W15_xTest	1st Pass	54	N/A	1.01	6.19	7.20	508.03	16.51%
	Reprobe	16	2.55	0.58	3.08	3.66		
W16_Reg	1st Pass	54	N/A	0.70	6.07	6.77	520.79	
	Reprobe	16	1.61	0.73	2.32	3.06		
W16_xTest	1st Pass	54	N/A	1.06	6.09	7.15	493.80	5.18%
	Reprobe	13	2.40	0.82	1.84	2.66		
W17_Reg	1st Pass	54	N/A	0.71	6.05	6.76	518.47	
	Reprobe	18	1.60	0.89	1.88	2.77		
W17_xTest	1st Pass	54	N/A	1.10	6.09	7.19	502.39	3.10%
	Reprobe	13	2.62	0.63	2.04	2.66		
W20_Reg	1st Pass	54	N/A	1.15	6.12	7.27	574.45	
	Reprobe	20	3.42	0.68	1.99	2.67		
W20_xTest	1st Pass	54	N/A	1.02	6.12	7.14	510.70	11.10%
	Reprobe	14	2.66	0.57	2.60	3.17		
W22_Reg	1st Pass	54	N/A	1.14	6.15	7.29	602.84	
	Reprobe	24	4.07	0.71	2.60	3.31		
W22_xTest	1st Pass	54	N/A	1.01	6.12	7.13	516.08	14.39%
	Reprobe	16	2.55	0.74	2.80	3.54		
W23_Reg	1st Pass	54	N/A	1.19	6.10	7.29	562.71	
	Reprobe	25	3.49	0.72	1.47	2.19		
W23_xTest	1st Pass	54	N/A	1.06	6.09	7.15	513.52	8.74%
	Reprobe	19	2.68	0.75	1.67	2.42		
Avg_Reg	1st Pass	54	N/A	1.05	6.12	7.17	580.29	
	Reprobe	21.25	2.38	0.76	2.15	2.91		
Avg_xTest	1st Pass	54	N/A	1.03	6.13	7.16	514.19	**11.39%**
	Reprobe	15.00	2.44	0.66	2.45	3.11		

- All wafers reprobed with xREPROBE shows fewer TD count of reprobe
- Index time on regular are unstable, some longer and some shorter, xREPROBE more consistent and mostly shorter than regular
- Longer test time on xREPROBE is reasonable due to xREPROBE tested more rejects per touchdown during reprobe
- Average saving of **11.39%** on probing a wafer!

Trail Run Summary

- **Longer index time was observed on correlation wafer and first two wafers, program was improved and prober setting updated to met similar or better index time from normal reprobe**
- **Did not met site to site setup issue, hence full xREPROBE capability not demonstrated**
- **Test Time saving of 11.39% (or 66.1sec) per wafer on 8 wafers trail run! Or equal to $0.92 saving per wafer**
  - (Calculation assumed on hour rate of $50)

xTEST's Portfolio

xREPROBE

- **Provides auto calculated reprobing path to minimize rescreen test time, maximize recovery yields, and allow production flexibility without downtime**

xCLEANING

- **Provides proactive control in cleaning**
  - Maintain target yield
  - Provide maximum throughput by only cleaning when needed

xSETUP

- **Auto-Z to setup prober for production environment and adjust overdrive on the fly**
- **Auto correlation / GRR for production setup**

xDATA

- **Provides real time data analysis for alert , monitoring and probe decisions**
- **Setup data stream to any database upon request**

Thank you!!!

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