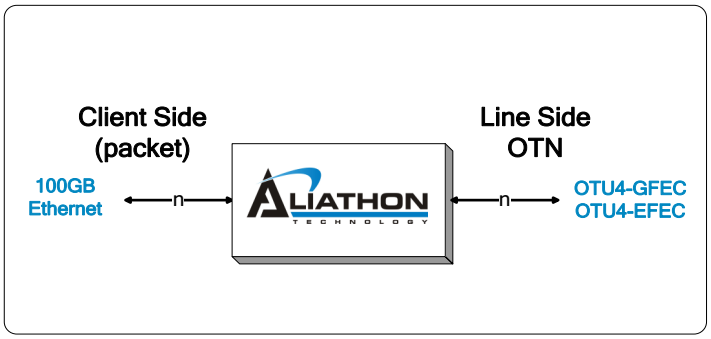
Overview

Aliathon's 100GE-OTU4 transponder is targeted towards packet optical transport in the OTN network. The application is the transport of 100GE clients over an OTN network, using the high-quality transmission capability of the OTN to extend the reach of a packet domain.

The solution is fully ITU G.709 compliant and resides in a single FPGA.



Headline Features

- 200MHz+ push button core performance.
- Sub 10W power consumption in today's leading edge FPGA fabrics.
- All products designed from ground up to allow future datapath & channel scaling.
    - Built on technology developed at 10G & 40G rates.
    - Enabling migration path to 400G solutions in the future.
- Direct access to core registers for rapid software development.
- Errors, defects and stats provided for client signal & OTU/ODU/OPU layers.
- CAUI client interface, OTL4.10 line interface.
- 100GB Ethernet mapped in to OTU4 payload via the GMP.
    - Ethernet stats supported via integrated MAC & PCS layers.
- OTU4 framing and section/path overhead processing.
- Support for both standard and enhanced FEC;
    - 7db NECG @ 6.7% OH G.709 GFEC.
    - 9.35db NECG @ 7% OH Enhanced FEC (CI-BCH-3™).

Figure 1 Overview

On the Ethernet side, 10 10.3125G SERDES are used to implement a CAUI (IEEE skew budget compliant) interface. After bit de-muxing, the individual lanes are 66B de-framed, de-skewed and reordered to produce an interface that is 10 aligned, contiguous 66B codewords wide. The associated PCS & MAC blocks (IEEE802.3 compliant) provide codeword unpacking, frame delineation and CRC checking.

The 100G Ethernet to OTU4 blocks bit transparently maps the 66B codewords into an ODU4 payload for transport by the OTU4 framer using the Generic Mapping Procedure (GMP).

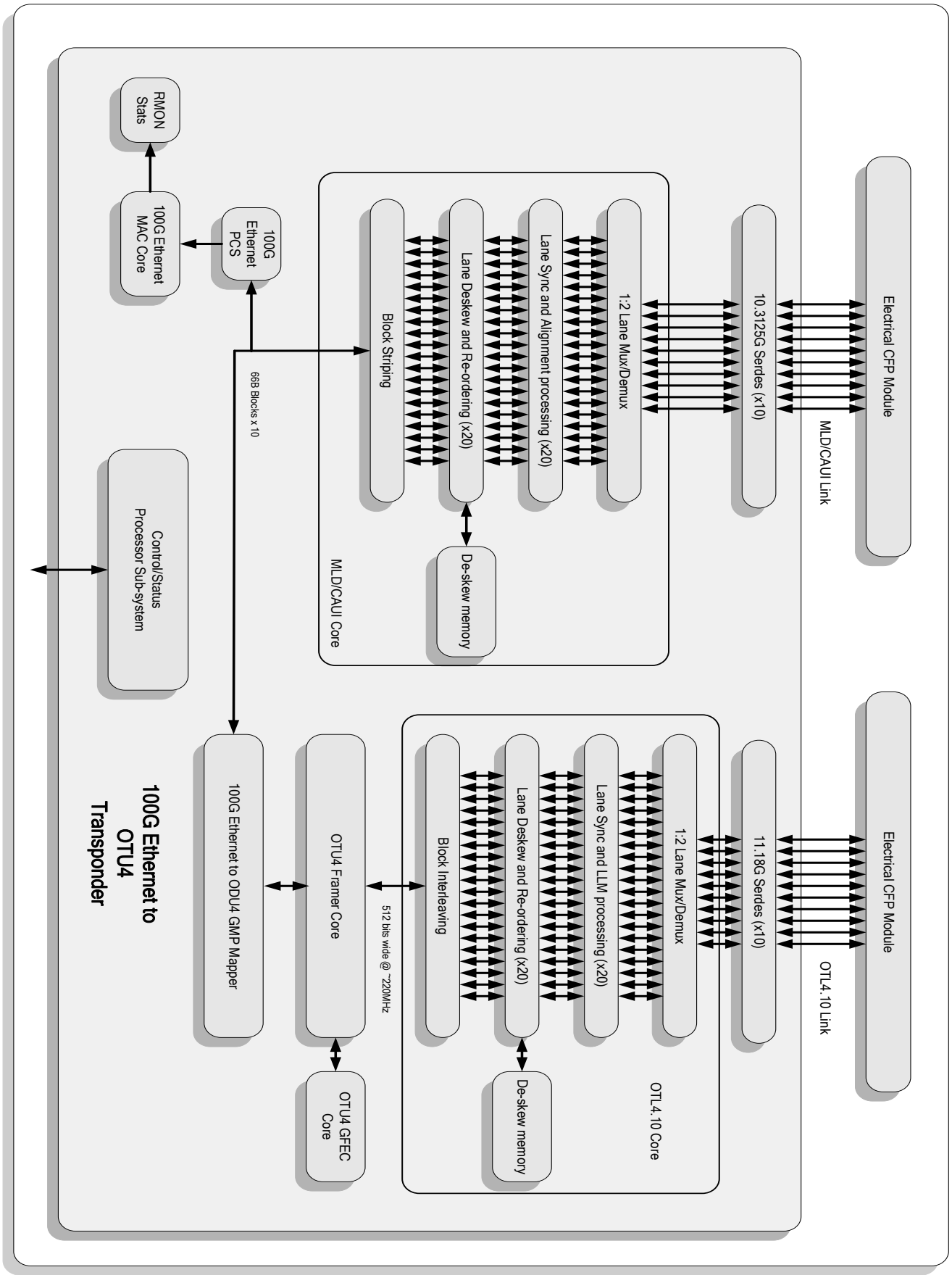
The OTU4 core provides standard G.709 OTN framing, scrambling, detection of parity errors and adds/drops the overhead.

FEC Options are;

- G.709 Standard Compliant FEC: 6.7% OH, delivering 7db of Net Electrical Coding Gain (NECG). Stats provided are corrected/uncorrected bits, blocks and codes
- Continuously Interleaved, 3-error correcting BCH (CI-BCH-3™) eFEC - 7% OH, delivering 9.35db of Net Electrical Coding Gain (NECG). Stats provided are corrected/uncorrected bits, blocks and codes

On the OTU4 side the design implements an OTL4.10 interface (supports 1024bits of skew matching the IEEE MLD Requirement). This incorporates 10 11.18G SERDES with individual lane framing (based on the OTU4 FAS pattern and the inserted LLM bytes), skew adjustment and reordering.

Figure 1: Architectural Block Diagram



OTN Overhead Alarms Supported / Processed

Frame

- OOF: Out of Frame (FAS error).
- LOF: Loss of Frame (OOF persistence).
- OOM: Out of Multiframe (MFAS error).
- LOM: Loss of Multiframe (OOM persistence).

OTU Section Monitoring

- SM-BIP-8: SM Bit Interleaved Parity.
- SM-BEI: SM Backward Error Indication.
- OTU-AIS: OTU Alarm Indicator Signal.
- SM-BDI: SM Backward Defect Indicator.
- SM-IAE: SM Incoming Alignment Error.
- SM-BIAE: SM Backward Incoming Alignment Error

ODU Path Monitoring & TCM

- PM-BIP-8: PM BIP Error
- PM-BEI: PM Backward error Indication.
- ODU-AIS: ODU Alarm Indicator Signal.
- ODU-OCI: ODU Open Connection Indication.
- ODU-LCK: ODU Lock Defect.
- PM-BDI: PM Backward Defect Indication.
- PM-TIM: Trace Identified Missmatch.
- TCMi-BIP-8, TCMi-BEI, TCM-BDI, TCM-BIAE, TCM-AIS, TCM-OCI, TCM-LCK, TCM-LTC, TCM-IAE, TCM-TIM.

OPU

- PTM: Payload Type Missmatch
- CSF: Client Signal Fail.

Target Families & Deliverables

Altera

- Stratix
- Arria

Xilinx

- Virtex
- Kintex

IP

- EDIF/BIT/SOF/QSF/UCF. Encrypted ModelSim & Back annotated VHDL

Documentation

- Datasheet, Verification Results, User Guide.

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