Technical Overview: WIP Tracking IC Manufacturing Workflow and Cycle-time Reduction

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Introduction

It is well known that talented product planners and engineers can achieve tremendous savings in time and money through their knowledge of the workflows and relationships in the integrated circuit (IC) manufacturing supply chain.

This document describes the "prototype" and "mass production" workflows based on typical durations for the purposes of discussing Work-in-Progress (WIP) tracking and optimization. Written from the perspective of a fabless ASIC provider, this paper proposes that WIP tracking can reduce the cycle time from GDSII tape-out to the delivery of packaged and tested chips.

The potential of various WIP tracking mechanisms to reduce cycle time is presented based on typical project plans for prototype and production runs. Using a mathematical framework to analyze the cycle-time reductions (CTR), each mechanism is evaluated for both workflows during normal operation and in the case of unforeseen circumstances. An analysis based on conservative assumptions reveals the following potential cycle time reductions:

WORKFLOW	NORMAL OPERATION	UNFORSEEN PROBLEMS OCCURRED
Prototype	-14%	-17%
Production	-14%	-18%

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Motivation for WIP Tracking

WIP tracking provides silicon suppliers and their customers with visibility into the progress of the manufacturing process. This enables cycle-time reduction and continuous improvements in efficiency throughout the IC manufacturing supply chain.

While visibility for the customer is the most obvious value of WIP tracking, the exchange of more reliable scheduling information within the supply chain can also reduce overall cycle time. Each participant of the supply chain can optimize its processing to a much tighter schedule.

Visibility: Build Credibility and Correct Quickly

Virtually all design project managers are under incredible pressure to reduce the cycle time from "design start" to "volume production". A significant part of the cycle is the time spent from "GDSII tape-out"[1] to volume production. The following steps are part of this sub-cycle:

1. GDSII tape-out
2. Prototype manufacturing
3. Debugging of the design data and test programs
4. Additional prototype-manufacturing cycle
5. Preparation of volume production, e.g., improving design and test program
6. First volume production run

During the GDSII tape-out to "manufactured and tested parts" phase, there maybe as many as seven subcontractors involved in the supply chain. It is likely that some of these subcontractors are located in other time zones and other countries.

WIP tracking empowers the customer through complete visibility into the design and manufacturing process. WIP data is updated daily and made accessible via the web. This allows the customer to schedule follow-up activities as soon as the manufacturing process has progressed far enough to provide sufficient confidence that the expected delivery date will be met.

Visibility also enables the customer to take necessary measures to protect its business goals in the event any phase of the process cannot be completed according to plan. For example, the customer can react to unforeseen issues by re-scheduling tasks related to the delivery of manufactured and tested parts.

[1] The tape-out has long been replaced by ftp-out. Therefore, "tape-out" describes the step in which a design team commits to a final version of the layout.

Cycle-time Reduction

Creation of an Internet infrastructure for the exchange of vital WIP data can drastically improve the flow information within the supply chain. For example, if information about the status of a particular process is sent more quickly, resulting actions can be performed in a more timely manner.

WIP tracking and intelligent processing can reduce the cycle-time via the following mechanisms. Detailed discussions of these mechanisms are provided in the subsequent section entitled, " Cycle-time Reduction Enabled by WIP Tracking".

1. Workflow automation.
2. Advanced notices to supply chain partners.
3. Alerts to product engineers, planners, and other process controllers to correct problems quicker.
4. Just-in-time design / manufacturing of ICs.
5. Real-time padding reduction: dynamic tightening of planning and safety margins.
6. Tighter long-term planning based on statistical analysis of manufacturing data.
7. The ability to instantaneously place make-up orders.

Over time, WIP tracking accumulates a database of manufacturing run information that provides a foundation for statistical analysis. This analysis can provide insight into meaningful approaches for a systematic, continuous improvement of the manufacturing workflow. For example, manufacturing partners can be evaluated on their ability to deliver parts within the agreed-upon schedule.

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Workflows

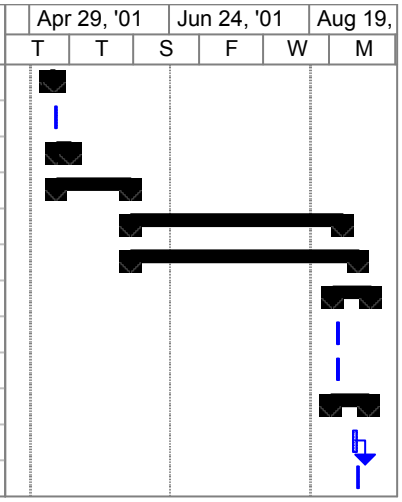
In this section, two exemplary manufacturing workflows will be described: prototype / NRE and production. Generally, both have many variations. However, the workflows described below provide a good baseline for the discussion of WIP tracking.

Prototype / NRE

Overview of the Prototype/NRE Flow

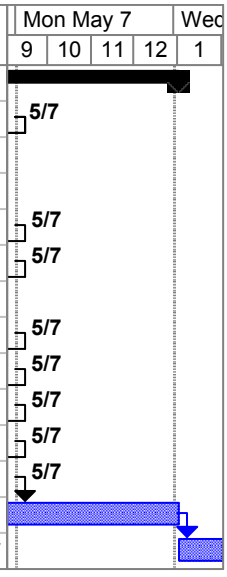
The following are the major steps in a Prototype/NRE flow:

Task Name	Duration
Quotation Processes	**2 days**
Time taken by customer to decide	1 day
Order Processing	**3 days**
ASIC Vendor GDSII Preparation	**21 days**
Work at Foundry	**61 days**
Work at Probe / ASSY / Test	**65 days**
Work at ASIC provider: Test Program debugging	**11 days**
Move out probe cards to shipper (for Transfer to ASSY)	1 day
Transfer Data: transfer SORT and Final to ASSY	1 day
Transfers by Freight Forwarder	**11 days**
Deliver Parts	1 day
Invoice Customer	1 day



Quotation Process

Task Name	Duration
Quotation Processes	**2 days**
RFQ Submitted	0 days
ASIC provider RFQ Processes	**0 days**
Collecting preliminary technical details from customer	**0 days**
Foundry Technology	0 days
Package selection	0 days
Delivery Estimation	**0 days**
Get foundry wafer capacity availability/schedule	0 days
Confirm ASSY availability	0 days
Check on Design Services Availaibility/Scheduling	0 days
Return Delivery Estimate	0 days
Customer Qualification	0 days
Quote Returned	2 days
Time taken by customer to decide	1 day



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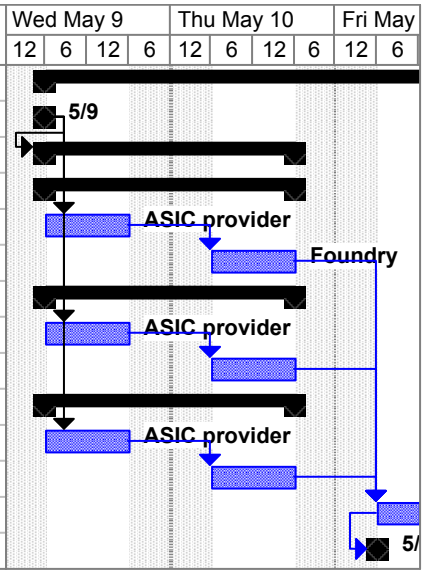
The quotation process includes all actions following the submission of the request for quote (RFQ) by the customer through the signing of the manufacturing contract. After receiving the RFQ, the ASIC provider evaluates the viability of the business opportunity and the availability of required internal and external resources including wafer allocations, design service availability, etc.

The quote estimate is delivered to the customer as soon as these tasks are completed. The customer and the ASIC provider collaborate to refine the description of the project and its deliverables, and then a manufacturing contract is signed.

Order Processing

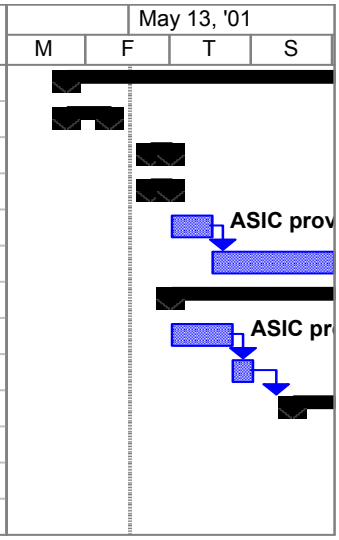
Task Name	Duration
Order Processing	**3 days**
Purchase Order Submitted to ASIC provider	0 days
Work Order Processing	**2 days**
Purchase Order to foundry	**2 days**
Send Purchase Order	1 day
Confirmation of PO	1 day
Work Order to Probe / ASSY / Test	**2 days**
Send Work Order against blanket PO	1 day
Confirmation of WO	1 day
Work Order to Freight Forwarder	**2 days**
Send Work Order against blanket PO	1 day
Confirmation of WO	1 day
Confirmation of Purchase Order to Customer	1 day
Invoice customer	0 days



After the customer submits the purchase order, the ASIC provider in turn submits the appropriate purchase orders to the various sub-contractors and freight providers. After each of these purchase orders are confirmed, the ASIC provider notifies the customer of the confirmation, and subsequently invoices the customer.

GDSII Preparation Process

Task Name	Duration
GDSII Preparation	**19 days**
Design Team Set-up	**2 days**
Ship Design Kit to Customer	**1 day**
Collecting final technical details	**1 day**
QA incoming test vectors	2 days
Preliminary Test-Program Development	14 days
Signal integrity checking	**15 days**
DRC	3 days
Order Loadboard, probe card, burn-in board, etc.	1 day
Design Sign-Off	**3 days**
Data Transfer to Manufacturing Partners	**1 day**
GDSII Transfer to Foundry	**1 day**
Transfers to ASSY	**1 day**



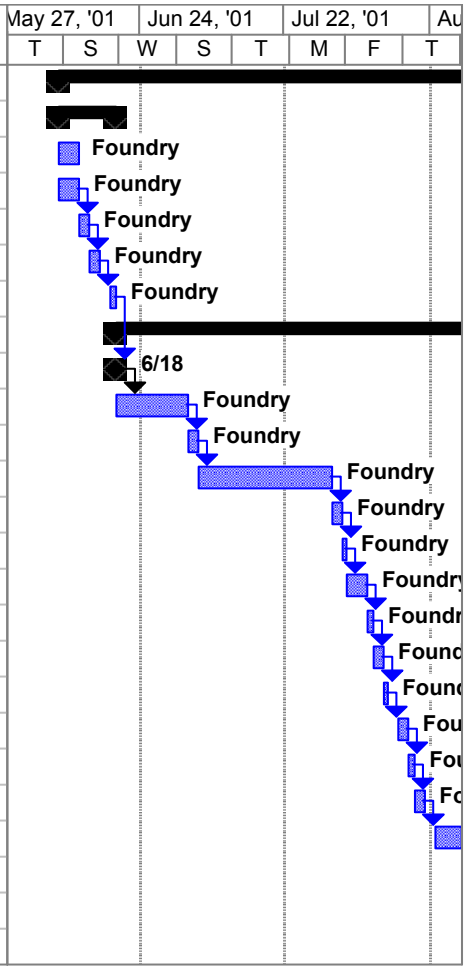
After receiving the purchase order from the customer, the ASIC provider assembles a design team appropriate for the particular project, and then hosts a design review kick-off session with the customer's design team. At this point, the ASIC provider delivers the design kit to the customer, which includes design rule check (DRC) decks, SPICE models, and package templates. The customer outlines for the ASIC provider the required technical details, such as specifications for foundry, package, and test.

The ASIC provider then proceeds to qualify the test vector specifications provided by the customer, and immediately begins development of the preliminary test program. During this "GDSII preparation phase", the ASIC provider can also deliver other design-related services, such as signal integrity checking, if requested.

After the customer completes the GDSII design, the ASIC provider runs the appropriate DRCs against the foundry-standard DRC decks. Orders for the required test hardware based on the bond pad information are then submitted. Once "design sign-off" has taken place, the design and package data is transferred to the foundry and assembly partners.

Foundry

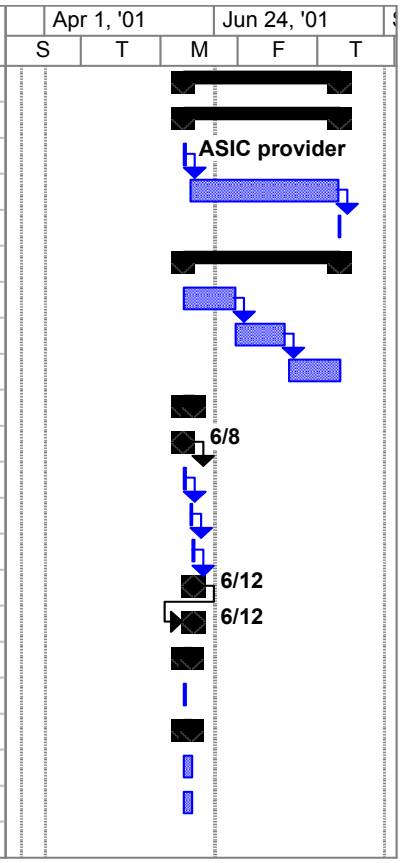
Task Name	Duration
Work at Foundry	**61 days**
Layout pre-processing	**7 days**
Phase shift masking	2 days
Optical proximity correction	2 days
Add frame to GDSII	2 days
Add scribe line	2 days
Add Process Monitors	1 day
Wafer Fabrication	**54 days**
lot start	0 days
Intermediate Steps	10 days
Poly-Si Layer Definition	2 days
Intermediate Steps	18 days
Metal 1 Definition	2 days
Intermediate Steps	1 day
Metal 2 Definition	2 days
Intermediate Steps	1 day
Metal 3 Definition	2 days
Intermediate Steps	1 day
Metal 4 Definition	2 days
Intermediate Steps	1 day
Metal 5 Definition	2 days
Intermediate Steps	6 days
Wafer Acceptance Test	1 day
SORT Test	2 days
Move out of the fab and ship	1 day



After the GDSII design is taped-out to the foundry partner, the foundry partner will generate the masks and manufacture the prototype wafers.

Assembly

Task Name	Duration
Work at Probe / ASSY / Test	**56 days**
Probe card making	**56 days**
Receive probe card data	1 day
Build probe / load cards and sockets	54 days
Transfer of cards and sockets to shipper	1 day
Package Development	**56 days**
Design package	18 days
Tooling requirements	18 days
Fabricate prototype	20 days
Packaging (Mass Production)	**3 days**
Receive Wafers	0 days
Die Bank	1 day
Die Attach	1 day
Mold	1 day
Move out to Shipper for Transfer to Test	0 days
Transfer to Testing (within ASSY)	0 days
Testing	**2 days**
Receive Probe cards	1 day
Verify Final Test Program	**2 days**
Get back SORT and Final test pgm	2 days
Verify that pgms are OK	2 days



Test hardware and package tooling starts immediately following design sign-off and data transfer to manufacturing partner during the GDSII preparation phase. This ensures that sufficient time is provided to complete these product-engineering tasks before the prototype wafers are ready.

Development of the preliminary test program also starts during the GDSII preparation phase so that an early version of the program is available when wafers are ready. The wafers are assembled and shipped to the ASIC provider for test program debug and testing.

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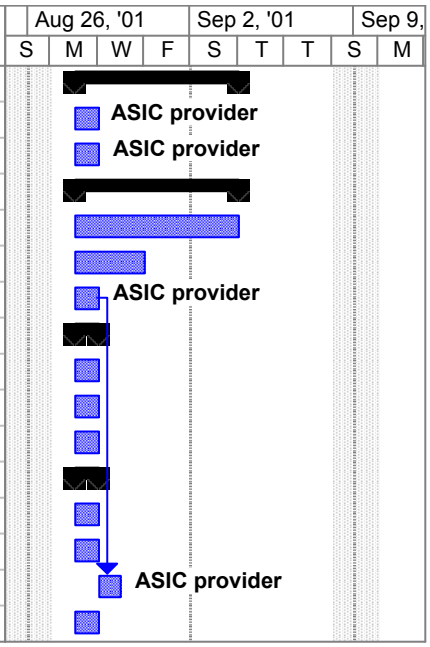
Work at the ASIC Provider

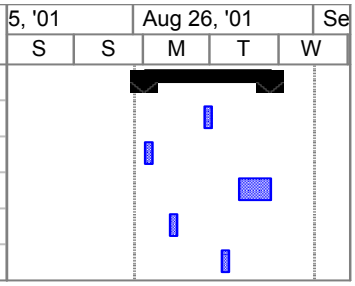
Task Name	Duration
Test Program debugging	**5 days**
Receive probe/load cards from Probe card house	1 day
Receive packaged part from ASSY	1 day
Debug SORT and Final test program	**5 days**
Debug Final test program	5 days
Develop & Debug SORT program	3 days
Transfer SORT and Final test programs to ASSY	1 day
Characterization	**1 day**
Proto lot	1 day
Corner lot	1 day
Product qualification	1 day
Testing of prototype parts for customer	**1 day**
Final Test	1 day
Approval of Test PGM by eSi customer	1 day
Move out probe cards to shipper (for Transfer to ASSY)	1 day
Transfer Data: transfer SORT and Final to ASSY	1 day



Test program debugging, prototype testing, and characterization are performed by the ASIC provider, once the initial prototypes are assembled and available from the foundry and assembly partners.

Transfer by Freight Forwarders

Task Name	Duration
Transfers by Freight Forwarder	**11 days**
Wafers: Foundry => ASSY	1 day
Probe/load Cards: ASSY => Test	1 day
Parts: ASSY => Test	2 days
Probe/load Cards: ASIC provider => ASSY	1 day
Parts: ASSY => Customer	1 day



The logistic/freight forwarder partner assists the ASIC provider in transporting the parts between their facility and the various manufacturing partners.

Continuous WIP Update

The ASIC provider continuously updates the WIP and engineering data for the customer throughout the entire manufacturing process. Data is downloaded from the foundry, assembly, and freight partners. Yield reports are updated and accessible as sc ıs data is downloaded.

Status data and schedules are also continuously updated and accessed through WIP tracking. Alerts and flags are sent when movement in the foundry, assembly, or freight phases differs by a specified margin from pre-defined durations.

Summary of Prototype/NRE Flow

WORKFLOW STEP	ACTOR	TOTAL TIME
Order Processing	ASIC provider	3
GDSII Preparation	ASIC provider	19
Fabrication	Fab	61
Probe Card Making	ASSY	56
Package Design	ASSY	56
Wafer Transfer	Freight Forwarder	1
Packaging	ASSY	3
Parts Transfer	Freight Forwarder	1
Test & Debug	ASIC provider	5
Parts Transfer	Freight Forwarder	1
TOTAL		**94**

Production

The production flow is less complex than the prototype / NRE flow, since many "tools" have been produced and tested in the prototype flow. The main differences from the prototype flow are:

1. Final mask preparations, e.g., DRC not required.
2. A verified test program is already available; therefore, the test program may only be improved.
3. Tools, like masks or probe cards, are already available. Potentially, additional probe cards may need to be ordered.

Additional complexity may be introduced in the production phase in order to meet the volume goals, e.g., assembly at different manufacturing partners. The prototype flow is driven by the need to get "working parts" as quickly as possible. Whereas, the production flow is driven by the need to meet production goals of the customer in an economical manner.

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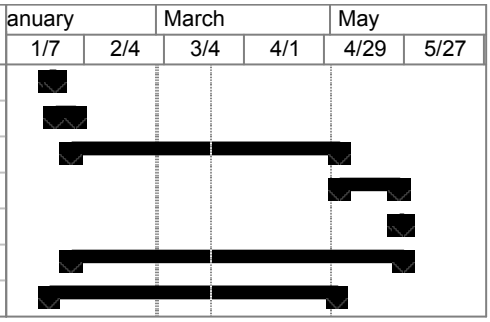
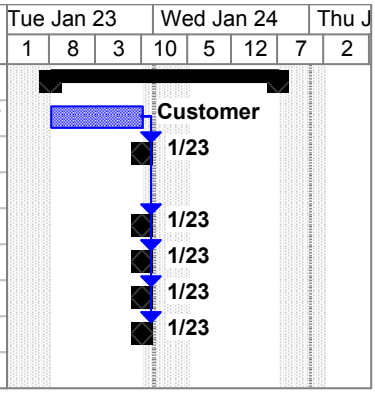
Overview of the Production Flow

Task Name	Duration
Quotation Processes	**2 days**
Order Processing	**5 days**
Work at Foundry	**68 days**
Work at Probe / ASSY / Test	**15 days**
Work at ASIC provider	**1 day**
Transfers by Freight Forwarder	**84 days**
Continous WIP update	**73 days**



Quotation Process

Task Name	Duration
Quotation Processes	**2 days**
RFQ Submitted	1 day
ASIC provider RFQ Processes	0 days
Confirmation of final production data	**0 days**
Final test program	0 days
Foundry Technology and FAB Selection	0 days
Package selection	0 days
Package marking	0 days
Check available assets	**0 days**



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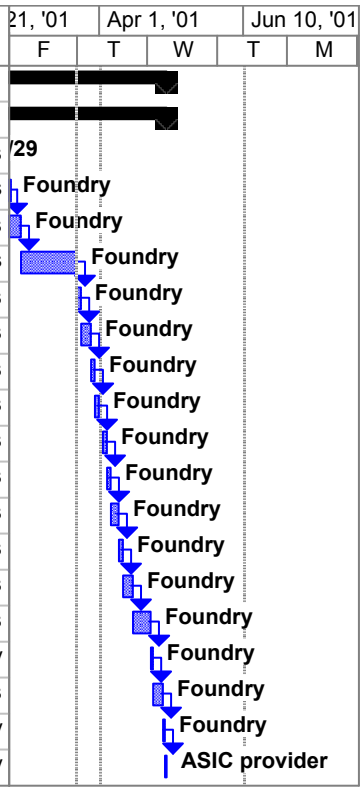
Foundry

Task Name	Duration
Work at Foundry	**68 days**
Wafer Fabrication	**68 days**
Lot start	0 days
Intermediate steps	14 days
Poly-Si Layer Definition	3 days
Intermediate steps	20 days
Metal 1 Definition	2 days
Intermediate steps	2 days
Metal 2 Definition	2 days
Intermediate steps	2 days
Metal 3 Definition	2 days
Intermediate steps	2 days
Metal 4 Definition	2 days
Intermediate steps	2 days
Metal 5 Definition	3 days
Intermediate steps	7 days
Wafer Acceptance Test WAT	1 day
SORT Test (Probe cards needed)	2 days
Move out of the fab and ship	1 day
Triggers payments -> Finance	1 day



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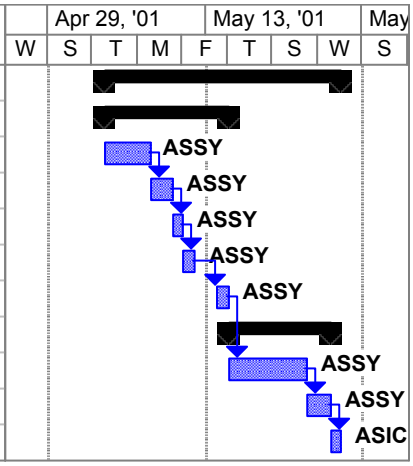
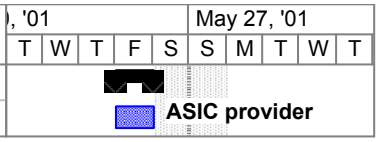
Assembly

Task Name	Duration
	15 days
Assembly	**7 days**
Die Separation (Scribe / Break)	2 days
Die Attach	2 days
Wire bond	1 day
Mold (Seal / Lead trim)	1 day
Marking	1 day
Final Testing	**7 days**
Final Test	5 days
Burn-in tests (rare)	2 days
Release final parts to Customer	1 day



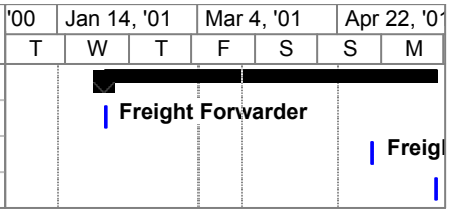
Work at ASIC Provider

Task Name	Duration
Work at ASIC provider	**1 day**
Invoice customer	1 day



Freight Forward

Task Name	Duration
Transfers by Freight Forwarder	**84 days**
Probe Cards: ASSY => Foundry	1 day
Wafers: Foundry => Probe / ASSY / Test	1 day
Parts: Test house => customer	1 day



Summary of Production Flow

WORKFLOW STEP	ACTOR	TOTAL TIME
Order Processing	ASIC provider	5
Fabrication	Fab	68
Wafer Transfer	Freight Forwarder	1
Package/Test	ASSY	15
Parts Transfer	Freight Forwarder	1
TOTAL		**90**

Cycle-Time Reduction Enabled by WIP Tracking

There are three principal mechanisms for reducing cycle time of the IC manufacturing process. Option one is not within the ASIC provider's control. Therefore, this discussion is focused on options two and three.

1. Reducing the mean time needed to perform a given step, e.g., the lapping of the wafers before assembly.
2. Reducing the intra-process uncertainty through better dissemination of information within the supply chain.
3. Introduction of parallelism, in which some processes can be performed simultaneously.

Better Information Flow

WIP tracking provides a holistic view of the information flow, and as such it enables improvements at a systemic level. To this end, several types of information exchanges and the corresponding actions and recipients have been identified.

1. *Exchange:* Immediate ***"end-of-action notice"***
   Recipient: A downstream activity or actor that performs a planned activity (designer, test engineer, etc.)
   Action: A notification that a planned activity is finished, and the next activity in the process can begin. The "notifier" is the predecessor of the "notifyee" in the process flow. *The purpose of this is to give a real-time "wake-up" call to the next action so that no time is lost between the steps.*
   (This is a good illustration of workflow automation in action.)

2. *Exchange:* An ***"advanced notice"***
   Recipient: A *remote* downstream activity or actor that performs a planned activity (designer, test engineer, etc.)
   Action: An update of the earlier planned activity *with the purpose of reducing uncertainty relating to the status of the current step*.

3. *Exchange:* An ***"alert notice"*** that a certain step of the process is out of the norm
   Recipient: A "workflow supervisor" or "controller" whose role is to make sure the process is on track (product engineering, logistics people, payables, etc.)
   Action: Fix the problem to resume process.
   Notification is sent ONLY if the process is out of the norm!

Concurrency

Cycle-time reduction can also be achieved through "parallelism". This is when two or more activities are executed concurrently, though traditionally they are performed sequentially.

Basic Cycle-Time Reduction Mechanisms

Workflow Automation

Complete workflow automation ensures that information about the status of the process is always available in real time and is updated automatically on a continuous basis. When one step of the process is completed, the next step is automatically notified and initiated as soon as possible.

Basic Mechanism: "end-of-action" notice

Advance Notices to Supply Chain Partners

The WIP data allows the ASIC provider to give advanced notice to the downstream supply chain partners. Advanced notices might contain expected shipment dates and the actual content of a particular shipment. Such notices allow the supply chain partners to optimize their internal processes and thereby reduce cycle time. For example, some packaging vendors have indicated that they could reduce their cycle time by 20 to 50 percent, if they receive reliable advanced notice of incoming shipments.

Basic Mechanism: "advance" notice

Alerts to Product Engineers, Planners, and Other Process Controllers to Correct Problems Quicker

When something unforeseen occurs during the manufacturing cycle, WIP data enables participants to react quickly and get the project back on track. For example, perhaps a shipment is incorrectly labeled to go to a supply partner other than the one next in the workflow. Consequently, it sits for days on the dock of the downstream supply chain partner, and the process is delayed. In a case such as this, WIP updates allow product engineers to quickly discover and correct the situation.

Basic Mechanism: "alert" notice

Just-in-time Design / Manufacturing of ICs

Reliable WIP tracking enables supply chain partners to input data or materials "just-in-time" for use within the workflow. The ability to overlap outputs from supply partners has tremendous potential to reduce the cycle time[2] by fundamentally improving the information flow between IC design and manufacturing. For example, detailed design data about the metal layers is only needed halfway through the foundry process in many cases.

Basic Mechanism: "concurrency"

[2] WIP tracking is necessary, but not sufficient for JIT design / manufacturing, since the libraries and design flows must also be suitable, e.g., sea-of-gates library and JIT-DRC.

Systemic Mechanisms for Cycle Time Reduction

Real-time Padding Reduction: Dynamic Tightening of the Planning and Safety Margins

Real-time WIP updates reassure customers and supply chain partners that the manufacturing process is indeed on-track. As a result, the customer and supply chain partners can avoid the cumulative effects of contingency "padding" and proceed with greater confidence toward meeting the delivery target. For example, the customer can schedule activities with greater certainty once the previous step is two-thirds completed.

Mechanism: "better information flow"

Tighter Long-term Planning

WIP tracking allows the ASIC provider to automatically collect accurate project data and perform a statistical analysis of past performance, e.g., *98 percent of deliveries within two days of promised target*. The results will help the ASIC provider, its partners and the customer to plan with less "schedule padding".[3]

Mechanism: "better information flow" and "Reduction of uncertainty leads to increased confidence level" allow the immediate activation of subsequent steps without contingency[4]

Ability to Instantaneously Place Make-Up Orders

The "instantaneous" availability of testing and quality data is an important aspect of WIP tracking. Test and quality data is used by product engineers to identify yield problems, determine root causes, and to quickly react with corrective actions or alternatives. For example, "make-up" orders can be placed immediately to ensure that customer delivery commitments are met.

Mechanism: "better information flow"

[3] Illustration of the "random variable" target date: If you know with 98 percent confidence level that the target will be met within plus/minus two days of target and you assume that 98 percent confidence level is sufficient for your planning, then two days of schedule padding is sufficient. In short: higher confidence level will lead to less schedule padding.

[4] Reduction of cycle-time variance within the flow enables a reduction of the mean cycle time for customers.

Analytical Cycle-Time Model

The following model is used to describe the multi-step manufacturing process and to quantify the exact cycle-time reduction.

$$T_{cycle} = \sum_{i=1}^{N} T_{step}^{i}$$

Time spent on each step is described by the following equation.

$$T_{step} = dt_{lag} + dt_{prep} + T + dt_{safe} + dt_{post}$$

- dt_{lag} is the time between when the "start" message is available from the previous step and the time any response actually happens (human/system "delay" factor, e.g., somebody assigned to a task gets the "start" message in-time, but is unavailable to perform the task.)

- dt_{prep} is the time between registration of the "start" message and when the prescribed activity actually begins (scheduling, preparation, queuing, etc., e.g., somebody assigned to a task gets the "start" message, but can't execute the task since a required resource such as a tester is not available at that time.)

- T is the "ideal" time for a given process step ("station" time).

- dt_{safe} is the contingency time or "padding" for some unexpected event (longer-than-expected delay, manufacturing and yield problems, etc.).

- dt_{post} is the time between when the activity has finished and the next step is notified. (For example, somebody may have completed an assigned task, but for some reason the "notice of completion" doesn't arrive in timely fashion at the supply chain partner downstream in the process.)

MEANS TO REDUCE THE CYCLE-TIME COMPONENTS

- dt_{lag} can be reduced through *"end-of-action"* notice.
- dt_{prep} can be reduced through *"advanced"* notice.
- dt_{safe} can be reduced through *"real-time"* WIP updates.
- dt_{post} can be reduced through *"status alert"* notice.

The following table summarizes this section:

DELAY FACTOR	dt_{lag}	dt_{prep}	dt_{safe}	dt_{post}
CTR Mechanism	*"End-of-action"*	*"Advanced notice"*	**"***Real-time WIP updates"*	*"Status alert"*

Case Studies

Several cases are presented in this section to illustrate the cycle-time reduction potential of a WIP tracking system for both the prototype and production flows.

Prototype Flow

"Normal" Flow Without WIP Tracking

Conditions: Normal (problem-free) workflow. The WIP system is not implemented. This is the base case.

Assumptions: All the durations are taken from the MS project specification of the workflow. All the durations are broken down into the five components of the analytical cycle-time model described earlier. The safety margin (padding time) is on the order of 10 to 15 percent, which is believed to be fairly conservative[5]. The cycle-time reductions may be even more impressive in real-world scenarios.

WORKFLOW STEP	ACTOR	TOTAL TIME	Tlag	Tprep	Tstat	Tsafe	Tpost
Order Processing	ASIC provider	3	0.5		1.5		0.5
GDSII Preparation	ASIC provider	19	1	2	12	3	1
Fabrication	Fab	61	2	4	47	6	2
Probe Card Making	ASSY	56	2	4	44	5	1
Package Design	ASSY	56	2	4	44	5	1
Wafer Transfer	Freight Forwarder	1			1		
Packaging	ASSY	3	0.5	0.5	1.5		0.5
Parts Transfer	Freight Forwarder	1			1		
Test & Debug	ASIC provider	5	0.5		3	2	0.5
Parts Transfer	Freight Forwarder	1			1		
TOTAL		**94**					

The expected total length of this prototype flow is: 94 days.

[5] The "contingency time buffer" also known as "schedule padding" is determined by the perceived variance of the target time. Sources reveal that even a 15 percent variance is quite low.

Technical Overview: WIP Tracking
IC Manufacturing Workflow and Cycle-time Reduction

"Normal" Flow with WIP: All the Benefits are Merely Due to CTR Mechanisms

Conditions: Normal (problem-free) workflow. The WIP system is implemented.

Goal: Demonstrate that the WIP infrastructure can reduce cycle time through the mechanisms described in this document even when everything goes according to plan.

Assumptions: CTR factors were assumed uniformly for each step of the process. The percentage represents the reduction in uncertainty that can be achieved for the given delay through the WIP system. These are believed to be fairly conservative. The cycle-time reductions may be even more impressive in real-world scenarios.

CTR FACTOR	dt_{lag}	dt_{prep}	dt_{safe}	dt_{post}
Percent Reduction	50%	50%	50%	50%

The workflow schedule**:**

WORKFLOW STEP	ACTOR	TOTAL TIME	Tlag	Tprep	Tstat	Tsafe	Tpost
Order Processing	ASIC provider	2	0.25	0	1.5	0	0.25
GDSII Preparation	ASIC provider	15.5	0.5	1	12	1.5	0.5
Fabrication	Fab	54	1	2	47	3	1
Probe Card Making	ASSY	50	1	2	44	2.5	0.5
Package Design	ASSY	50	1	2	44	2.5	0.5
Wafer Transfer	Freight Forwarder	1	0	0	1	0	0
Packaging	ASSY	2.25	0.25	0.25	1.5	0	0.25
Parts Transfer	Freight Forwarder	1	0	0	1	0	0
Test & Debug	ASIC provider	4.5	0.25	0	3	1	0.25
Parts Transfer	Freight Forwarder	1	0	0	1	0	0
TOTAL		**81**					

The expected total length of this prototype flow is: 81 days. **This is a 14 percent improvement.**

Workflow with Unplanned Exceptions

Conditions: Wafers were mislabeled at Fab-ASSY Transfer. Five days are lost.

Assumptions: Real-time WIP updates enable the problem to be detected early. Only two days are lost.

Result: Without WIP, the expected total length of this prototype flow taking into account delays is: 99 days. The implementation of WIP notifications reduces the expected total length of this prototype flow to: 82 days. **This is a 17 percent improvement in cycle time.**

Manufacturing Flow

"Normal" Flow Without WIP Tracking

Conditions: Normal (problem-free) workflow. The WIP system is not implemented. This is the base case.

Assumptions: All the durations are taken from the MS Project specification of the workflow. All the durations were broken down into the five components of the analytical cycle-time model described earlier. The safety margin (padding time) is on the order of 10 to 15 percent, which is believed to be fairly conservative. The cycle-time reductions may be even more impressive in real-world scenarios.

WORKFLOW STEP	ACTOR	TOTAL TIME	Tlag	Tprep	Tstat	Tsafe	Tpost
Order Processing	ASIC provider	5	0.5		1.5		0.5
Fabrication	Fab	68	2	4	54	6	2
Wafer Transfer	Freight Forwarder	1			1		
Package/Test	ASSY	15	1	2	9	2	1
Parts Transfer	Freight Forwarder	1			1		
TOTAL		**90**					

The expected total length of this manufacturing flow is: 90 days.

"Normal" Flow with WIP: All the Benefits are Merely Due to CTR Mechanisms

Conditions: Normal (problem-free) workflow. The WIP system is implemented.

Goal: Demonstrate that the WIP infrastructure can reduce cycle time through the mechanisms described in this paper even when everything goes according to plan.

Assumptions: CTR factors were assumed uniformly for each step of the process. The percentage represents the reduction in uncertainty that can be achieved for the given delay through the WIP system. These factors are believed to be fairly conservative. The cycle-time reductions may be even more impressive in real-world scenarios.

CTR FACTOR	dt_{lag}	dt_{prep}	dt_{safe}	dt_{post}
Percent Reduction	50%	50%	50%	50%

The workflow schedule:

WORKFLOW STEP	ACTOR	TOTAL TIME	Tlag	Tprep	Tstat	Tsafe	Tpost
Order Processing	ASIC provider	2	0.25	0	1.5	0	0.25
Fabrication	Fab	61	1	2	54	3	1
Wafer Transfer	Freight Forwarder	1	0	0	1	0	0
Packaging	ASSY	12	0.5	1	9	1	0.5
Parts Transfer	Freight Forwarder	1	0	0	1	0	0
TOTAL		**77**					

The expected total length of this prototype flow is: 77 days. **This is a 14 percent improvement achieved by simply implementing the various CTR mechanisms.**

Workflow with Unplanned Exceptions

Conditions: Wafers were mislabeled at Fab-ASSY Transfer. Five days are lost.

Assumptions: Real-time WIP updates enable the problem to be detected early. Only two days are lost.

Result: Without WIP, the expected total length of this prototype flow taking into account delays is: 95 days. The implementation of WIP notifications reduces the expected total length of this prototype flow to: 78 days. **This is an 18 percent improvement in cycle time.**

Summary

This document proposes that WIP tracking mechanisms can effectively reduce cycle time for both prototype / NRE and production flows. A mathematical framework is used to calculate cycle-time reductions in the manufacturing supply chain. An analysis based on very conservative assumptions (typical processing times) derives the following potential cycle time reductions:

WORKFLOW	DURATION	NORMAL OPERATION		UNFORSEEN THINGS HAPPENED	
Prototype	94d	-13d	-14%	-17d	-17%
Production	90d	-13d	-14%	-17d	-18%