Developing the Mid-End Foundry

A Silex Microsystems White Paper

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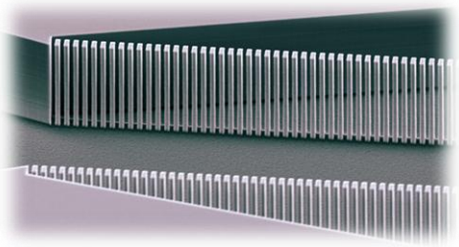
Advances in semiconductor design, manufacture and packaging have defined much of the innovation in modern electronics over the past 40 years. Moore's Law, the observation that circuit density and processing power doubles every 18 months, has progressed from industry anecdote to the status of fundamental force driving the progress of the industry. The industry now has a sophisticated and complex global supply chain in place to support the production of billions of ICs produced yearly, and continues to grow in complexity and scale.

Silex Microsystems was founded in 2000 to service the manufacturing needs of advanced microelectromechanical systems (MEMS) devices. MEMS devices, being based on micromachined, silicon-based structures, inherently have unique manufacturing challenges in bringing ideas to reliable, high volume production. Equally challenging are the tasks of packaging MEMS devices, often in combination with traditional ICs, in a way that meets the stringent quality and reliability requirements of our customers. This has been the engine of new innovations in packaging and manufacture, and Silex, with over 200 successfully completed MEMS projects over its 10-year history, has a portfolio of solutions to service its customers' critical needs. With fully production qualified 150mm and 200mm lines and proven MEMS manufacturing and wafer level packaging capabilities, it has grown to be the largest pure-play MEMS foundry in the world.



Advanced MEMS fabricated at Silex

The IC world and MEMS world have co-existed for the past many years, with separate and independent foundry operations often only combined

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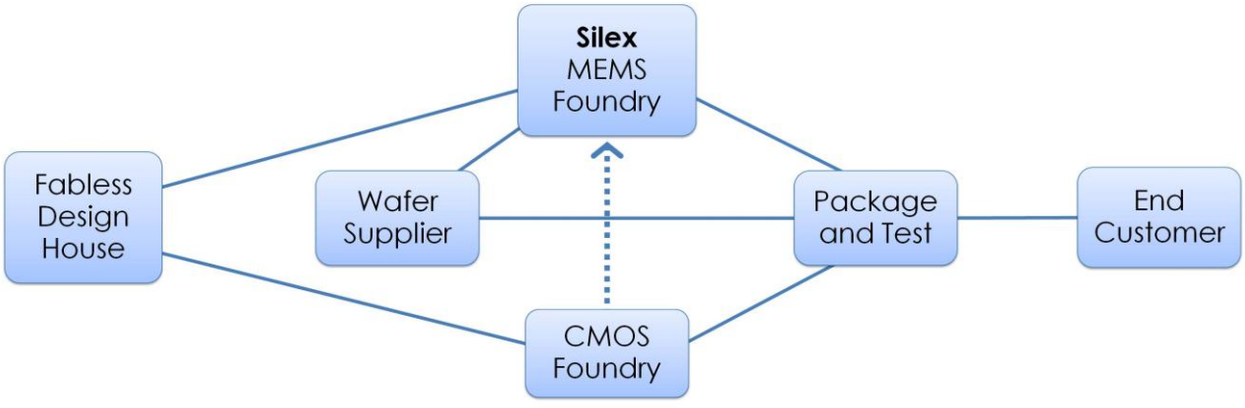
at the package or module level. Year by year, however, the challenges of keeping up with Moore's Law grow larger, and the pressure for higher processing power and functionality in smaller footprint is making the industry search for new solutions.

3D packaging is emerging as the most hopeful candidate. Covering a wide range of technologies, 3D ICs are generally stacked die solutions combining multiple chips in a single package using either stacked wirebond, flip chip, through-silicon vias (TSV), silicon interposers, or a combination of these solutions. While primarily seeing microprocessor unit (MPU) or system-on-a-chip (SoC) flip-chip solutions for mobile processing needs, in reality many functions from RF to power to sensors are already incorporating these same solutions to meet the functionality per unit area challenges.

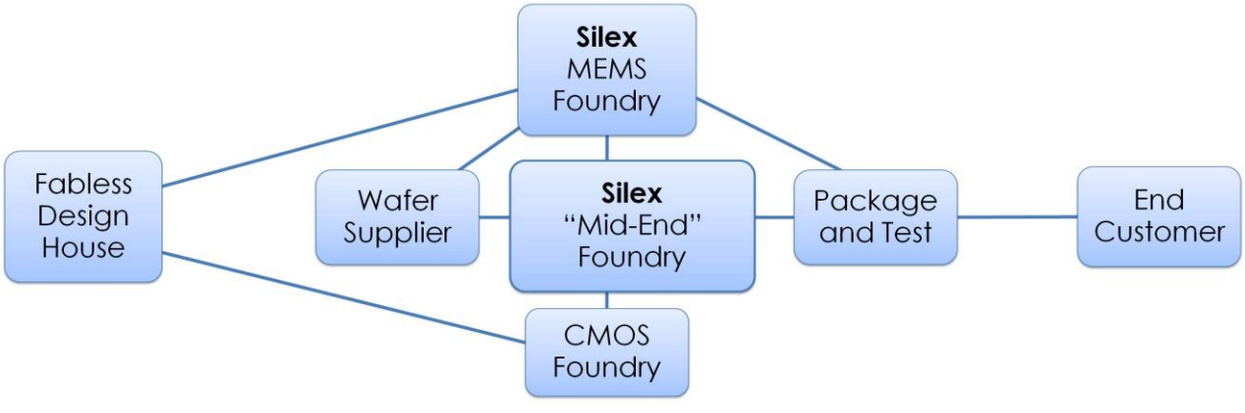
However, executing on these technologies requires new capabilities for processing at the wafer level, something neither the traditional CMOS foundries nor packaging houses can generally offer. The search for these solutions has turned to MEMS foundries like Silex, to leverage off of our extensive technologies and experiences in providing these same solutions for our MEMS customers. Not purely front-end, and not exclusively back-end, a new category of "Mid-End Foundry" is emerging in the marketplace, a category which Silex is ready to service.

The Emergence of Mid-End

Due to the different and unique processing requirements for MEMS and ICs, the traditional supply chain uses parallel paths for component manufacture, often with separate supporting infrastructure requirements such as CAD, simulation or layout. Wafer level preparations at the MEMS foundry prepare the component for traditional packaging and test, often taking the completed CMOS wafer and combining into a single component (wafer level packaging, or WLP.)

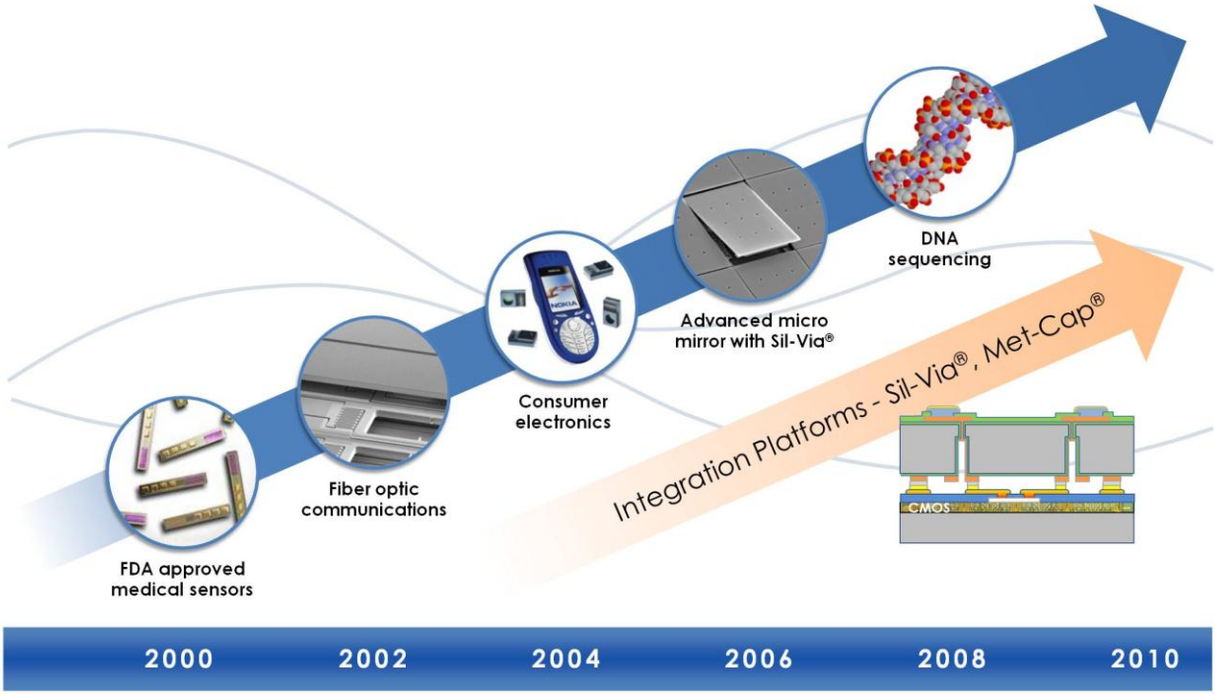


3D packaging technologies require wafer level processing prior to delivery to the packaging house, technologies that traditional CMOS foundries often lack. MEMS foundries, however, have an inherent competency in these processes, especially low temperature wafer level bonding, high reliability TSVs, thick metal plating, high vacuum processing and environmental hermeticity. And while much of the advanced MPU and SoC work is being done at 300mm moving to 450mm, nearly 40% of all wafer production is still at 200mm and below (source: WSTS). This area, with Silex' 150mm and 200mm production capability, is where the Mid-End Foundry emerges.



Silex Microsystems Experience in 3D Packaging

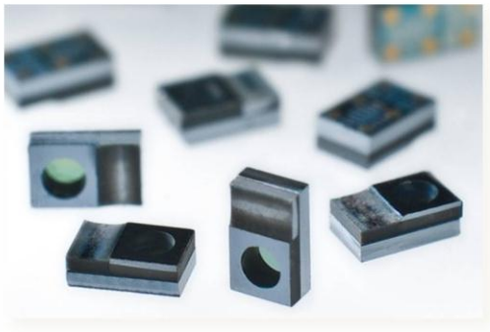
Silex was founded in 2000 to serve as the manufacturing partner for the world's leading MEMS companies. Starting with BioMEMS, the company quickly expanded to service MEMS needs across the application spectrum, and to date has completed over 200 MEMS projects.



Silex' work with 3D integration platforms began in 2003

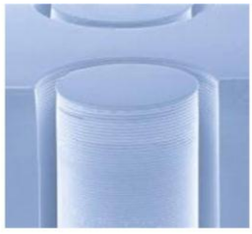
Early commercialization of MEMS devices was often complicated by the constant need for customized and expensive packaging and interconnect solutions. Silex' Sil-Via® process was initiated as a core module capability by Silex to address this recurring need.

Our Sil-Via solution, the industry standard in all-silicon full wafer thickness through vias, began development in 2003 to support an advanced MEMS microphone for mobile phone applications. Volume production began in 2006, ramping to 2000 6" wafers per month. Sil-Via thru-Silicon vias (TSV) have been in volume production at Silex continuously for the past five years.



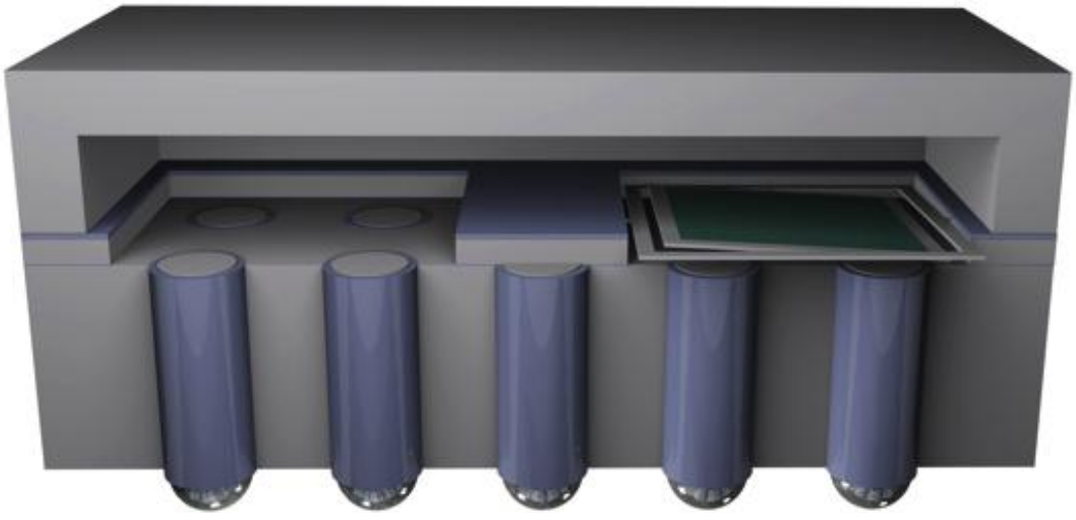
Microphones for mobile telephones

It uses low-ohmic substrates and advanced MEMS DRIE processing to create all silicon pillars, or vias, through the silicon substrate. These vias are then backfilled with oxide to provide fully isolated vias with TeraOhm level integrity.



Sil-Via® DRIE process

When combined with hermetic wafer bonding with embedded cavities, a complete packaging solution for MEMS structures is realized which maximizes functionality and reliability and minimizes component footprint.

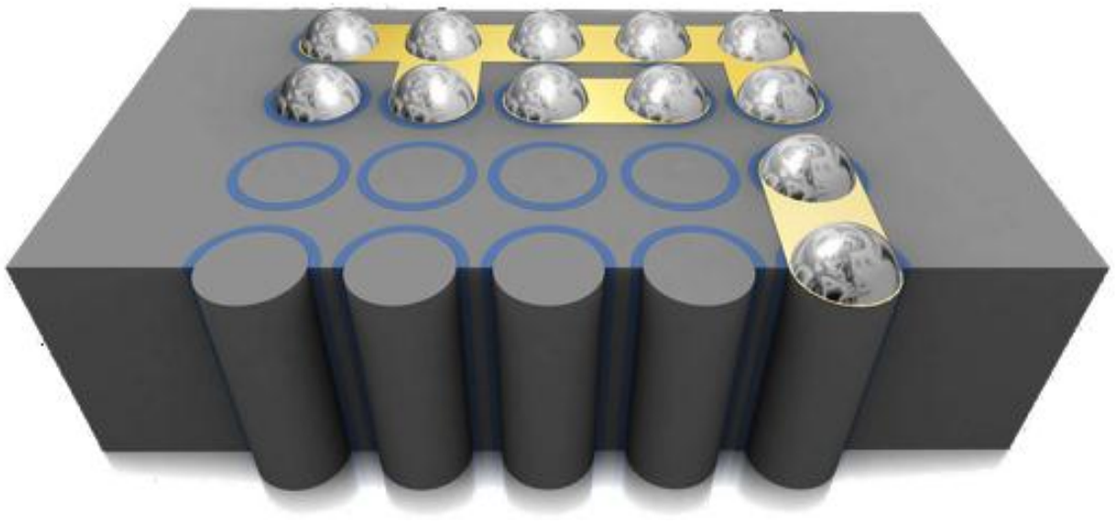


Sil-Via® Through-Silicon Via integration in MEMS with hermetic wafer cap

To date, Silex has implemented Sil-Via TSVs on over a dozen projects, including microphones, accelerometers, flow sensors, gyros, IC interposers, Lab-on-Chips, micromirrors, optical benches, pressure sensors, print heads, resonators and micro batteries. This track record makes Sil-Via vias the industry benchmark for production TSVs for MEMS applications.

Silicon Interposer Solutions enabled by Sil-Via technology

When combining MEMS to ICs, or when seeking to combine different ICs vertically in a single package, topographical challenges often arise. Quite commonly, bond pads and TSVs do not line up due to active area or physical size constraints, and power and signal bussing may be required on top of actual pad connections. A silicon interposer resolves these challenges by providing structural strength, redistribution layer (RDL) flexibility, and two-sided bump and route capability.



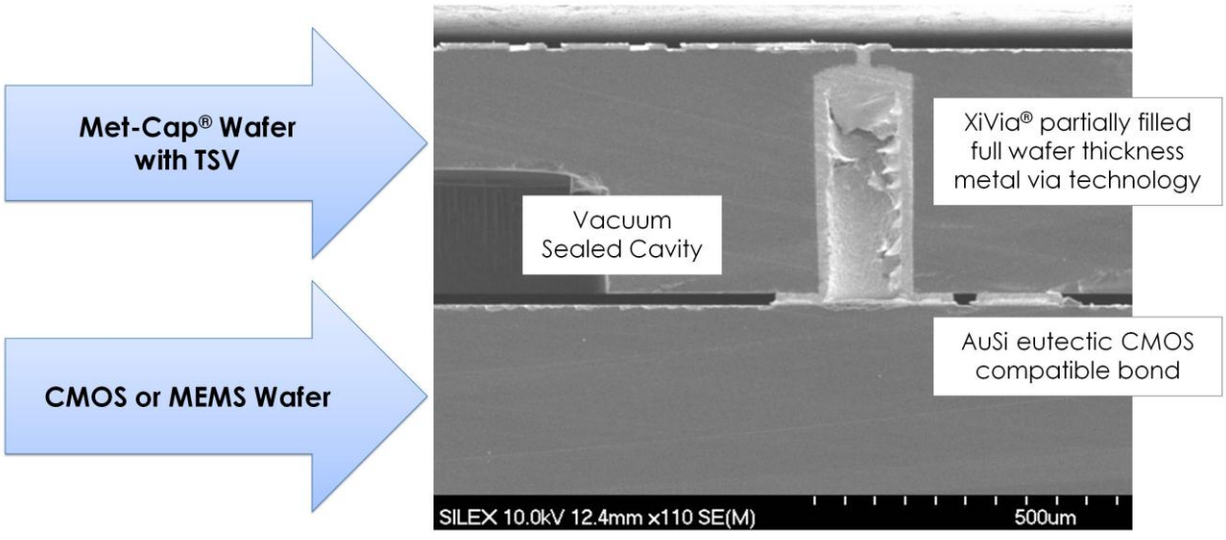
Silicon Interposers incorporating Sil-Via TSVs enables high density 3D IO routing

Silex' Sil-Via technology enables highly flexible Silicon Interposer solutions for 150mm and 200mm needs. Wafer thickness from 300mm to 600mm can be manufactured, and Sil-Via pitches down to 50 µm mean high density support for I/O intensive ASICs. Isolation of via to substrate exceeds one TeraOhm, making for perfect low resistance, zero leakage TSV vias.

Other 3D Integration Solutions from Silex

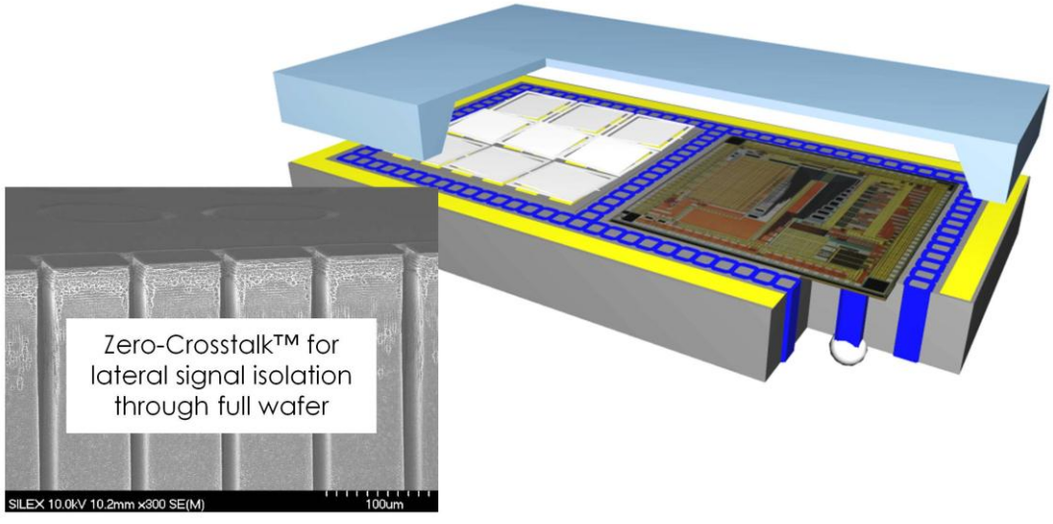
Bonding silicon to silicon while maintaining connectivity to the underlying circuits and ensuring seal integrity is a critical requirement of CMOS-to-MEMS packaging. Silicon wafers with etched cavities are designed to provide wafer level packaging without impeding or contaminating the MEMS structure underneath. Connectivity must be provided through TSVs and, since completed CMOS wafers are used in the packaging process, the wafer bonding must be 100% CMOS compatible.

To meet these challenges, Silex has developed its Met-Cap® metal via based integration platform. A partially filled full wafer thickness metal via is combined with a fully CMOS compatible AuSi eutectic wafer bond for the complete wafer level solution. Total via resistance from front side to back side of wafer is below 20 mOhm.



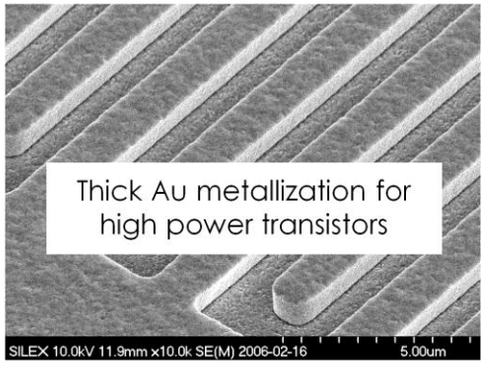
Silex "Mid-End" processing options for CMOS foundries and IDMs – today's reality, tomorrow's promise

The underlying processing capability which makes Sil-Via TSVs possible also enable novel "2D" integration options for CMOS foundries and IDMs. By extending the Sil-Via concept into a chain of vias with common isolation walls, Silex has created fully dielectrically isolated SOI capabilities for CMOS circuit processing. Named Zero-Crosstalk™ preparation, it creates completely isolated active areas and can integrate Sil-Via TSVs during the same process. The resulting substrate is fully CMOS compatible and can withstand wafer processing up to 1100°C.



Zero-Crosstalk prepared substrates mean CMOS designs can have completely electrically isolated areas separated by isolation barriers of less than 100 µm. This allows potentially interfering circuit blocks like RF, power, and signal processing to be fabricated on the same chip. Similarly, high voltage IOs and low voltage cores can be co-located without performance or size penalties by trying to combine within the same design environment.

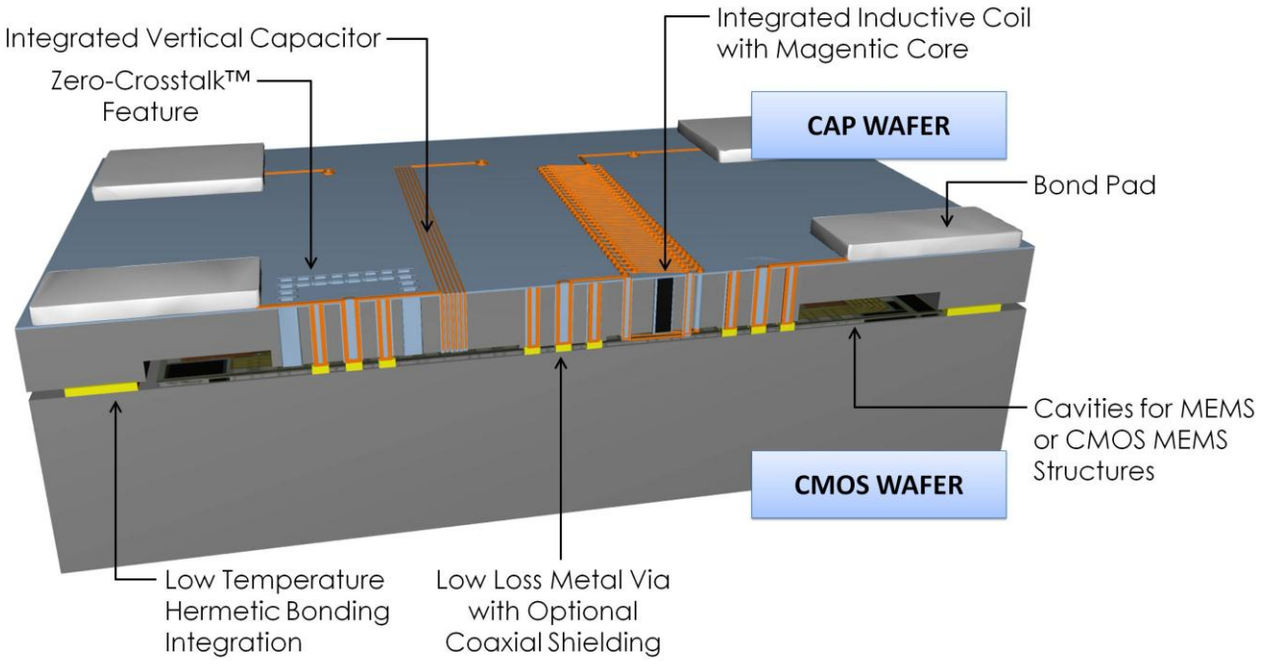
Gold metallization gives high power ICs advantages in low resistance, high current carrying capabilities. Gold, however, is a highly mobile heavy metal contaminant in normal CMOS processing and as a result most CMOS foundries will not allow gold processing in their fabs. Silex has a well controlled environment for gold electroplating and this ability to post-process thick plates onto finished CMOS wafers is another facet of Silex' migration into the Mid-End Foundry space.



What "Moore" can MEMS do for CMOS?

The combination of MEMS unique capabilities with the integration needs of advanced ICs opens the door for new packaging capabilities to be exploited.

"Functional Capping" is a term we use to describe this evolution – when bypass, RF and signal conditioning passives can be integrated into the wafer cap, higher levels of functionality and integration are achieved within the same footprint. The ability to combine with metal or silicon vias, cavities for embedded MEMS devices, highly hermetic wafer seals, and active area islands enabled by Zero-Crosstalk preparation all mean that tomorrow's integrated package solutions can truly be called Systems on a Chip.



System on a Chip package level integration enabled by Silex technologies

About Silex

Silex Microsystems is the world's largest pure-play MEMS foundry that services the advanced MEMS and packaging needs of the world's leading companies.. With production operations totaling 25,000 square feet with dedicated lines for both 6" and 8" wafers, Silex has successfully completed over 200 MEMS projects with over 80 corporate customers. Silex' Sil-Via® has provided advanced TSV solutions for over 5 years. Silex' core technologies enable some of the world's brightest innovations. For more information, please visit www.silexmicrosystems.com.