Wake-Up and Verify (WAV) Data Sheet

Proven System Block (PSB) for QuickLogic Customer Specific Standard Products (CSSPs)

Features

The QuickLogic WAV PSB has the following features:

- Allows for detection of changes of state of external devices (keyboards, headphones, etc.) and internal devices (sliders) while the CPU is in a power-down state
- CPU remains in a low power state during detection, greatly reducing system-level power consumption

Overview

System architects must constantly balance the requirements for system performance against system power. This is often a fine balance, which becomes more complicated when the system must manage external devices connecting into the architecture at random and infrequent periods. Devices such as external keyboards, headphone jacks, and computers are typical features consumers connect to their mobile devices to extend functionality.

The issue facing designers is how they can detect these activities while making sure minimal power is consumed waiting for this activity. This system requirement is not restricted to external devices, but also for internal connectivity within a mobile device. This includes functionality typically involving the CPU such as detection of slider motion, keypad or touch press and sensor activities.

QuickLogic has developed a new PSB which enables detection of activities on a bus or signal while the system is in a power down state. This implementation can consume fewer than 5 µA of current while it monitors activities and detects when to wake up the system or part of the system to act upon. When this PSB is used in conjunction with other PSBs to build a CSSP, the solution can be used to detect, act upon and inform various aspects of the system - enabling a more efficient solution for the management of active and standby power during specific application tasks, resulting in much longer battery life.

The WAV PSB is available for inclusion in QuickLogic CSSPs using the ArcticLink®, ArcticLink II, PolarPro® and PolarPro II solution platforms.

PSB Architecture

Wake-Up and Sleep Logic

The Wake-Up and Sleep Logic contains the necessary logic to put the CSSP into sleep mode or to wake up the CSSP from Sleep mode.

The CSSP enters Sleep mode when the external *Sleep* signal is set high. To bring the CSSP out of Sleep mode, the *Sleep* signal must be reset to low and the *Wake_En* signal must be set high. Once these conditions are met and the CSSP detects a rising-edge *Wake* signal, the *Logic_Pwr* pin will be set to 1.8 V, which turns on the logic voltage (Vcc).

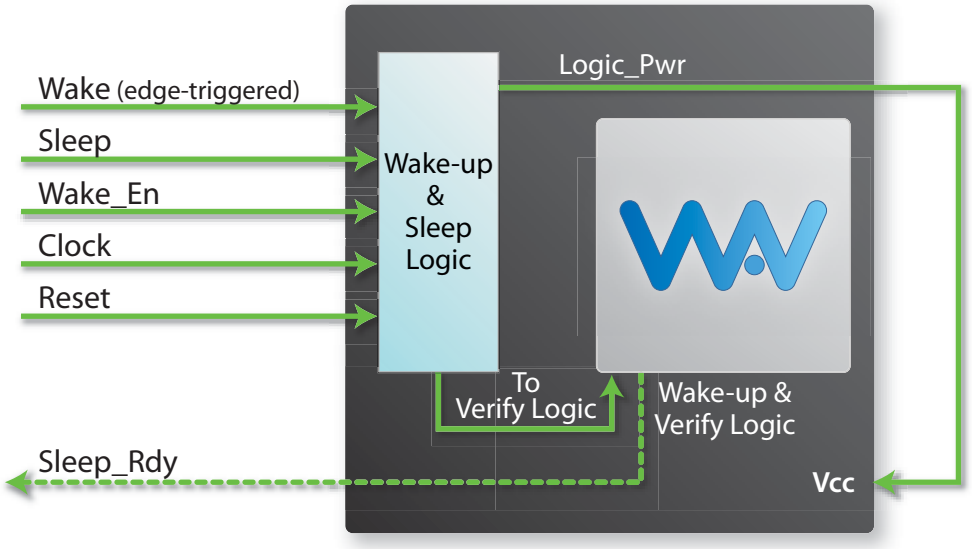
Wake-Up Verify Logic (Optional)

The Wake-Up and Verify Logic is optional but recommended when coming out of Sleep mode. Although the module must be tailored for the application, the basic implementation is the same.

The purpose of this module is to bring the CSSP out of Sleep mode into a previous known state. By storing values in the CSSP embedded RAM blocks, logic states (e.g., state machine states) can be retrieved upon wake-up and set to values that existed prior to entering Sleep mode.

Figure 1 shows a system level block diagram of the WAV PSB.

Figure 1: WAV PSB System Level Block Diagram

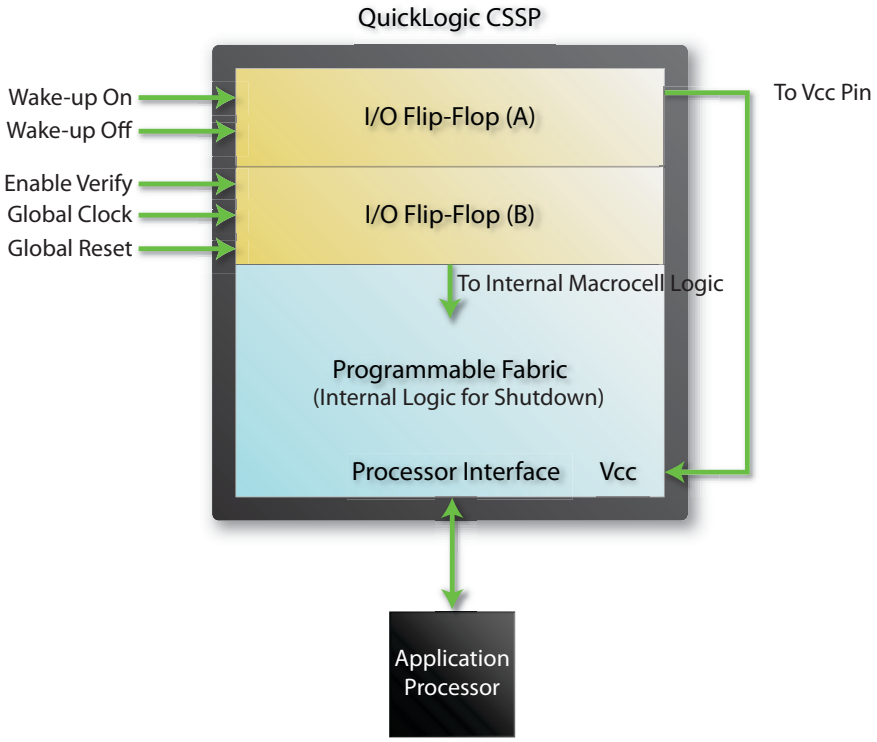


Functional and Module Description

The WAV PSB consists of the following functional blocks as shown in **Figure 2**.

- **I/O flip-flop (A)** — Controls the power to the core voltage. This requires dedicated external D-input, output, clock and reset pins.
- **I/O flip-flop (B)** — Controls the external request to shut off the core voltage. This flip-flop uses the global reset and clock signals.
- **Processor interface** — Communicates to the Host bus. It is responsible for decoding the local address of the transfer, and steering the transaction to the CSSP registers, internal SRAM, peripheral buses, or the USB Controller. Local bus byte lanes are assumed to be enabled at all times.

Figure 2: WAV PSB Block Diagram



Interface List and Description

Table 1 summarizes the WAV PSB interface signals.

Table 1: Pin Descriptions

Pin	Type[a]	I/O Rail Voltage	Description
General Signals			
Clock	I	1.8 V – 3.3 V	Global system clock.
Reset	I	1.8 V – 3.3	Global system reset.
Wake	I	1.8 V – 3.3 V	Activates power to internal logic. Used in conjunction with *Wake_En*.
Wake_En	I	1.8 V – 3.3 V	Enables logic to enter low power Sleep mode. Used in conjunction with Wake mode.
Sleep_Rdy	O	1.8 V – 3.3 V	Optional. Denotes that the CSSP can be placed into Sleep mode.
Logic_Pwr	O	1.8 V	Power to Vcc pin (i.e., logic voltage).
Sleep	I	1.8 V – 3.3 V	Puts logic into low power Sleep mode.
Vcc	Pwr	1.8 V	Logic voltage.

a. I = Input
O = Output
Pwr = Power

Power Consumption

Figure 3 shows an example test design.

Figure 3: Test Design Block Diagram

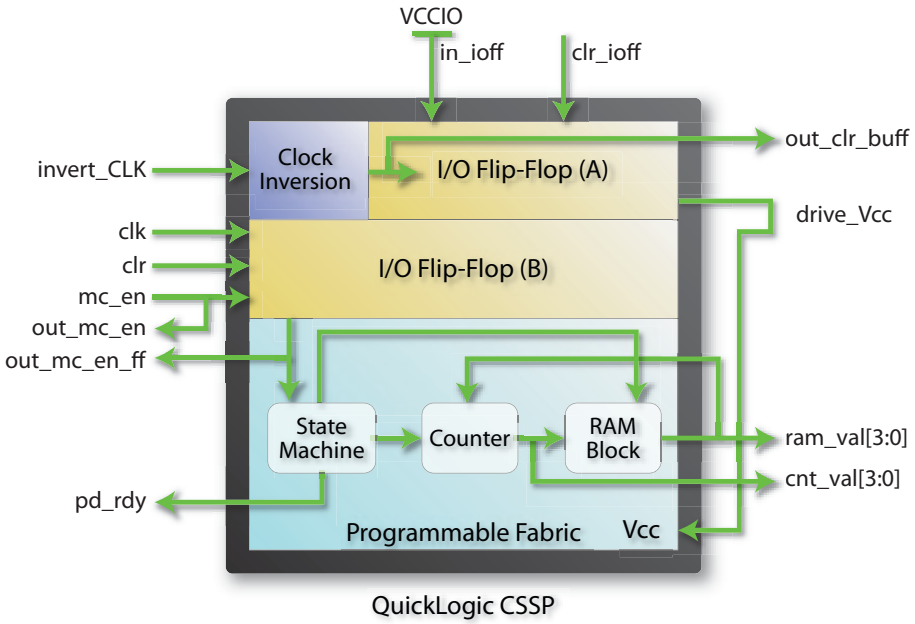


Table 2 summarizes the test design pin descriptions.

Table 2: Test Design Pin Descriptions

Pin	Type	Description
VCCIO	I	Input voltage tolerance pin.
clk	I	The external global clock signal for the CSSP logic. It does not clock the dedicated I/O flip-flop that controls *drive_Vcc*.
clr	I	The external global reset signal for the CSSP logic. It does not control the reset of the dedicated I/O flip-flop that controls *drive_Vcc*.
clk_ioff		Clocked value of *in_ioff* on the falling-edge of *invert_CLK*.
clr_ioff	I	Clear signal for *drive_Vcc* and is connected to the CLR input of the dedicated I/O flip-flop. When high, voltage to the internal logic is shut off. When low, *invert_CLK* is enabled to turn on power to the CSSP core.
cnt_val[3:0]	O	Lower four bits of the test counter.
drive_Vcc	O	Drives the voltage to the core and is connected to the dedicated I/O flip-flop output.
in_ioff	I	*drive_Vcc* is the clocked value of *in_ioff* on the falling-edge of *invert_clk*. Tie high to VCCIO.

Table 2: Test Design Pin Descriptions *(Continued)*

Pin	Type	Description
invert_CLK	I	On its falling-edge, turns power on to the CSSP macrocell logic. The CSSP inverts this signal internally and sends it to the clock input of the I/O flip-flop controlling the CSSP macrocell power.
mc_en	I	The macrocell-enable signal and D-input to one of the dedicated I/O flip-flops. When high, this notifies the CSSP that the internal logic is enabled. When low, this signals to the CSSP to prepare for shutdown.
out_clr_buff	O	Buffered version of *clr_ioff*.
out_inv_clk	O	Inverted version of *invert_CLK*.
out_mc_en	O	Buffered version of *mc_en*.
out_mc_en_ff	O	Clocked (by *clk*) version of *mc_en*.
pd_rdy	O	Indicates that the CSSP is ready for power-down of core.
ram_val[3:0]	O	Lower four bits of the RAM block.

The test design resulted in the following power measurements:

Conditions:

- clk 50 kHz, free-running
- VCCIO (all) 3.3 V
- VDD 1.8 V
- Vcc 1.8 V

Table 3: PolarPro II WLCSP-64 System Board

Vcc (Macrocell Voltage) = Hi (ON)					
Dynamic Power			Static Power		
	Vpump = Lo	Vpump = Hi		Vpump = Lo	Vpump = Hi
$I_{1.8V}$	93.1 µA	14.8 µA	$I_{1.8V}$	85.4 µA	8.4 µA
$I_{V3.3V}$	2.8 µA	3.1 µA	$I_{V3.3V}$	1.0 µA	1.2 µA
Vcc = Lo (OFF)					
Dynamic Power			Static Power		
	Vpump = Lo	Vpump = Hi		Vpump = Lo	Vpump = Hi
$I_{1.8V}$	84.6 µA	7.2 µA	$I_{1.8V}$	80.5 µA	2.6 µA
$I_{V3.3V}$	1.2 µA	1.3 µA	$I_{V3.3V}$	1.0 µA	1.2 µA

The power savings when the macrocell logic voltage is off is minimal. This may have been due to the small size of the test design. If necessary, additional logic can be added to determine the power savings on larger designs.

NOTE: For maximum power savings, tie the CSSP Vpump pin to a 3.3 V source.

Supported Operating Systems

The WAV PSB supports the following operating systems:

- Windows® CE
- Windows Mobile®
- Linux®
- Android®

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Revision History

Revision	Date	Originator and Comments
A	July 2010	Andy Green, Paul Karazuba and Kathleen Bylsma

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