eSilicon's Networking-Centric 14LPP IP Platform

Physical IP, Ternary CAM, High-Bandwidth Memory and 2.5D

Is your chip hot? Need more bandwidth? eSilicon has complete physical IP and 2.5D high-bandwidth memory solutions on Samsung's 14LPP technology including high-performance, high-bandwidth networking-centric memory compilers, TCAM, HBM2 PHY, and extended voltage GPIO.

For complete data sheets, contact ipbu@esilicon.com or log on to https://star.esilicon.com.

Introduction

With the increasing number of Internet-connected consumer devices, manufacturing systems, business tools, customer service appliances, medical equipment, agricultural sensors and other devices, the difference between required and available bandwidth will become huge. High-speed, high-bandwidth networking enables the aggregation, automation and analysis of this data.

eSilicon offers a set of high-performance and high-bandwidth IP and 2.5D solutions that target networking and high-performance computing applications by offering 2.5GHz caches (worst-case operation) and TCAMs with more than a billion searches per second along with the 2.5D integration of 1024 Gbytes/sec data rate high-bandwidth memory (HBM2).

14LPP Networking and High-Performance Computing IP Platform

The silicon-proven 14LPP Networking and High-Performance Computing IP platform is available now. This IP platform has been designed specifically to meet the high speed and bandwidth requirements of ASICs and ASSPs targeted for networking and high-performance computing applications. The platform includes the following IP:

- High-speed and ultra-high-speed single-port ternary CAM compiler (SP TCAM)
- High-speed and ultra-high-speed pseudo two-port (P2P) SRAM compiler
- High-speed dual-port (DP) SRAM compiler
- High-speed single-port fast cache (SP FC) compiler
- High-density two-port asynchronous register file (2PARF) compiler
- High-density pseudo two-port (P2P) SRAM compiler1.8V oxide 1.8V/2.5V/3.3V general-purpose I/O library
- 1.8V oxide 1.8V LVDSOUT I/O library
- 1024 bit HBM2 PHY

Why TCAM?

Memory processing tends to be the bottleneck in network performance. If memory cannot keep up with increasingly fast processors, the processors have to wait, stalling the system. Specialty memories address the problem in a variety of ways. Ternary content-addressable memories (TCAMs) are unique — they search an entire lookup table in one cycle. eSilicon's eFlexCAM™ TCAM compiler provides up to 2.5 billion search results in one second (BSPS), enabling high-efficiency, cost-effective solutions for applications such as network search engines, cache for network processors, QoS services, classifications, Ethernet, ATM switches and other diverse networking applications.

TCAM Standard Features

- Flexible selection of width and depth – compiler based with up to 160Kb compiled and up to 40Mb cascading table size
- Easily cascadable to increase search depth without degradation in performance
- Single-cycle Compare operation
- Fast cycle and access time: 1.2 BSPS worst case and up to 2.5 BSPS under typical conditions
- Smart Power Management with valid-bit, match-in and partial pipeline search
- Global and local valid-bit reset
- Match, Hit, Multi-hit flags compile-time option
- Match-in lines
- Priority encoder compile-time option
- Redundancy
- Patented Duo architecture may be licensed for reduced area and power savings for bit widths less than or equal to 80 bits

High-Bandwidth Memory

HBM2 achieves higher bandwidth while consuming less power in a substantially smaller form factor than DDR4, GDDR5 or hybrid memory cube (HMC). This technology addresses the bandwidth gap with 1024 Gbytes/sec data rate with four HBM stacks in a package. HBM has eight independent channels using a total of 1024 input and output pins. This density of signals, coupled with interposer design, requires careful design and thorough timing analysis. eSilicon has designed IP and systems in package (SiP), manufactured, assembled and tested systems that include HBM2.

HBM2 PHY

The HBM2 PHY is JEDEC JESD 235B compliant. The PHY supports up to 256Gbytes/sec bandwidth with 8x128b channels at 2Gbps per I/O. The PHY is DFI 4.0 compliant with several controller-independent features such as:

- **Plug & play:** with hard macro and built-in clock control there's no lengthy timing closure and physical design
- **Custom design** for optimized timing and area
- Rich set of **built-in features**
- **Flexible**: minimum dependence on controller features
- **Signal integrity:** custom routing scheme used on interposer to significantly minimize crosstalk and skew
- **Maximum timing margin:** PHY includes training, calibration and VREF programmability features
- **DFI and IEEE1500 compliant**
- **APB interface** enables CPU override of built-in training, repair and calibration

About eSilicon Memory IP and Customization

eSilicon's 14LPP eFlex™ memories provide system-on-chip (SoC) architects with a reliable, affordable method of optimizing their product design. eSilicon optimizes its networking-centric memory compilers by leveraging ASIC system-level requirements for high bandwidth for optimal power, performance or area.

Our IP team has been a leading provider of high-quality memory IP since 2000. eFlex memories are available in silicon-proven 14nm-250nm technologies, customized to meet challenging PPA requirements for leading foundry and integrated device manufacturer (IDM) processes.

Contact and Online Access

Please contact eSilicon at ipbu@esilicon.com for more information, silicon quality results, white papers or complete data sheets. All eSilicon IP is available in Navigator at https://star.esilicon.com.

Product Name	Key Feature	Foundry Sponsored	eSilicon Licensed	Front-End Design Kit	Back-End Design Kit	Silicon Report
High-Speed SP TCAM	1.2GHz	X		Available	Available	Available
Ultra-High-Speed SP TCAM	1.5GHz		X	Available	Available	Jul-17
High-Speed SP Fast Cache	2.5GHz	X		Available	Available	Available
High-Speed DP SRAM		X		Available	Available	Available
High-Speed Pseudo 2-Port SRAM	1.2GHz	X		Available	Available	Available
High-Density Pseudo 2-Port SRAM			X	Available	Available	Available
High-Density 2-Port Asynchronous RF	Async READ		X	Available	Available	Available
Ultra-High-Speed Pseudo 2-Port SRAM	1.5GHz		X	Available	Mar-17	Jul-17
High-Speed Four-Port Register File			X	Available	Aug-17	NP
1.8V oxide 1.8V/2.5V/3.3V general-purpose I/O library		X		Available	Available	Available
1.8V oxide 1.8V LVDSOUT I/O library			X	Available	Available	Available
1024 bit HBM2 PHY	2Gbps per bit		X	Available	Available	Available

QUALITY SYSTEM CERTIFICATION
DNV·GL
ISO 9001