FOUNDRY LEADERSHIP FOR THE SoC GENERATION

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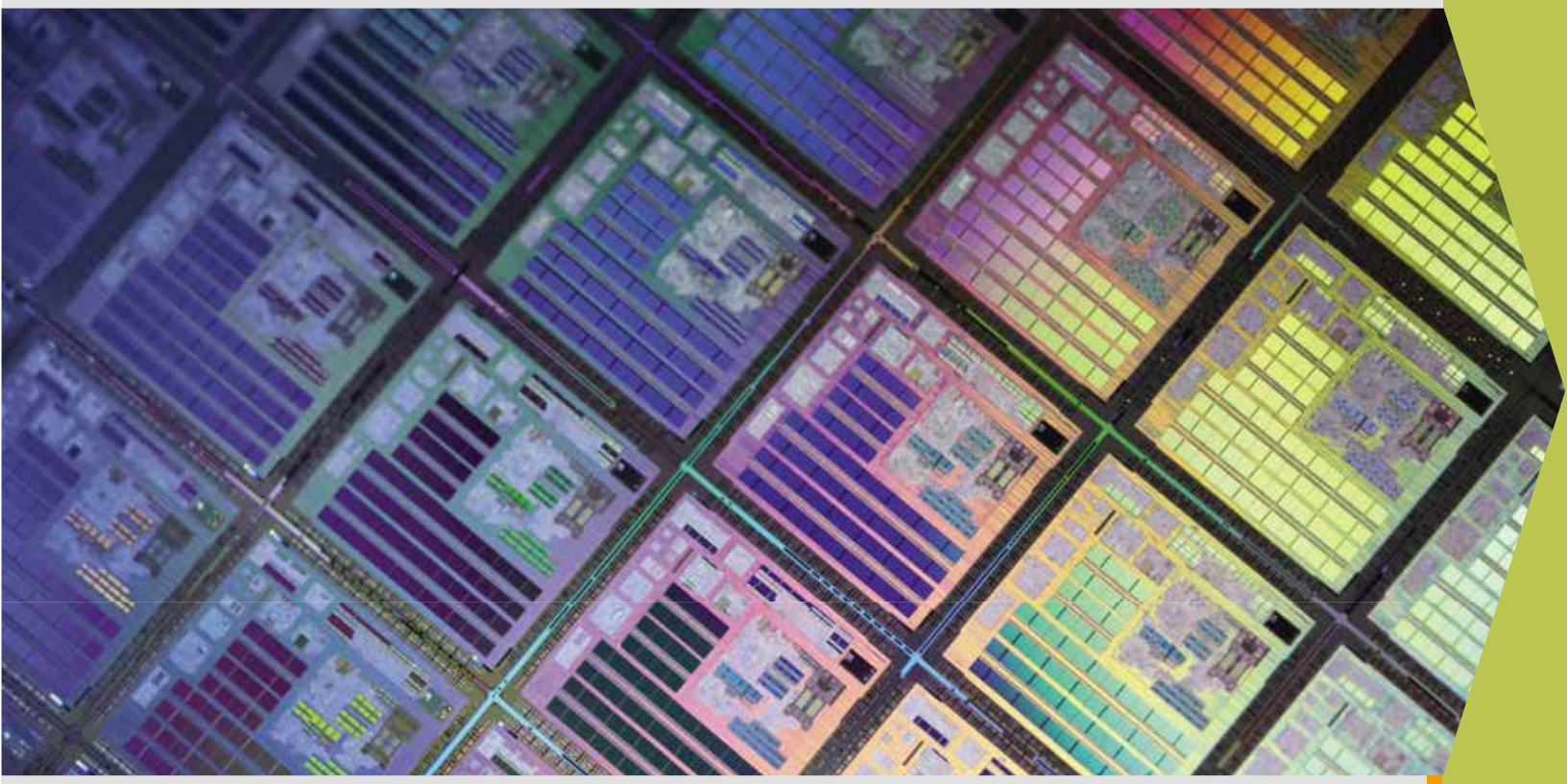
28

28 Nanometer

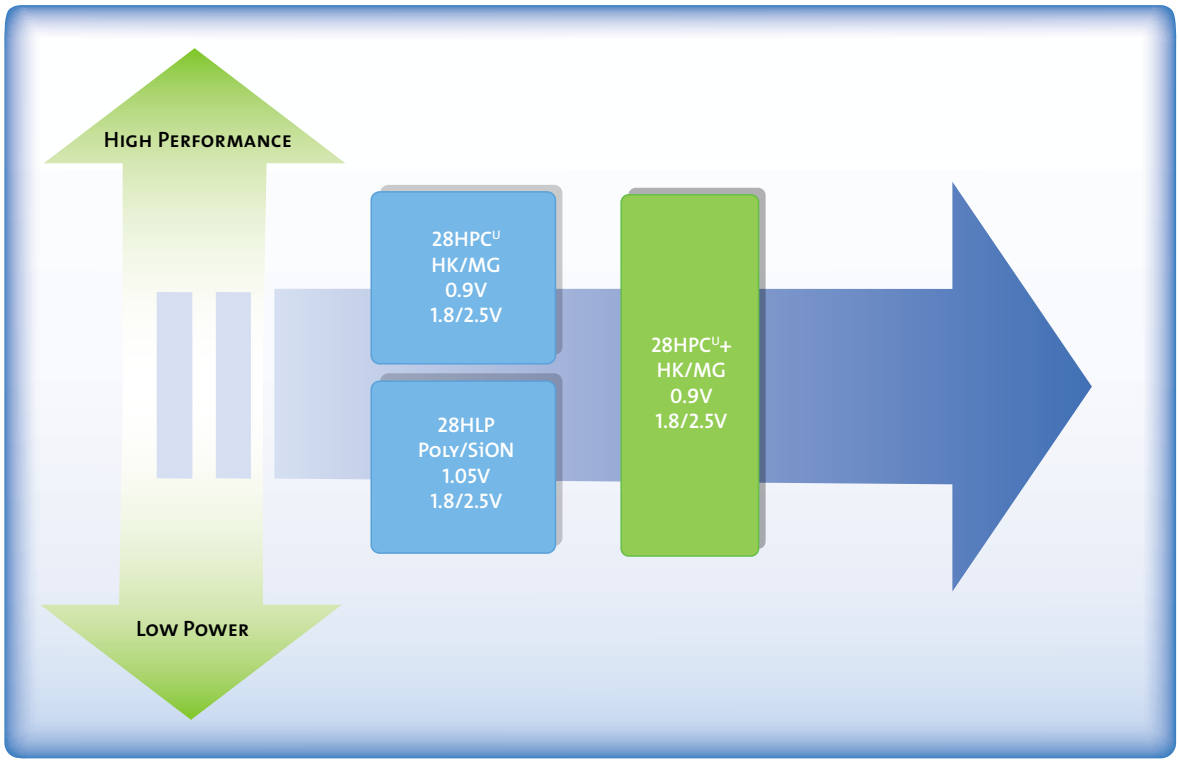


UMC

28 Nanometer

UMC's 28nm process technology is developed for applications that require the highest performance with the lowest power leakage. In October 2008, we were the first foundry to deliver fully functional 28nm SRAM chips and have proven in silicon the high-K/metal gate technology used for this technology node. Our 28nm platform is based on industry mainstream technology that includes conventional poly/oxynitride process and gate last, high-K metal gate, which provides superior performance over gate first high-k offerings. Currently, our 28nm is in volume production for several customer products.

Advanced Technology Roadmap



Value and Performance Driven 28nm Technology

Our 28nm process technology uses new stress techniques (SMT, t-CESL, c-CESL) and embedded SiGe to enhance electron mobility performance, and is ideal for applications that require high performance and low power consumption. We are currently in volume production for multiple customer products on both UMC's 28HLP SiON and 28HPC^{U} High-K-Metal Gate processes. UMC is aggressively adding 28nm capacity to meet the high customer demand for this popular process technology.

28HLP - with enhanced SiON

UMC's 28nm High Performance Low Power (28HLP) process provides a natural migration from 40nm with easy adoption, fast-time-to-market, and a very favorable performance / cost ratio. UMC's SiON solution delivers vastly improved performance and power consumption for customers demanding more speed for their particular application, with a 10% speed increase and 28% lower IDDQ over other 28nm SiON industry offerings.

28HPC^{U} - with High-k/metal gate stack

UMC's 28nm High-k/metal gate stack (28HPCU) supports broad device options for increased flexibility and performance requirements, targeting a wide range of products such as application processor, WLAN, Tablet, FPGA and Networking ICs. The High-k-/metal gate stack and abundant options for device voltages, memory bit-cells and under drive/overdrive capabilities help SoC designers realize unmatched performance and battery life, with 30% lower IDDQ over other industry offerings.

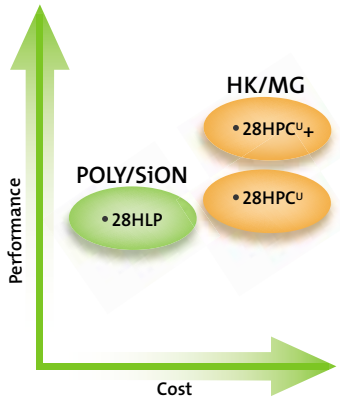
28HPC^{U}

With improved transistors 28HPC^{U}+ can provide 15% boost in performance or 30% lower IDDQ at the same speed. 28HPC^{U}+ targets for high performance SoC, networking, DTV/STB.

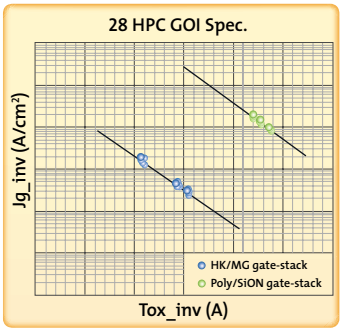
28nm Technology for Broad Applications

Our rich 28nm technology platform and multiple process approach satisfies the rigorous requirements of all major market applications. UMC incorporates multiple approaches for its 28nm technology to address different market applications. The first option is conventional poly-SiON technology used for our High-Performance Low Power (HLP) processes. The HLP process delivers a 10% performance enhancement over the industry standard platform due to process optimization techniques. These platforms are ideal for portable applications and consumer electronics such as mobile phones, wireless ICs and TVs. For applications that require performance enhancement but still maintain low power consumption, a second, High-K/Metal Gate (HK/MG) option is offered on a High Performance Compact for Mobile (HPC) platform. The HPC process is ideal for speed-intensive and power consumption optimization products such as digital TV applications, portable processors and high speed networking.

28nm Platform Cost vs. Performance



HK/MG Technology Benefits



* Based on UMC's internal benchmarking. Actual customer product performance results will vary.

28nm Device Solutions

UMC's 28-nanometer solution features a flexible technology design platform. Customers can choose the process device options optimized for their specific application, such as HLP, HPC^{U}, HPC^{U}+ transistors with their multiple Vt options.

L28 Device Offering

Platform Offering		HLP	HPC^{U}	HPC^{U}+
Core Vcc (V)		1.05	0.9	0.9
Vt Options	Ultra -Low		√	√
	Low	√	√	√
	Regular	√	√	√
	High	√	√	√
	Ultra - High		√	√
	Extra - High			√
1.8V IO	1.8V UD 1.2V		√	√
	1.8V UD 1.5V	√	√	√
	1.8V	√	√	√
2.5V IO	2.5V UD 1.8V	√	√	√
	2.5V	√	√	√
	2.5V OD 3.3V	√	√	√
SRAM	SP	√	√	√
	DP	√	√	√
Mixed Signal Devices		Native Vt / LDMOS / Bipolar / Diode / Varactor / Resistor / MOM / Inductor		

IP Support

Fundamental IPs (standard cells, I/Os, and memory compilers listed below) are optimized to UMC technologies, and are planned for development from several leading vendors to be available free-of-charge (please contact a UMC account manager for more information). Customers can also leverage application specific IPs for DTV, graphics, networking, etc. IPs available through UMC are DFM (Design for Manufacturing) compliant for better manufacturability.

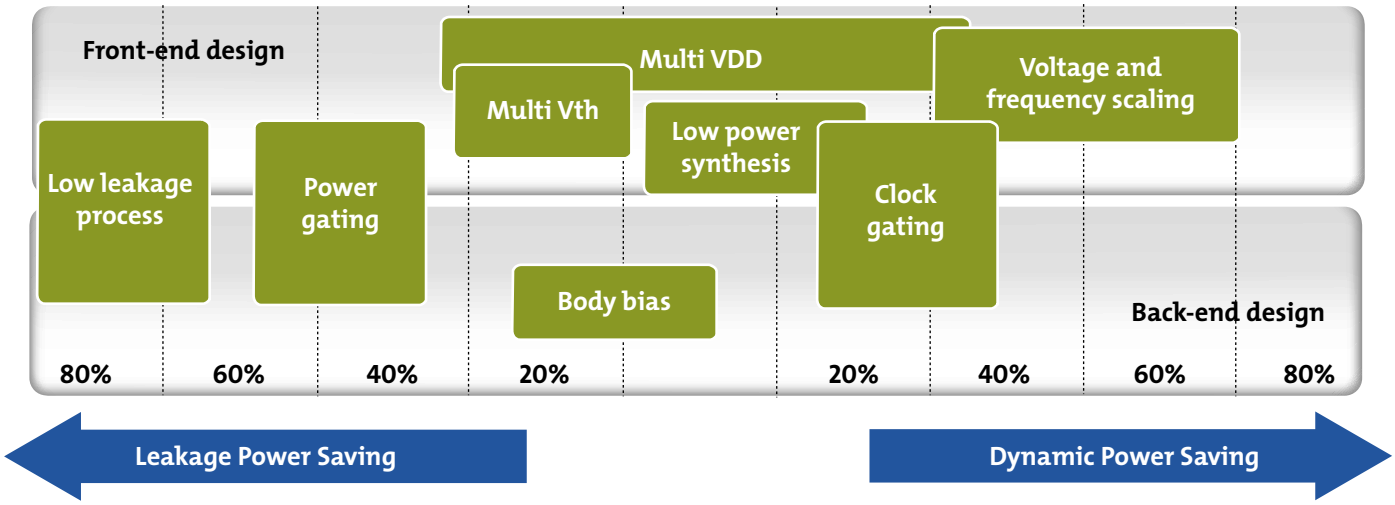
Fundamental IP, HLP, HPC^{U}, HPC^{U}+	Interface/functional IP, HLP	Interface/functional IP, HPC^{U}	Interface/functional IP, HPC^{U}+
Multi-voltage Standard Cell Library	USB2.0, USB3.0, HSIC	USB2.0, USB3.1 Gen1	USB2.0, USB3.1 Gen1/Gen2
1.8V IO Library	MIPI D-PHY, M-PHY	MIPI D-PHY, M-PHY	MIPI D-PHY TX, RX
2.5V IO Library	PCIE Gen2	PCIE Gen3	PCIE Gen2, Gen3
eFuse 32b~4Kb	DDR Multi-PHY DDR3/2, LPDDR3/2	DDR Multi-PHY DDR4/3, LPDDR3, LPDDR 4	DDR Multi-PHY DDR4/3, LPDDR4/3
Single Port SRAM Compiler	DDR Multi-PHY DDR4/3, LPDDR3	HDMI 2.0 TX	SATA 3
Dual Port SRAM Compiler	HDMI 2.0 TX	SATA 3	Ethernet, Serdes 12.5G
Single Port Register File	OTP 16kb~128kb	Serdes 12.5G	V-By-One 4Gbps
Dual Port Register File	General Purpose PLL with variable input/output frequency ranges	Speciality IO	OTP 16kb~128kb
ROM Compiler	Clock Generator PLL with variable input/output frequency ranges	OTP 16kb~128kb	Pipeline ADC
	SSCG PLL with variable input/ output frequency ranges	General Purpose PLL with variable input/output frequency ranges	
	Deskew PLL with variable input/ output frequency ranges	Clock Generator PLL with variable input/output frequency ranges	
	DDR DLL	SSCG PLL with variable input/ output frequency ranges	
		Deskew PLL with variable input/ output frequency ranges	
		DDR DLL	
		High Freq/ Low Freq OSC IO	

Low Power Features of Standard Cell Library

With today's proliferation of low power applications, lowering energy consumption without sacrificing performance has become a critical concern for designers of power management chips for portable electronics. UMC supports its standard cell library with low power design features, including multiple Vt, clock-gating, level shifter and other features to complement UMC's complete low power solution.

Type		Support Features		Support				
				28nm	40nm	65nm	90nm	0.13um
Operating Power	Voltage Island & Scaling	Level Shifters w / Insulator	Power & Timing Model @ 80% of Vdd	√	√	√	√	√
	Clock Gating & Frequency Scaling	Clock Gated F/F		√	√	√	√	√
Leakage Power	Multi-Vt	Multi-Vt cells		√	√	√	√	√
	Power Gating	Isolation cells, Retention F/F Headers / Footers, etc.		√	√	√	√	√
	Body Bias	Tapless cells	Timing / Power Model	√	√	√	√	√

Low Power Design Support



Reference Design Flow and Vendor Support

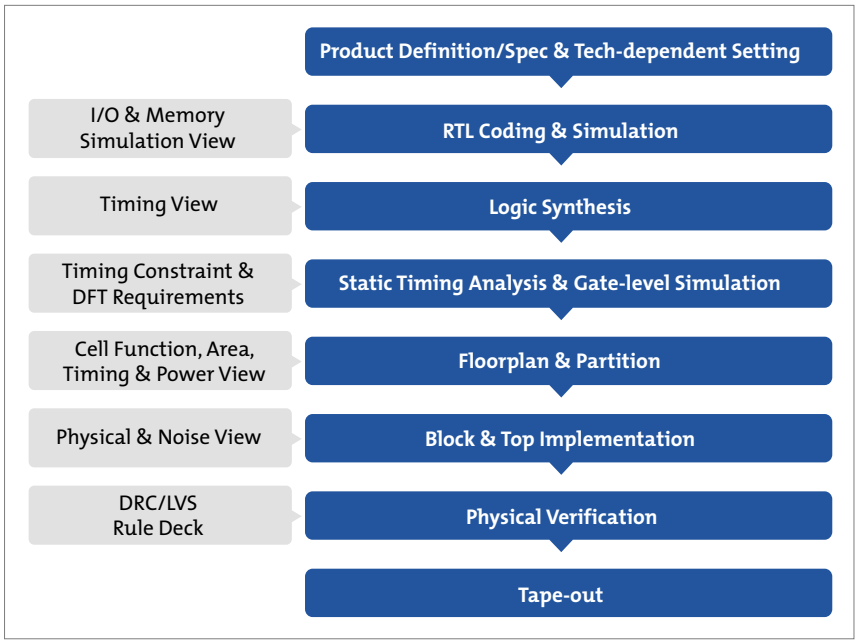
UMC works with leading EDA tool companies to provide a verified Reference Design Flow program to ensure the accuracy of customer designs in a proven environment. UMC's Reference Design Flow program integrates solutions for digital designs and low power solutions that incorporate the latest DFM resources available from leading third-party providers. Tools can be interchanged for added flexibility.

Features of Design Flow	Cadence	Synopsys	Mentor
Functional Logic Simulation	▲	▲	▲
Schematic Entry	▲	▲	-
Logic Synthesis	▲	▲	-
Static Timing Analysis	▲	▲	-
Timing Closure	▲	▲	-
Signal Integrity	▲	▲	-
Floor Planning	▲	▲	-
Physical Synthesis	▲	▲	-
Multi-Vt Low Power	▲	▲	-
Multi-Vdd Low Power	▲	▲	-
Design For Test	▲	▲	▲
Design For Diagnosis	▲	▲	▲
DFM - double via insertion	▲	▲	▲
DFM - dummy metal filling	▲	▲	▲
Circuits Simulation	▲	▲	▲
Power Analysis	▲	▲	-
Layout Editor	▲	▲	▲
Place & Route	▲	▲	-
Physical Verification	▲	▲	▲
Formal Verification	▲	▲	-
Parasitic Extraction	▲	▲	▲
Noise Analysis	▲	▲	-

Note: ▲ Available

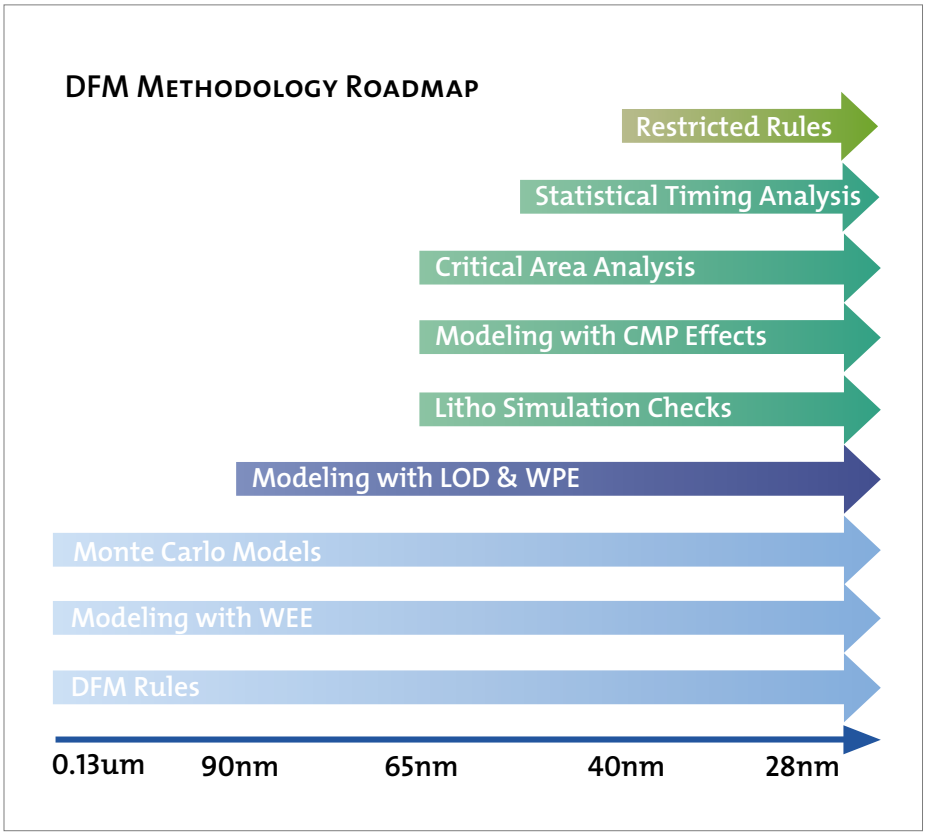
UMC Reference Design Flow

UMC Reference Design Flow provides a design methodology and flow validated with a "Leon2" system demonstration board. The flow incorporates 3rd-party EDA vendors' baseline design flows to address issues such as timing closure, signal integrity, leakage power and design for manufacturability and adopts a hierarchical design approach built upon silicon validated process libraries. UMC Reference Design Flow covers from RTL coding all the way to GDS-II generation and supports Cadence, Magma, Mentor and Synopsys EDA tools. All of these tools can be interchanged for added flexibility.



DFM Methodology

UMC offers optimal DFM (Design For Manufacturability) solutions to effectively and efficiently address factors that may negatively affect yield and performance for advanced technology designs. UMC's DFM solutions include advanced process models incorporated in SPICE and extraction decks for predicting random and systematic variations, technology files, DFM-compliant libraries and IP that embrace the intricacies of the fabrication process. Concise DFM recommendation rules are available along with a comprehensive rule-deck runset strategy to fulfill various design requirements.



UMC also offers pre-tapeout Optical Proximity Correction (OPC) and Litho Rule Check (LRC) for custom designs in addition to our standard post-tapeout services that include OPC, Litho Simulation Check (LSC), dummy fill, and metal slotting. At 65nm and below, UMC offers a DFM Design Enablement Kit (DEK) to seamlessly support model-based DFM tools. The DEK has a built-in Graphic User Interface (GUI) for DFM design database setup, and is completed with application notes and qualification reports for design reference.

New Customers
For new customer inquiries, please direct all questions to **sales@umc.com**

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