Viable Product Development at 22nm

Why an integrated value chain is becoming critical and where to find the necessary expertise to make all the pieces work together.

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Introduction

The end of classical scaling at 90nm and the introduction of a broad array of challenges that now have to be dealt with at every process node beyond 65nm has changed IC design forever. Design, manufacturing and production must be tied together more closely than ever in order to address the challenges of power, electrostatic discharge (ESD), electromagnetic interference (EMI), IP integration, complex packaging options and manufacturing yield. Few companies have the focused resources within each of these disciplines to successfully complete chips. Fabless semiconductor companies and medium-sized semiconductor companies that own their own fabs are forced to reconsider their business models looking outside for the high level of expertise required to complete the design and manufacture of chips.

If a complex system on chip (SoC) design costs $50 million to $100 million and it has a yield of about 10 percent to 25 percent, the real cost of the design can be orders of magnitude higher because bad yield has to be factored into the development cost. Finding a problem in embedded software that is hidden inside a piece of third-party IP is no simple task. Likewise, finding IP conflicts is difficult, but must be addressed. If a piece of IP doesn’t work well with other IP because it is too noisy, runs too hot or uses too much power, it can create havoc all the way across the design-to-manufacturing chain.

The above problems become more acute as the industry moves from the 28nm process node, which is just beginning to ramp up, to 22nm, which is now under development by leading semiconductor companies and foundries. Issues that used to be dealt with sequentially must now be dealt with concurrently across the entire supply chain.

This concurrent design imperative greatly increases the burden of understanding required by designers as well as the foundries that rely on successful designs and yield in order to reach their revenue targets. There are simply too many problems that can slip through the cracks.

This paper will discuss some of the challenges facing design and manufacturing in 22nm and offer solutions to help overcome these challenges.

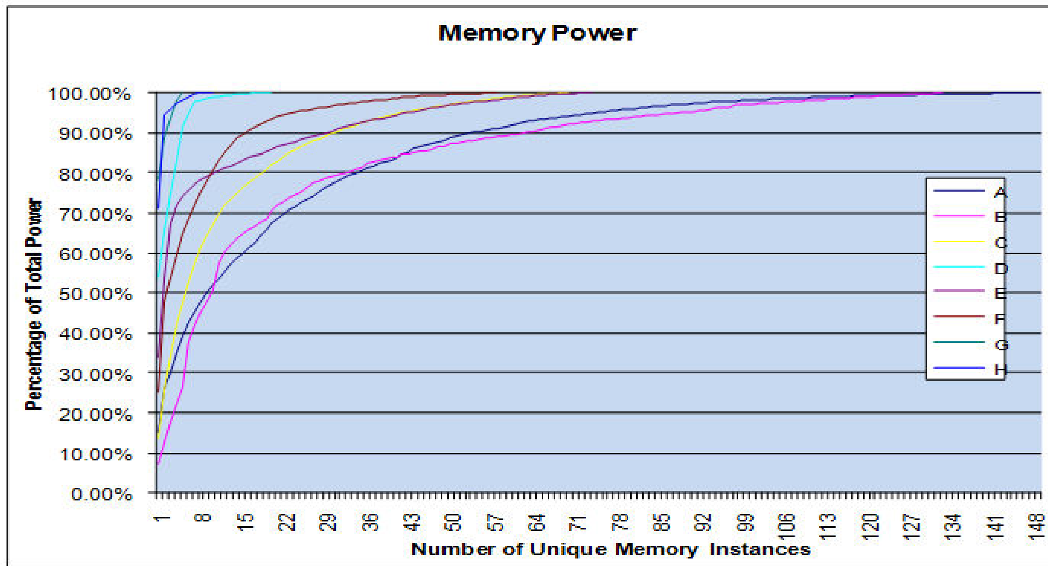
Power Challenges

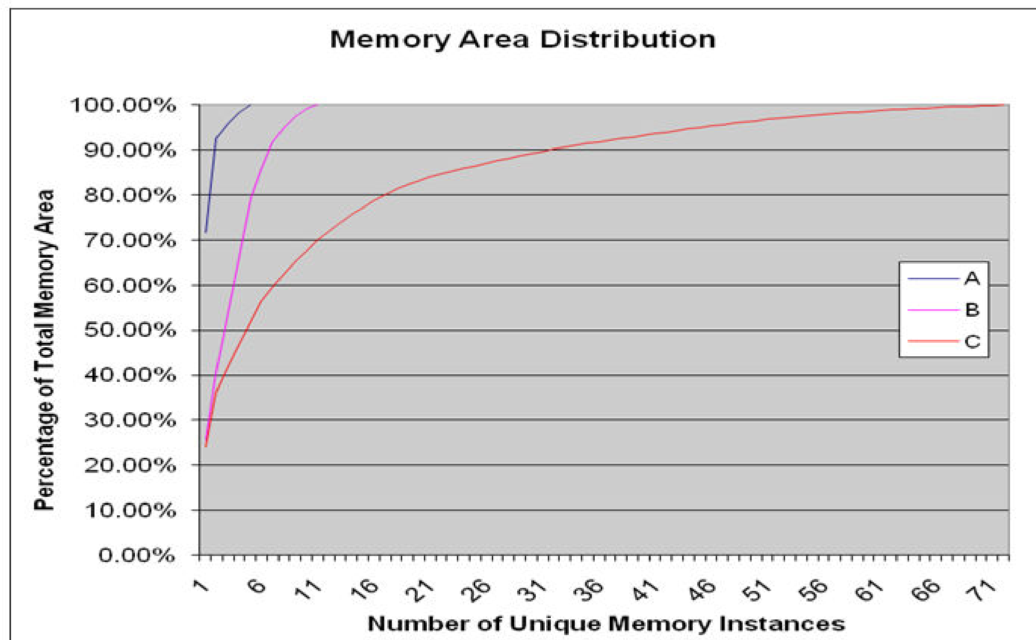
There are a number of distinct power-related challenges that are particularly difficult to rectify with a disaggregated supply chain:

- At 22nm, leakage is no longer confined to just static current. High-K/metal-gate technology has helped, but advanced nodes will require an understanding of both static and dynamic leakage. Electro-migration also becomes an issue as channels between wires continue to shrink, creating hot spots in chips that are difficult to predict and even harder to fix after the architectural phase.
- IP has to be characterized at each process node and for the particular circumstances in which it is used within a design. An I/O structure may work fine at 40nm, but it might create EMI effects at 22nm. Similarly, a two-core processor might fit the bill for power, but it may provide either too much or too little performance for a specific task. That, in turn, affects the overall power budget for an SoC.
- Power models are difficult to create when upward of 50 percent of a design involves third-party IP where accurate measurements are impossible to make at the architectural level. Unless a company is familiar with the way a particular piece of IP behaves, it is difficult to do up-front tradeoffs on a design. That creates problems at the back end, where it typically is too late—and far too expensive—to change.

Embedded Memory Challenges

Area and power in SoCs are dominated by memory. On average, embedded memory takes up more than 55 percent of the die area and more than 50 percent of the total power. These percentages are expected to increase over the next years. Interestingly though it is a few memory instances that represent most of the area and power ***(Refer to Diagrams)***. This presents a significant opportunity to reduce the power and size of the chip through the use of customized instances of those few memory blocks. Access to affordable, high-quality custom memory IP could reduce power and area of the SoC by 5-10 percent while also supporting product differentiation.





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Stacked Die Challenges

By late 2012 and early 2013, most foundries and large chipmakers believe some sort of stacking will be required.

There are compelling advantages to be gained with stacked die. Shorter wires and wider I/O mean a significant increase in performance using less energy to drive signals. There also could be a significant savings in development time if a pre-developed memory or logic chip can be connected using some standard connectivity with an older-process analog chip.

There are also some significant technical issues that have to be addressed:

- The number of choices will increase dramatically with stacked die. An intimate understanding of IP and how it works in these new structures will be essential.
- Risk management will increase significantly as die are stacked. Two known good die may work fine independently, but when they're put together may yield one bad stacked die. If there are two die in the package, the cost of bad yield doubles.
- Packaging expertise will be critical in the manufacturing of stacked die. Understanding the advantages and disadvantages of various packaging options and materials could mean the difference between a cost-effective implementation that works and one that costs too much and doesn't work.

Specialists Required

Specialization drives efficiency. When TSMC Chairman Morris Chang proposed a commercial foundry model in 1987, most chip developers believed the model was ill conceived. That was before the price of an advanced 300mm wafer fab rose to several billion dollars and Moore's Law forced chip designers to grapple with unbelievable complexity.

Fast-forward 24 years, and there are only a handful of pure-play chipmakers left. But even the largest of these companies use some foundry services, almost all purchase third-party IP, and an increasing number rely on outside companies for help at some stage in the design-to-manufacturing progression. Time-to-market pressures, international competition and the rising costs of chip designs caused by increasing complexity have made it imperative for companies to focus on what they do best, both from a technology and business standpoint. That means they need to decide which functions to offload to save time or money, or to make them more competitive technologically. But those companies completing one or two designs a year cannot hope to stay current with the latest tools and methodologies, and they don't know which IP will work best in a design or what tradeoffs should be considered.

Dealing with chip design at 22nm requires more specialization than ever before and that means working with the best partners.

Integrating the Disaggregated Value Chain

The increased complexity of the entire process at 22nm combined with a compression of the design-to-manufacturing cycle highlight the need for increasingly cohesive teams. Unfortunately, this comes at a time when design starts are down and most companies—including even the largest semiconductor companies—are producing fewer chips with fewer resources and typically with lower yields. With fewer design starts, it's nearly impossible to maintain the internal team of experts required to deal with extreme chip design.

Chipmakers are facing a difficult choice—what is their value add, where do they see their future profits, and what do they have to do to get there from an expertise standpoint? Is it the brand, the analog or digital IP, the manufacturing, or the whole design, productization and manufacturing process? And do they really understand the competitive tradeoffs of using existing processes, flows, IP and in-house skill sets? If they bring in outside specialists to solve these problems, do they have the best supplier contacts and do they have the staff and sophisticated, automated tools to manage the design through a complex team?

Within the last 10 years, value chain producers (VCPs), such as eSilicon, have built successful business models specifically to address the vast challenges of complex chip design and manufacturing. Offloading manufacturing to a VCP that produces hundreds of chip designs each year gives OEMs and IDMs confidence that they are improving

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their products through the VCP expertise, while decreasing overhead and freeing up valuable engineering time to address R&D, support and marketing.

Developing chips is only going to get harder. The companies who quickly identify what they do best and what they should outsource will be better positioned to beat competitors to market with better products as well as deal with the challenges of future generations of chips.

About the Author:

Kalar Rajendiran is the senior director of marketing for eSilicon Corporation, where he is responsible for the company's branding, corporate marketing, investor relations and marketing operations.

About eSilicon

eSilicon, the largest independent semiconductor value chain producer (VCP), delivers ASICs to OEMs and fabless semiconductor companies through a fast, flexible, lower-risk path to volume production by deploying its comprehensive suite of design through manufacturing services and custom IP offerings. We serve a wide variety of markets including the communications, computer, consumer and industrial segments.

Whether you need ASICs or ASSPs, custom semiconductor IP to optimize your chip's performance, or semiconductor manufacturing services to drive your proven chip through volume production, eSilicon can manage your design through production so you can focus on R&D for your next innovation.

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