Design Virtualization and Its Impact on SoC Design

Advanced SoC projects present the designer with a large number of options for technology, IP, foundation libraries, memory and operating conditions. Finding the right combination is difficult as costly and time-consuming trial implementations are needed. This paper discusses a unique new approach to this problem called design virtualization.

Executive Summary

At advanced technology nodes (40nm and below), the number of options that a system-on-chip (SoC) designer faces is exploding. Choosing the correct combination of these options can have a dramatic impact on the quality, performance, cost and schedule of the final SoC. Using conventional design methodologies, it is very difficult to know if the correct options have been chosen. There is simply no way to run the required number of trial implementations to ensure the best possible option choices.

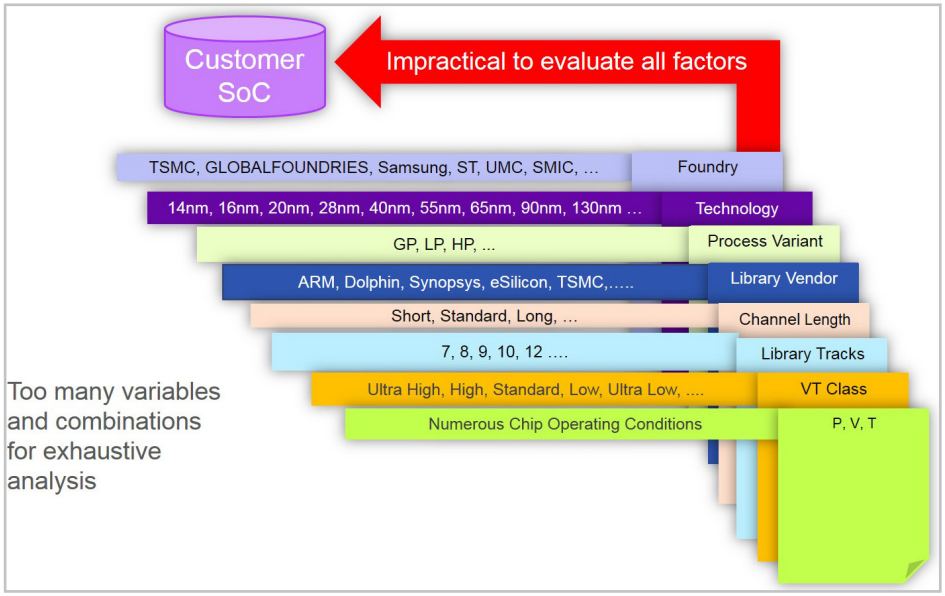
This document outlines the strategic customer benefits of applying a new technology called design virtualization to optimize SoC designs.

Design Challenges

Coupled with exploding option choices, the cost to design an SoC is skyrocketing as well. According to Semico Research Corporation, total SoC design costs increased 48 percent from the 28nm node to the 20nm node and are expected to increase 31 percent again at the 14nm node and 35 percent at the 10nm node.

Rising costs and extreme time-to-market pressures exist for most product development projects employing SoC technology. Getting the optimal SoC implemented in the shortest amount of time, with the lowest possible cost is often the margin of victory for commercial success. Since it is difficult to find the optimal choice of technology options, IP, foundation libraries, memory and

Figure 1. Option Choices Faced by the SoC Designer



operating conditions to achieve an optimal SoC, designers struggle to get the results they need with the choices they have made. These choices are made without sufficient information and so they are typically not optimal.

In many cases, there is time for only one major design iteration for the SoC. Taking longer will result in a missed market window and dramatically lower market share and revenue. For many companies, there is only funding for one major design iteration as well. If you don't get it right, the enterprise could fail. This situation demands getting the best result on the first try. All SoC design teams know this, and there is substantial effort expended to achieve the all-important first-time-right SoC project.

This backdrop creates a rich set of opportunities for technology that can reduce risk and improve results. Commercial electronic design automation (EDA) tools are intended to build the best SoC possible given a fixed set of choices. What is needed to address this problem is the ability to optimize these choices before design begins and throughout the design process as well. This will allow EDA technology and SoC design teams to improve the chances of delivering the best result possible.

Design Virtualization Defined

Design virtualization addresses SoC design challenges in a unique and novel way. The technology focuses on optimizing the recipe for an SoC using cloud-based, big data analytics and deep machine learning. In this context, recipe refers to the combined choices of process technology options, operating conditions, IP, foundation libraries and memory architectures. Design virtualization allows the optimal starting point for chip implementation.

The technology frees the SoC designer from the negative effects of early, sub-optimal decisions regarding the development of a chip implementation recipe. As we've discussed, decisions regarding the chip implementation recipe have substantial and far-reaching implications for the schedule, cost and ultimate quality of the SoC. A correctly defined chip implementation recipe will maximize the return-on-investment (ROI) from the costly and risky SoC design process.

In traditional design methodologies, the chip implementation recipe is typically defined at the beginning of the process, often with insufficient information. As the design progresses, the ability to explore the implications of changing the implementation recipe is more difficult, resulting in longer schedules, higher design costs and sub-optimal performance for the intended application.

Design virtualization changes all that. Through an abstraction layer, the ability to explore the implications of various chip implementation recipes now becomes possible. For the first time, SoC designers have "peripheral vision" regarding their decisions. They are able to explore a very broad array of implementation recipes before design begins and throughout the design process. This creates valuable insights into the consequences of their decisions and facilitates, for the first time, discovery of the optimal implementation recipe in a deterministic way.

In many ways, the process is similar to the virtualization concepts made popular in the computer and enterprise software

Figure 2. Computer Virtualization (Source: VMware)

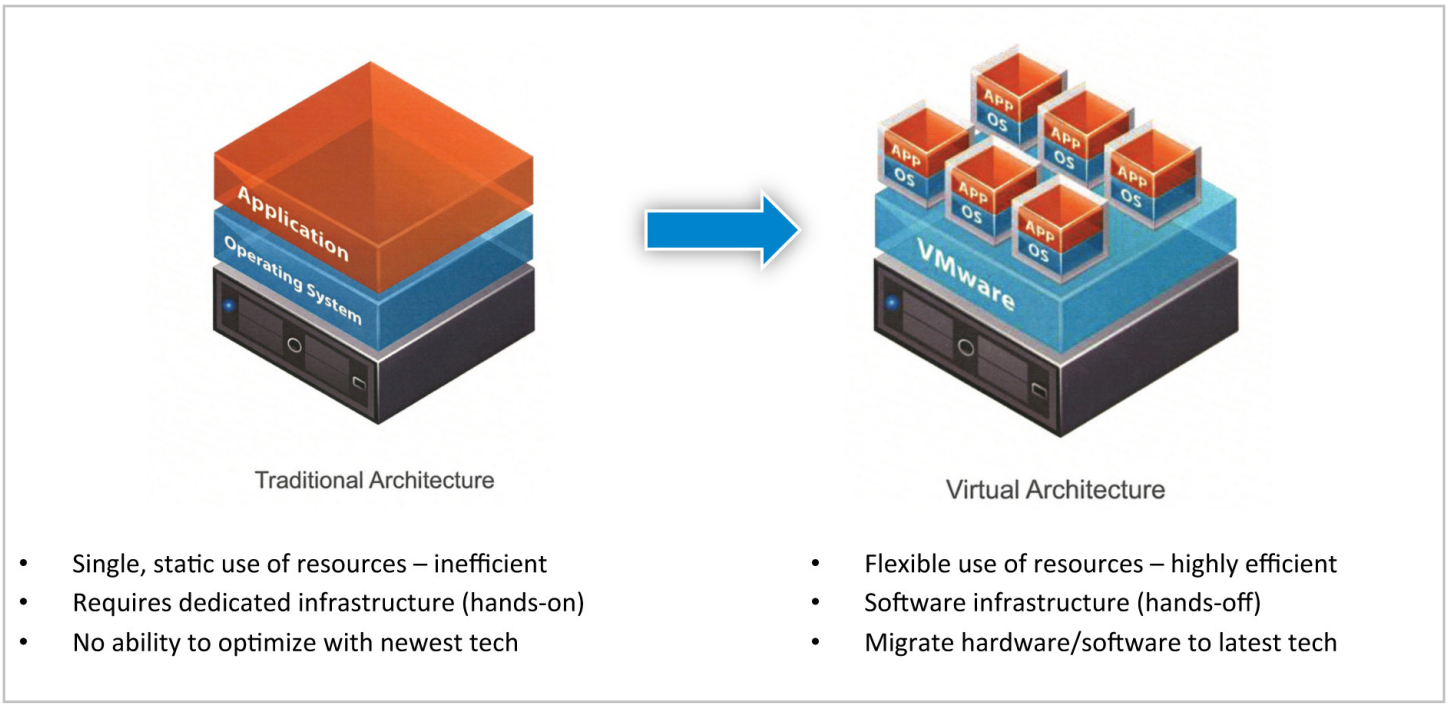
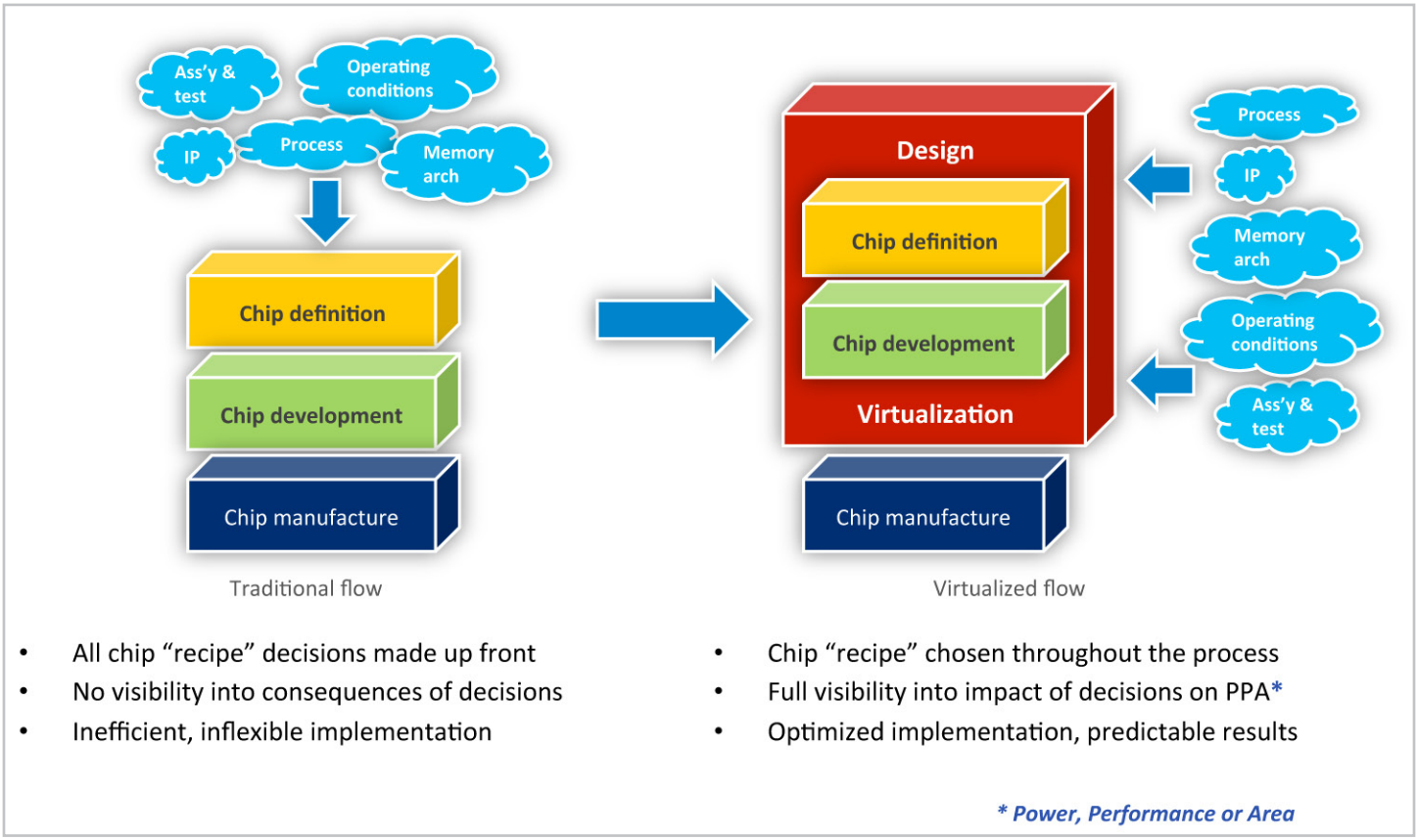


Figure 3. Design Virtualization: Traditional vs. Virtualized Design Flows (Source: eSilicon)



industries. Computer/network/storage virtualization facilitates the delivery of multiple and varied services with the same hardware through an abstraction layer. This abstraction layer maps the physical computing environment into a logical implementation, allowing flexible deployment of the resources. The result is a more efficient use of the underlying hardware and the delivery of multiple optimized user experiences.

Regarding SoC design, design virtualization creates an abstraction layer that maps actual physical results into predicted, logical results to assist in finding the best possible implementation recipe. The result is a more efficient use of the underlying process and design resources and delivery of an optimized SoC.

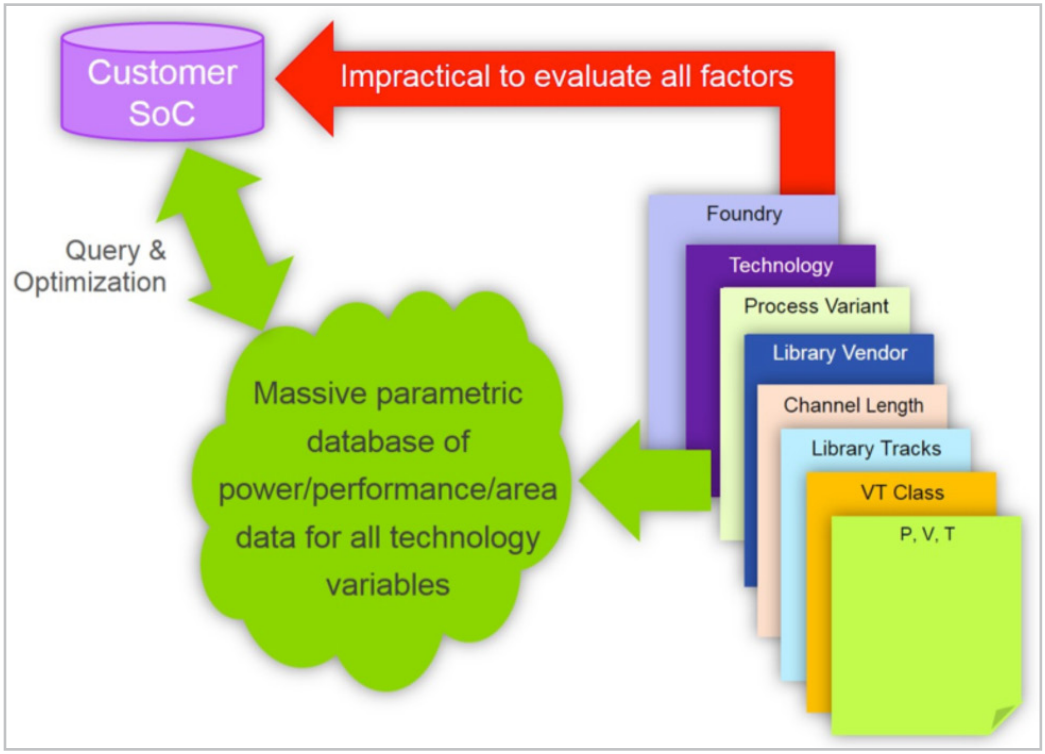
Design Virtualization – How it Works

At its core, design virtualization utilizes big data strategies to capture engineering knowledge from suppliers worldwide regarding how process options, IP, foundation libraries, memory architectures and operating conditions interact with each other to impact the power, performance and area (PPA) of an SoC design. Machine learning is then applied to this data to allow exploration of design options. The information is accessed through the cloud and real-time, predictive analysis is provided to guide the optimal choice for all these variables.

As discussed, all the choices contributing to the implementation recipe for an SoC are exploding below 40nm. Understanding how these choices interact to impact the final PPA of the SoC requires extensive trial implementations, consuming large amounts of time and resources, in terms of both staff and EDA tools.

Design virtualization solves this problem with a massive parametric database of options for semiconductor value chain suppliers, worldwide. A cloud-based front-end query system is provided that facilitates real-time, predictive analysis from this database. Because all data is pre-generated, exploration of various options can be done instantly, without the need for expensive EDA tools or time-consuming trial implementations. This approach creates a new-to-the-industry capability.

Figure 4. Architecture of Design Virtualization



Design Implementation

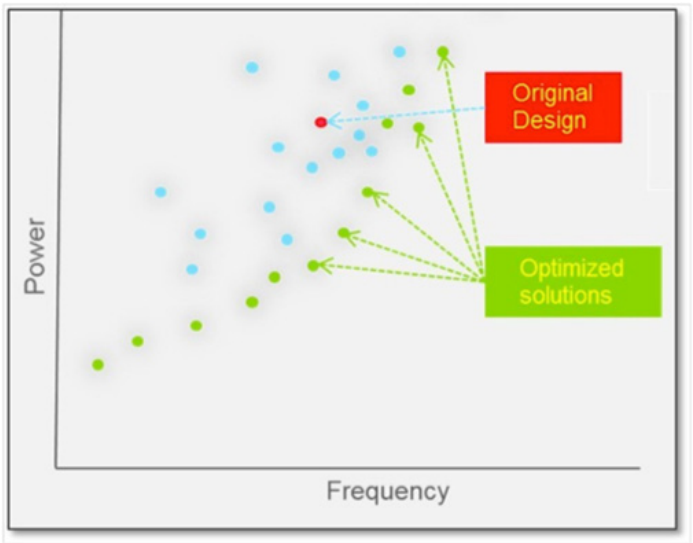
There is a significant gap between what EDA vendors and IP vendors deliver when compared with the new issues facing every SoC designer today. The gap can be characterized by two key observations:

- EDA focuses on creating an optimal solution for one, or a limited number, of design implementation recipes
- The ~$4B EDA industry is focused on logic optimization and not memory optimization

Regarding chip implementation recipes, the ability to explore the broader solution space for each design is now within reach of all design teams. Thanks to the big data, cloud-based machine learning employed by design virtualization, designers may now perform “what if” exercises for their design recipe options in real time, creating a palette of solutions that has been previously unavailable.

Using this technology, the design team can start with the desired PPA target and quickly identify the implementation recipe required to hit that target. This essentially reverses the typical time-consuming design exploration process. The result is an optimized implementation recipe that balances the PPA requirements of the SoC with the commercial options offered by the worldwide semiconductor supply chain.

Figure 5. Quickly Identifying Optimal Implementations



With regard to memory optimization, 50 percent or more of the total area of today’s SoCs can contain on-chip memory. The detailed configuration of these memories can have a

substantial impact on the final PPA of the chip, but most design teams choose a series of compiled memories early in the design process and never revisit those choices during design implementation. The result is often lost performance, wasted chip area and sub-optimal ROI for a bet-your-company SoC design project.

Design virtualization provides a way to explore all possible memory configurations for a given implementation recipe in real time. Memory customization opportunities can also be identified. Using generic memory models that can be provided by eSilicon, further refinement and optimization of the memory architecture of the SoC is possible, right up to tapeout. This design implementation flexibility is commonplace for the logic portion of the chip, but is new for the memory portion.

The EDA design flow is as important as ever, but now the starting point for design implementation can be an optimized implementation recipe, resulting in an SoC with superior PPA and optimized cost and schedule. An example of the impact of exploring implementation recipes for a 28nm design is shown below.

Conclusion

We have discussed a new approach to improve the results of SoC design called design virtualization. We believe the approaches outlined in this document provide new-to-the-industry capabilities with the opportunity for significant strategic differentiation.

Design virtualization can substantially improve the PPA and schedule of an SoC, resulting is an improved ROI for the massive cost and high risk associated with these projects.

The techniques described here are used daily inside eSilicon for all customer designs. We have achieved significant power reduction and broad design implementation improvements by analyzing customer designs and employing design virtualization techniques.

eSilicon is developing a robust product roadmap to make selected design virtualization capabilities available to all design teams worldwide, regardless of size.

For more information contact info@esilicon.com or visit www.esilicon.com.

Table 1. Optimization Results With Design Virtualization

Technology	Industry 28nm Process	Alternative A	Alternative B	Alternative C	Alternative D
Area (sq.mm)	42.4	42.57	44.97	42.54	46.53
Speed	Target same speed				
Voltage	1V ± 0.1V	0.9V± 0.1V	1V ± 0.1V	1V ± 0.1V	1V ± 0.1V
Standard Cell Library	30nm SVT and LVT	30nm LVT	40nm LVT	30nm SVT	35nm SVT and LVT
Leakage Power (FF, Vmax, 125C)	1.29W	657mW	2.06W	650mW	1.25W
Dynamic Power (TT, Vnom, 25C)	756mW	663mW	971mW	670mW	1.05W

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