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Evaluation of integration schemes for contact-hole grapho-epitaxy DSA: A study of substrate and template affinity control

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ABSTRACT

An electrical test vehicle for fabricating direct self-assembly (DSA) sub-30 nm via interconnects has been fabricated employing a soft mask grapho-epitaxy contact-hole shrink. The generation of the resist pre-pattern was carried out using 193i lithography on three different stacks and the BCP assembly was evaluated with and without template affinity control on the resist pre-pattern. After DSA shrink, the holes were transferred in a 100 nm oxide for standard Tungsten metallization for electrical characterization.

INTRODUCTION

In recent years, block copolymer (BCP) directed self-assembly (DSA) has been widely investigated as a potential technique to extend lithography to meet the challenging requirements of future nodes[1,2,3]. Versatility and low cost are the key points that make DSA so attractive when compared to 193i multiple patterning and extreme ultraviolet lithography (EUVL), which requires further source development. Indeed, with DSA PS-b-PMMA lithography, holes having sizes as small as 20 nm can be obtained with a single exposure.

The critical points for a grapho-epitaxy contact-hole shrink DSA process in a template include obtaining a good quality resist pre-pattern and realizing proper phase separation of the BCP through the control of the free surface energy in the template[4]. Therefore, the study of the pre-pattern formation of the targeted structures on three stacks is first addressed. As for the BCP phase separation, the effect of template affinity control on the pre-pattern for free surface energy control is investigated.

The three layer test vehicle under study is called EVEREST (EV28), a 28 nm planar flow composed of two metal layers (LI2 and M1) and V0 (figure 1). In the V0 layer the 193i resist pre-pattern is printed and constitutes the pre-pattern for DSA-BCP shrink.

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This electrical test vehicle for contact-hole shrink has been previously used with a Si blend that allowed for a 60 to 28 nm shrink[5]. Using a BCP instead, allows not only contact-hole shrink but also pitch multiplication and CD repair[6].

The EV28 test vehicle measures two types of electrical structures: Kelvin (or single resistance measurement) and chain structures where 10, 100 and 10000 holes are connected (see figure 1). The evaluation of BCP assembly as a function of CD, open hole yield, and template affinity control of the resist pre-pattern is studied in the staggered hole array. Specifically, this work focuses on the 55P90-110 staggered holes as shown in figure 1.

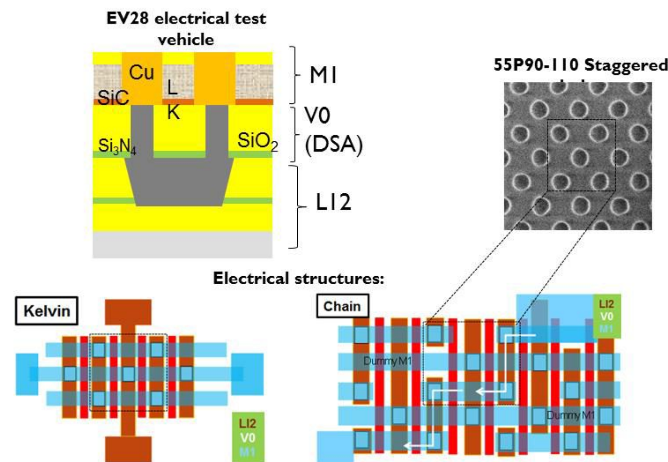

Figure 1. EV28 stack and structures under evaluation

As mentioned above, the surface energy is the key for obtaining good BCP assembly and typically a neutral layer is deposited to ensure good orientation of the BCP. With this in mind, aside from the EV28 standard or CVD stack, two more stacks are added to the study: the NLD or neutral layer stack and a trilayer stack (figure 2). The NLD stack ensures good BCP assembly but it negatively impacts the etch selectivity to open the hole and transfer the pattern (note that the neutral layer is a random PS-r-PMMA polymer, thus similar chemistry to the BCP). On the contrary, the trilayer stack provides good etch selectivity (spin-on SOG/SOC) and also doubles as a neutral layer. In addition, it provides reflectivity control, which is important for the resist pre-pattern definition.

The CVD stack for the EV28 vehicle comprises a 15 nm Si_3N_4 etch stop, a dual dielectric layer (100 nm SiO_2 + 100 nm APF), and a 20 nm SiOC hardmask. For the neutral layer stack, a 10nm PS-r-PMMA layer is cast on the standard stack. Lastly, the trilayer stack is composed by 20/100nm SOG/SOC on top of 100 nm SiO_2 and 15 nm Si_3N_4 etch stop layer.

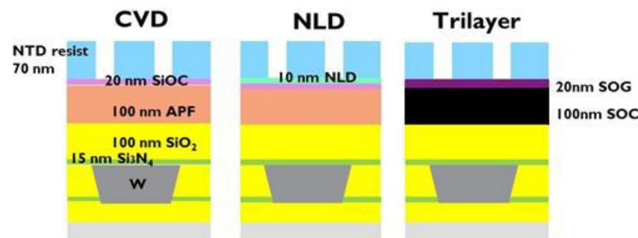

Figure 2. EV28-V0 DSA-BCP stacks under study

The grapho-epitaxy DSA contact shrink flow is depicted in figure 3. First, a 70 nm negative tone developable (NTD) photoresist is patterned. A NTD resist is employed because of its enhanced aerial image and capability for printing holes. Also, as a negative tone resist is insoluble in most organic solvents, our cylindrical PS-b-PMMA BCP can be coated without impacting the resist pre-pattern. After litho, a hard-bake step is required to crosslink the resist in order to make it resistant to the high annealing temperatures of the BCP (>200°C). For BCP assembly the flow is as follows: first the BCP film is cast and annealed. During the phase separation, the PS is ideally positioned in the walls of the hole with the PMMA in the core. For this contact-hole shrink process we use a wet development process as described elsewhere[7]. In this wet process there is a combination of DUV exposure for PMMA chain scission followed by a solvent rinse that selectively removes the PMMA[8]. As the PMMA is removed, a better etch selectivity is provided for pattern transfer compared to RIE etch resulting in a contact-hole CD of approximately 23 nm. Next, etch and strip is performed until the Si_3N_4 stop layer. Note that at this step the holes are open to ~37 nm (larger CD than after DSA) due to the restrictions of the standard W-ALD metallization. This is necessary to understand the performance of DSA BCP hole shrink versus the standard etch shrink procedure. However, the DSA shrink holes are intended for testing new metallization schemes, for instance, NiB electroless[9]. Last, the holes are filled with W-ALD metallization, planarized, and M1 is deposited to allow electrical measurements.

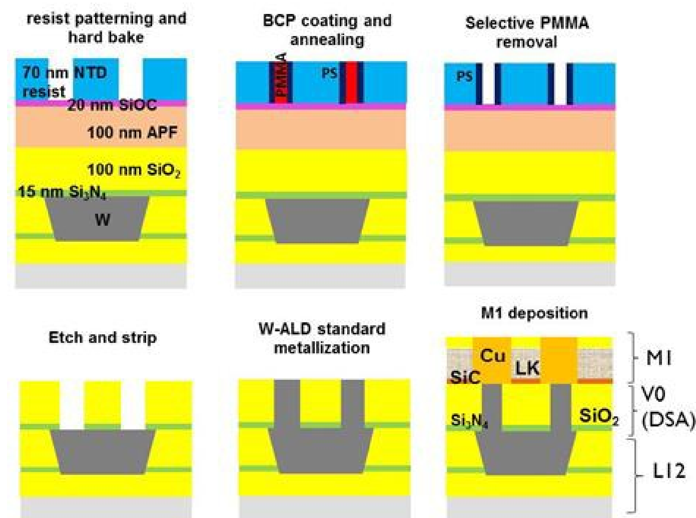

Figure 3. EV28-V0 DSA-BCP shrink process flow

EXPERIMENTAL

EV28-VA0 pre-patterns were obtained by exposing wafers on an ASML 1950i immersion scanner using IMEC's EVEREST-28 VA0 mask and a custom Flexray illumination setting (NA=1.35, ϴ=0.776/0.614, XY-polarized). An NTD guide resist material (Gen 3) was employed. After exposure it was subjected to a hard bake step for 300s at 200°C.

The CVD stack was treated with a dehydration bake (205°C; 60sec). The contact hole shrink grapho-epitaxial process flow was performed on TEL CLEAN TRACK ACT™ 12. It has been found that a 15-19 nm BCP film is the optimal thickness for filling the guide pattern. However, for the electrical wafers, 15 nm was found to be the optimal for filling the electrical structures. The BCP was coated to a film thickness of approximately 15-19 nm (as determined for a similarly cast film on bare silicon) and annealed at 240°C for 600 seconds under an N_2

environment. Next, the wafer was exposed to UV light for degrading the PMMA core of the BCP and it was selectively removed with organic solvent.

Film thickness measurements were made on a KLA-Tencor SCD100 ellipsometer. Overlay measurements for the LI2-VA0, VA0-MT1, and LI2-MT1 layers were assessed with using either a KLA-Tencor Archer200 or Archer-AIM. CD SEM measurements were performed on a Hitachi CG-4000. All cross-section SEM measurements were performed on a Hitachi SU-8000. For FIB analysis, a Helios450HP dual-beam FIB/SEM system was employed. All etch studies reported herein were performed on the TEL Tactras^{TM} platform.

RESULTS AND DISCUSSION

1-Resist pre-pattern definition

In this section, the definition of the pre-pattern for our NTD resist in the three targeted DSA structures (staggered, Kelvin and Chain) is described.

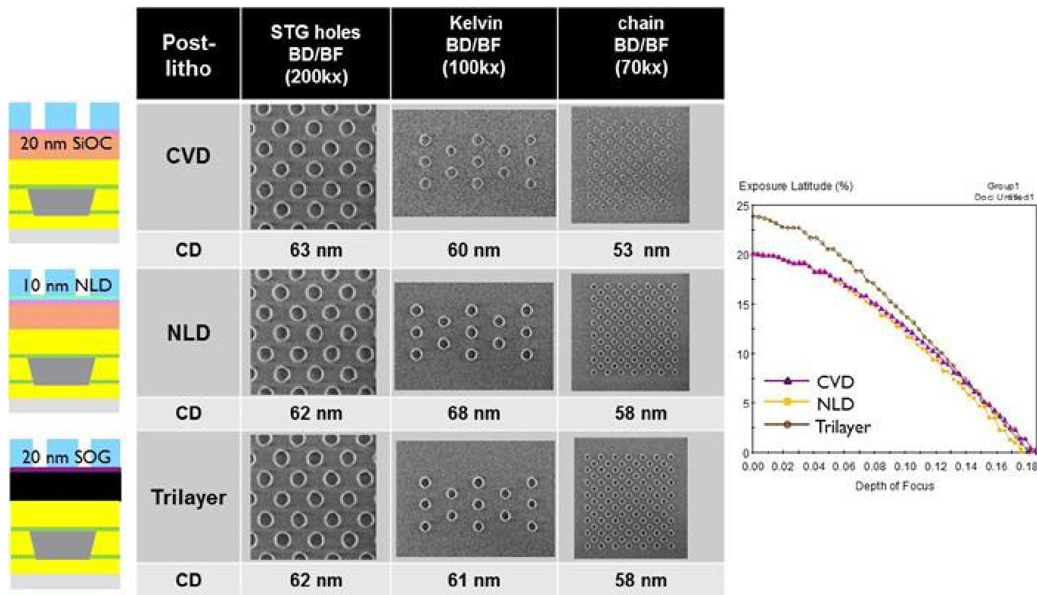

Figure 4. Resist pre-pattern definition with the resist for the STG and electrical structures

Figure 4 shows the results for the targeted structures after litho for the three stacks. For a target CD of 60 nm at the best dose/ best focus, the staggered contact-hole array shows good results for the three stacks. However, for the electrical structures, the CD tends to shift for the CVD and NLD stacks. This is not the case for the trilayer which shows similar CD regardless of the dense (staggered), semi dense (chain), and isolated (kelvin) structures. Indeed, the exposure latitude versus depth of focus (DOF) plotted in figure 4 shows a superior performance for the trilayer stack. Next, hard-bake is performed at 200°C under N_2 and a reflow of the resist is observed. The CD after hard-bake increases approximately 10 nm during the crosslinking of the resist, therefore, the target CD of 60 nm at litho becomes 70 nm after hard-bake.

2-BCP phase separation and template affinity control of the pre-pattern

As explained above, during the phase separation, ideally the PS is positioned in the walls of the hole with the PMMA in the core. However, PS wetting at the bottom of the hole has been observed[7]. This section aims to

study the effect of template affinity control on the pre-pattern during BCP phase separation. This study is focused on the dense staggered hole structures that offer the possibility to evaluate both the BCP assembly and the template affinity control.

The first thing to establish for the grapho-epitaxy BCP assembly is the optimal BCP film thickness (FT). There are two boundary conditions to find the optimal FT: first, the film is too thin and the pre-pattern is not properly filled, second if it is too thick parallel orientation will be observed as a consequence of polymer overflow. In between these two scenarios lies the optimal film thickness which is between 15 and 19 nm for the polymer under study.

For studying the CD influence, a 300 mm wafer having hole pre-patterns with CDs ranging from 80 to 55 nm was prepared by changing exposure dose and focus. As depicted in the CDSEM pictures in figure 5(a) and (b), the optimum CD pre-pattern for BCP assembly was between 75 and 65 nm after hard bake. At larger CDs the holes became elliptical until both parallel and cylindrical orientation was observed. The CD after DSA is approximately 23 nm (which translates to a 65% hole shrink). Further observation at higher magnification shows the presence of a top ring for the 19 nm and missing holes for 15nm FT. This means that 15 nm FT probably belongs to the regime where the polymer is too thin.

However, even for the optimal 19 nm FT, remaining polymer is observed on top of the resist pre-pattern. The next step is the study of the template affinity control. This process is integrated in a specific module in the track and allows us to make the surface of the pre-pattern more hydrophilic. The effect of the template affinity control is observed in figure 5 (b) and (c) where no PS over ring and no polymer remaining are observed on the pre-pattern after the pre-treatment. Contact angle measurements of the resist after template affinity control show a change from 70 to 40 degrees. Thus, as a result of making the surface more hydrophilic, the PS component of the BCP is more prone to diffuse into the hole instead of remaining on the pre-pattern surface. Indeed, further XSEM analysis of the 65 nm CD after etch shows that the over ring observed without template affinity control creates a closure on top of the hole, while with template affinity control a clean hole is obtained. Although figure 5 only depicts the result for the trilayer stack, the same effect has been observed for the three stacks under study and no missing holes were observed regardless of the stack after template affinity control as seen in figure 6. From the top CDSEM is difficult to discern what happens at the bottom of the hole in terms of BCP phase separation, but the electrical measurements will determine if the template affinity control also helps the segregation of the polymer at the bottom of the hole.

With this in mind, dose stripe electrical wafers with and without template affinity on the CVD and trilayer stacks are going to be studied. As for the NLD stack, only the influence of the NLD is studied (no affinity control). In addition to the DSA wafers, control wafers (no DSA) are included in order to evaluate the electrical performance of the stack versus the DSA shrink. For these dose/stripe electrical wafers, CDs ranging between 75 and 60 nm have been targeted.

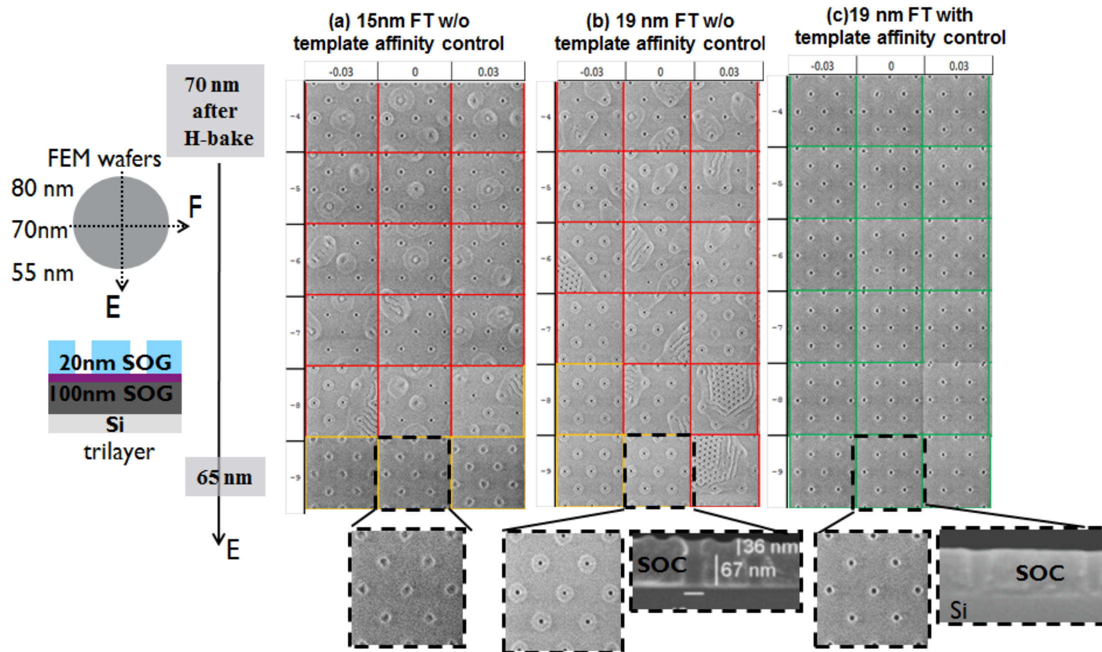

Figure 5. Effect of film thickness and template affinity control for BCP alignment in the resist pre-pattern for the trilayer

(a) CVD die 0,-9		(b) Trilayer die 0,-9		(c) NLD die 0,-9	
with affinity control	w/o affinity control	with affinity control	w/o affinity control	With affinity control	w/o affinity control
CD 24 nm (65% shrink)	CD 20 nm (65% shrink)	CD 23.3 (65% shrink)	CD 19.5 nm	CD 24.5 nm (65% shrink)	CD 20 nm (65% shrink)

Figure 6. Effect of template affinity control on the three stacks (a) CVD, (b) trilayer and (c) NLD

3-Etch, metallization and electrical characterization

The etch development was performed first in the control wafers (no DSA and no template affinity control). Figure 7 shows the CD after etch on the STG, kelvin, and chain structures for die (0,7) with an initial CD of 70 nm after hard bake for the three stacks. In general, good transfer is found for the CVD and NLD stacks but the etch in the trilayer seems to be tapered. Cross-section of the substrate after resist, SOG, and SOC etch show good transfer until the etch in the oxide, where the CD is smaller. Indeed, the CD in the STG is 10 nm smaller for the trilayer than for the other stacks. For the case of the electrical structures, etch in the kelvin and chain is fine in the CVD and NLD stacks and not completely transferred on the trilayer stack. After metallization, all the pre-patterns for the STG array show good metal filling (see same figure).

Post-etch die 0,7	STG holes (200kx)	Kelvin (100kx)	chain (70kx)	Metallization STG holes (20kx)
CVD 71 nm after H-bake				
CD	61 nm	53 nm	52.1 nm	filled
NLD 72.5 nm after H-bake				
CD	62 nm	56 nm	60 nm	filled
Trilayer 72 nm after H-bake				
CD	55.6 nm	50 nm	52 nm	filled

Figure 7. Etch in the control electrical wafers for the three stacks in the staggered, kelvin and chain structures. The last column depicts the metallization in the staggered holes

As for the DSA wafers, figure 8 shows the effect of the template affinity control after DSA and etch. It is clear that there is an impact on CD uniformity if we compare the images with and without affinity control for the CVD stack. The NLD stack shows missing holes after etch, which suggests that the NLD might be crucial in a chemo-epitaxy scheme but it is not so important in grapho-epitaxy, where the walls offer larger surface area than the bottom of the via. In addition, surface energy measurements of the resist show a neutral behaviour. Therefore, in the NLD stack, the full via will behave as neutral with no preferential wetting from either the walls or the bottom. Indeed, the DSA shows a different hole CD. The etch in the trilayer stack is definitely marginal as compared to the other two stacks. Although DSA looks similar to the CVD with the template affinity control, few holes were transferred in the STG array.

These observations are supported by the electrical characterization data. Figure 9 summarizes the electrical data for the 40nm kelvin structures in the three stacks for control (no DSA) and DSA samples. The control wafers show good conductivity with higher resistance observed for the trilayer since the resistivity also takes in account the volume of the via (contact holes were 10 nm smaller after etch than in the CVD and NLD stacks). The DSA wafers show good conductivity only for the CVD stack. The NLD wafers show high resistance and the trilayer does not yield any electrical data.

In order to see the relationship between resistance and via size, a few data-points for the Kelvin structures have been collected for the control and DSA with affinity control after etch for the three dies in the CVD stack (figure 10). Out of this plot can be observed that the CVD without affinity shows larger resistance than with affinity. In the same figure, the pictures for the kelvin structures are shown with and without affinity control. It is important to remark that the DSA with affinity control shows a smaller CD after etch, but the resistance is much lower than for the DSA wafer without affinity control, where larger CDs are observed. From these results it can be concluded that the template affinity control is improving the BCP assembly. The insert in the same figure shows that the trend of resistance versus CD (control vs. DSA affinity) can be fitted to a linear trend with higher resistance for smaller CDs.

Die 2,6 @ STG	Hole CD~70nm (200kx)	DSA and etch with template affinity control (200kx)		DSA and etch without template affinity control (200kx)		CMP+W-ALD metallization (20kx)
stack	H-bake	DSA	etch	DSA	etch	metallization
CVD						
NLD		NA	NA			
Trilayer						

Figure 8. DSA and etch in DSA electrical wafers for the three stacks in the staggered structures.
The last column depicts the metallization in the staggered holes)

Contrary to the Kelvin, the chain structures did not show electrical conduction for the DSA wafers (figure 11). The control showed similar resistance for the Kelvin and the 10 hole chain structures. However, the resistance is larger for a larger number of connected holes, meaning: R(10000)>R(100)>R(10). The cause for DSA failure is shown in the same figure where the picture of the chain after etch reveals incomplete transfer.

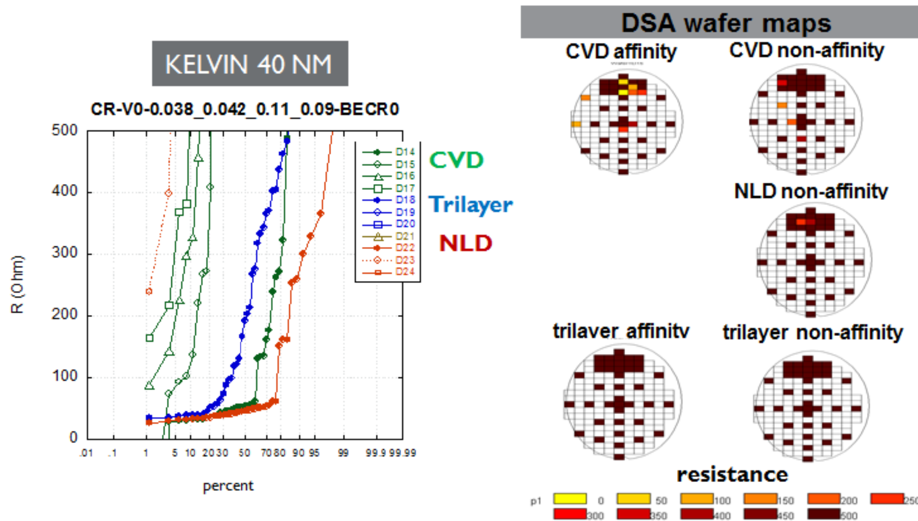

Figure 9. Electrical measurements for control and DSA wafers in the 40nm kelvin structures. Full data points correspond to control and open points to DSA wafers. Slots 15, 16,19 and 20 correspond to template affinity control. The wafer maps for the DSA wafers depicting the resistance per die are also shown. In the resistance scale, yellow means zero resistance and brown means R>500 Ohms.

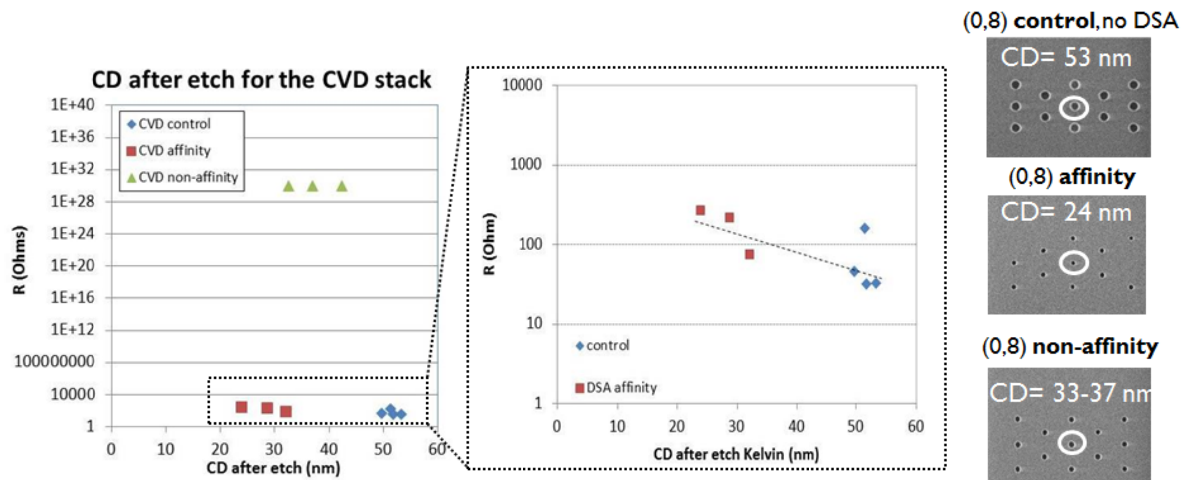

Figure 10. Resistance in function of CD after etch for the CVD control, DSA affinity, and DSA non-affinity in dies (0,6), (0,8), and (2,6). The insert of the graph shows the linear dependence of the resistance with contact hole CD. The CDSEM top-view pictures show the kelvin structures in die (0,8) after etch: only the central hole is active for electrical measurements.

XSEM and FIB cross sections (figure 12) show opening in the STG holes for both CVD and trilayer but this is not the case in the electrical structures. In fact, the kelvin structures in the trilayer stack are not opened at all and in the CVD incomplete transfer is observed. For the particular case of the CVD wafers, the missing contact hole is the only active hole for the single resistance measurement as observed in 10 different FIB images.

Since the Kelvin structures are perfectly opened in the control wafers for both stacks, it is necessary to look into more detail in the BCP assembly in the different stacks and different structures (staggered vs. kelvin). Both the CVD and trilayer have a hydrophilic bottom surface which will lead to preferential PMMA wetting and at this regard they should be similar. As for the structure density, different BCP filling probably occurs in dense versus isolated structures. Additional SEM inspection of staggered, kelvin and chain structures after DSA showed that a 15nm FT is more appropriate for filling the electrical structures although the staggered ones need a 19nm FT film to have good assembly. Of course, this will result in a different etch rate for every structure as observed in the XSEM and FIB analysis. The BCP pattern filling density effect has been observed already in multiple contact-hole BCP assembly[10].

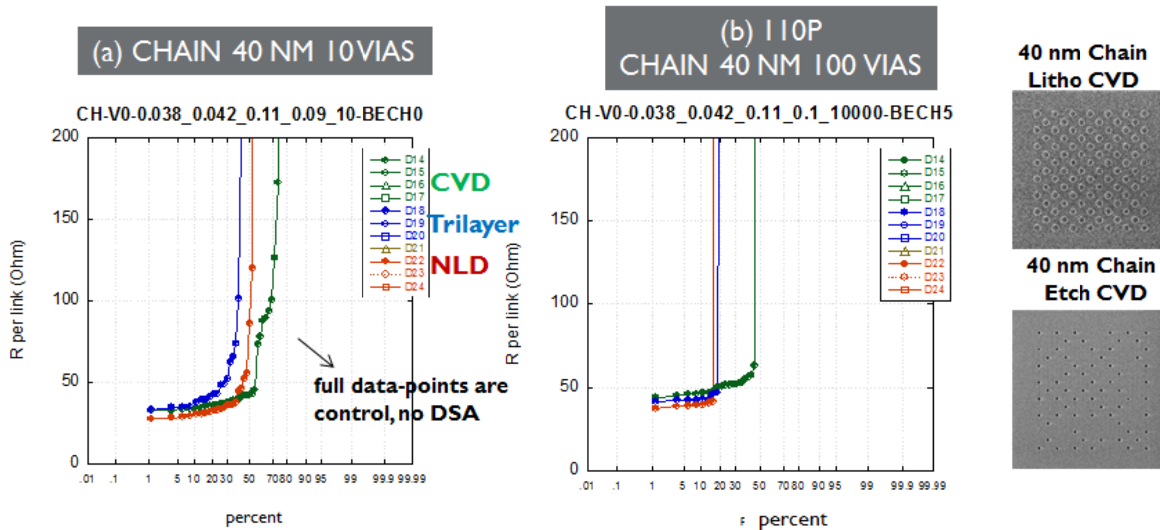

Figure 11. Electrical characterization for control and DSA wafers in the 40nm chain structures for (a) 10 holes and (b) 100 holes. Full data points correspond to control wafers. The CDSEM pictures depict the incomplete transfer of the chain structures, which leads to electrical failure.

	XSEM Staggered DSA Affinity	FIB 40nm Kelvin DSA Affinity	FIB 40nm Kelvin Control
DSA CVD after M1 (0,7) E failure	M1 V0 L12 300 nm	M1 V0 L12 200 nm	Active hole 200 nm
DSA trilayer after M1 (-1,7) E failure	300 nm	200 nm	200 nm

Figure 12. SEM and FIB cross-section images for the staggered (DSA wafers) and kelvin (DSA and control wafers) for the CVD and trilayer stacks in die (0,7). These dies showed electrical failure for the DSA wafers and electrical conductivity for the control wafers.

CONCLUSIONS

An integrated BCP contact-hole shrink electrical test vehicle for enabling sub-30 nm vias has been established. BCP assembly has been improved inside the template with template affinity control. Although transfer was achieved and 4% of the dies showed good conductivity in the standard stack, the differences in BCP thickness for different pattern densities led to incomplete etch in the electrical structures. Continued optimization,

including etch development tailored towards the electrical structures will result in a higher percentage yield of electrical dies.

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