

Integrated Test Solutions




Full Turnkey Services from Bump, Wafer Probe, Assembly, Final Test, Post Test and System Level Test to Drop Shipment



As one of the largest test outsourcing providers, we offer a full suite of test platforms and engineering services to support a broad range of mixed signal, RF, analog and high-performance digital semiconductor devices for the communications, digital consumer and computing markets. We combine operational efficiencies with proven test capabilities to achieve the lowest cost of test with the highest possible throughput and faster time-to-market.



Test Platforms

	Teradyne	Advantest	LTXC
 DIGITAL & MIXED SIGNAL	UltraFLEX iFLEX J750 Catalyst	PS400 PS800 PS1600 T2000 (GEN1, EPP)	Fusion CX
 RF	UltraFLEX iFLEX Catalyst	PS800 PS1600	Fusion CX
 MEMORY	Magnum	T5503	

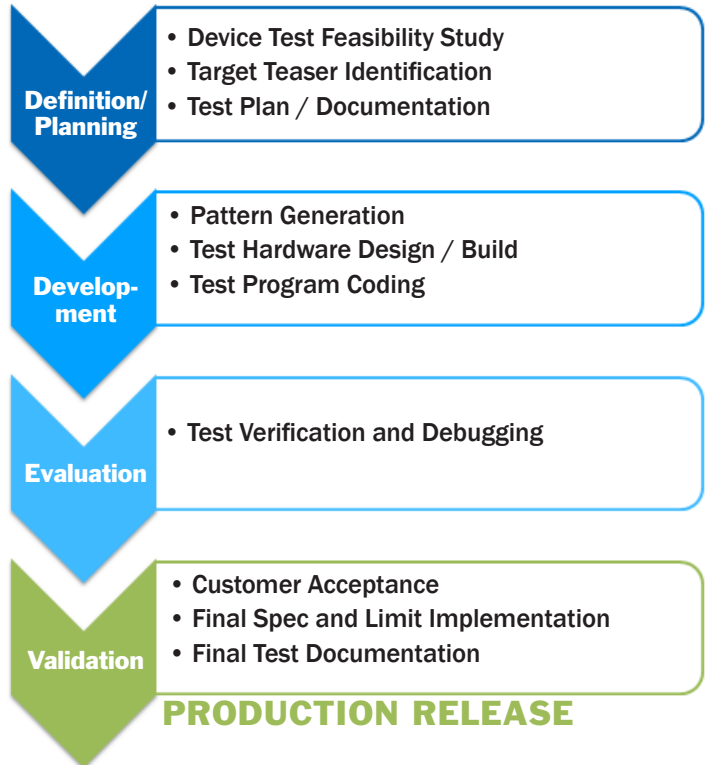
Test Engineering Services

Our experienced R&D and test teams have helped customers reduce their engineering burdens and prepare products for high volume manufacturing in the shortest time possible. Our world class test development and test program migration services include:

- Test program development, debug, optimization and validation
- Device characterization
- First silicon characterization (Wafer Probe)
- Probe card design, fabrication and qualification (Wafer Probe)
- Load board design, fabrication and qualification (Final Test)
- Prototype evaluation
- Multi-site migration to higher parallel testing
- Test program conversion to new tester platform



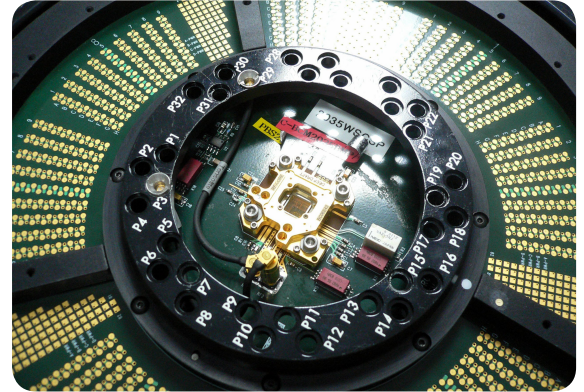
NEW PRODUCT



Wafer Probe

Wafer Probe is a critical step in semiconductor manufacturing due to the need to maximize device throughput, yield and quality in order to reduce the overall cost of test. We operate some of the highest precision probers available in the industry. Our probe services include, but are not limited to:

- Probe card design, development and maintenance
- Copper pillar bump wafer probe
- Known Good Die (KGD) testing for System-in-Package
- Prober network customization to support real-time data
- Fine-pitch, RF, bump, thin wafer probing
- Multiple site (x128) probing
- 3 row staggered / sample
- Advanced fabrication wafer node
- 300mm (12") or 200mm (8") wafer probing



Final Test and Post Test

Every stage of the manufacturing process is critical and test automation is an important differentiator. We have a Next Generation Final Test Cell and highly automated Post Test systems that achieve extremely high throughput while maintaining a zero defects standard of quality. Whether you require production with minimum or full engineering support, we can provide:

- Multi-site implementation: x32 (Digital), x320 (Memory), x16 (Mixed Signal), x8 (RF)
- Testing advanced wafer level packages
- Testing silicon-based Integrated Passive Devices
- Yield enhancement with monitoring and feedback
- Test time optimization
- Wafer sort to final test correlation feedback
- Quick-turn failure analysis
- Reliability services (i.e., ESD, latch-up and HTOL)
- Handlers with Active Thermal Control (ATC)



System Level Test

We offer comprehensive test services for System-in-Package (SiP) and miniaturized modules including:

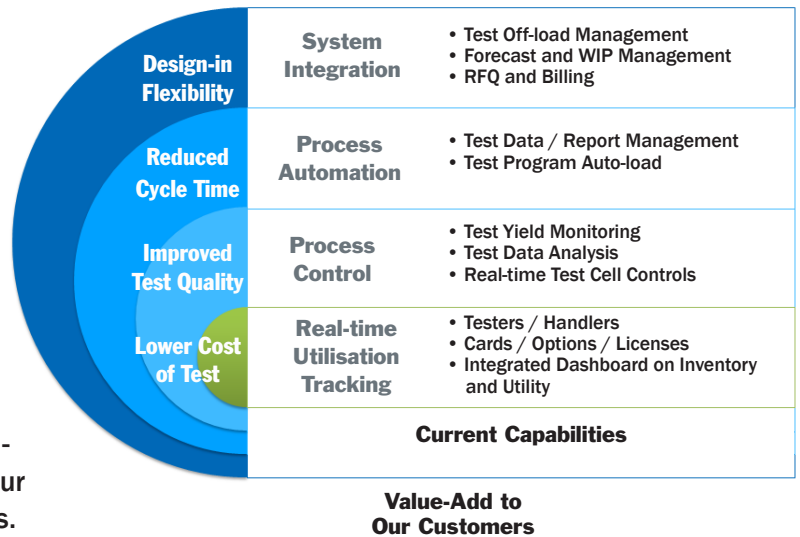
- Test program and hardware development
- Expertise in Digital, Mixed Signal and RF test solutions
- Characterization of SiP and modules
- Quick-turn failure analysis
- Cost effective ATE test platforms
- Extensive custom SLT solution experience
- Highest overall equipment effectiveness (OEE) in the industry with real-time machine down detection
- Latest technology on ATE and handler to support various package form factors



Integrated Test Management System (ITMS)

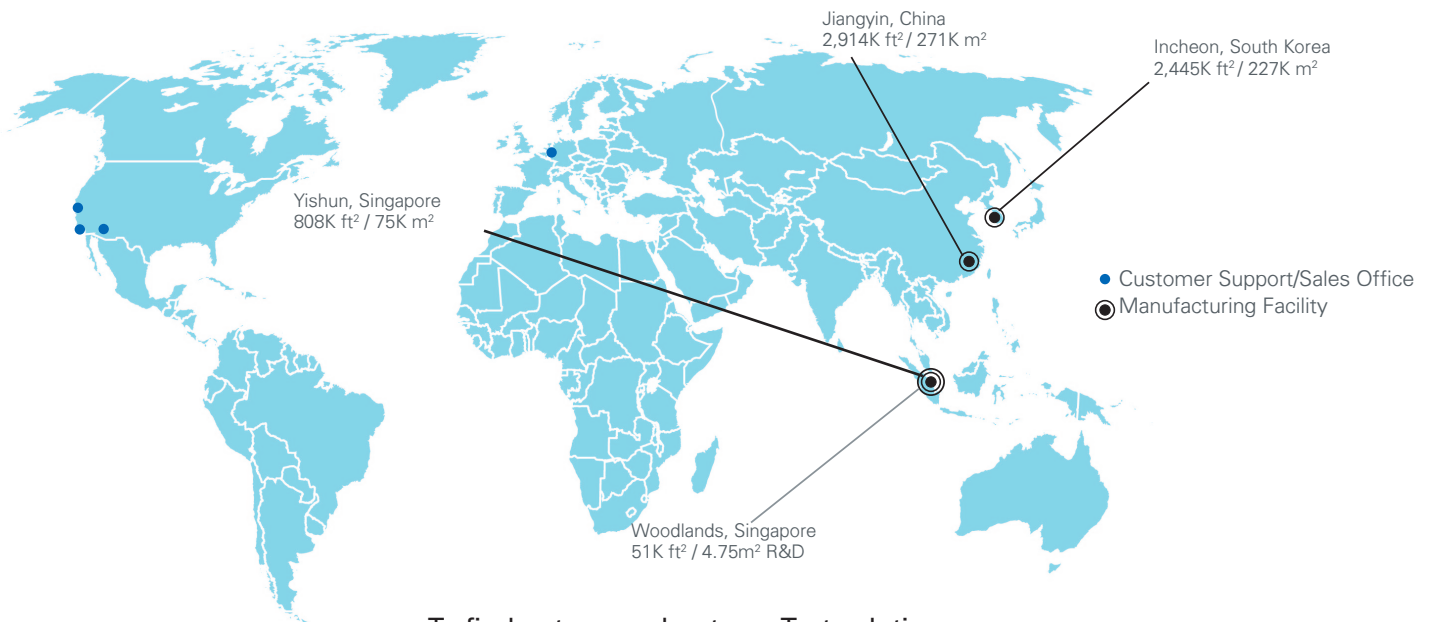
Our test capabilities include an innovative Integrated Test Management System (ITMS) that efficiently and effectively integrates the test systems and business processes with all of our factories to achieve the highest levels of quality and throughput with a lower cost of test.

ITMS automates test systems and manufacturing processes in order to eliminate manual steps, reduce cycle time and provide an automatic closed-loop control process with real-time data analysis and monitoring. ITMS helps our customers gain significant yield improvements as well as the design-in flexibility of having their devices tested in any of our factories while receiving the same successful results.



Flexible Test Services to Meet Your Needs

We specialize in full turnkey test solutions that are supported in multiple geographies. Since 1999, we have provided world class test development and proven test experience in RF, mixed signal, digital, memory and integrated system-on-chip (SOC) devices. We also offer Wafer Sort only or Final Test only options to meet your unique test requirements. If you are looking for a test provider who can deliver a lower cost of test, proven test quality, design flexibility, higher yields, reduced cycle time and a broad geographic footprint, we have a solution for you.



To find out more about our Test solutions, visit us online at www.statschippac.com or www.jcetglobal.com.

STATS ChipPAC Pte. Ltd.

www.statschippac.com or www.jcetglobal.com

The JCET logo is a registered trademark of Jiangsu Changjiang Electronics Technology Co., Ltd.. Trademark registered in the People's Republic of China (registration number: 3000529). All other product names and other company names herein are for identification purposes only and may be the trademarks or registered trademarks of their respective owners. STATS ChipPAC disclaims any and all rights to those marks. STATS ChipPAC disclaims all warranties and makes no representations regarding the accuracy, completeness or suitability of the information given in this document, or that the use of such information will not infringe on the intellectual rights of third parties. You should seek professional advice at all time and obtain independent verification of the information contained herein before making any decision. Under no circumstances shall STATS ChipPAC be liable for any damages or losses whatsoever arising out of the use of, or inability to use the information in this document. STATS ChipPAC reserves the right to change the information at any time and without notice. ©Copyright 2018. STATS ChipPAC Pte. Ltd. All rights reserved.

