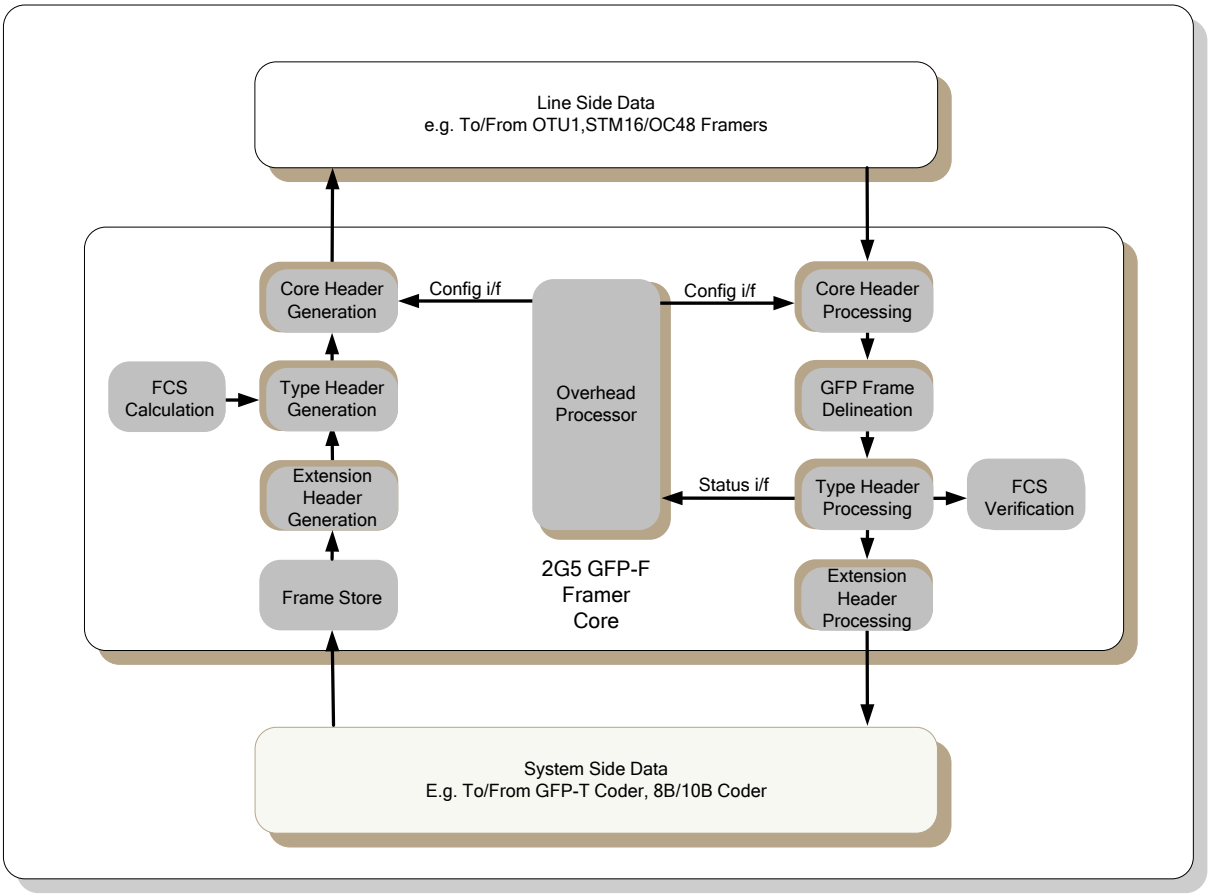
2G5 GFP-F (Framer)
Product Brief

Overview

Aliathon's 2.5Gbps GFP-F Framer Core provides a flexible, resource-efficient, high-density programmable logic based solution for GFP interfacing. Running at over 166.62MHz, it provides GFP-F Frame generation and delineation for 2.6Gbps data streams.

Block Diagram



Key Features

- Compliant with ITU-T G.7041 specification.
- Best-in-Class size and performance with multiple FPGA vendor support.
- Interfaces to 2.6/2.5 gigabit data sources, such as Aliathon's OTU1 and STM16 framer cores. Combines with Aliathon's GFP-T Block Encoder core for GFP-T solutions, or may be used stand-alone for GFP-F solutions.
- Generates/Synchronises to a 16-bit wide GFP data stream including IDLE frames.
- Provides GFP scrambling/descrambling.
- Generates/Processes Core, Type and Extension headers.
- Generates and inserts a 32-bit FCS. Verifies received 32-bit FCS.
- Calculates HEC for Core, Type and Extension headers.
- Implements single-bit error detection and correction for Core, Type and Extension headers.
- Full Overhead and Defect processing including:
- Core HEC error, Type HEC error, Extension HEC error (for all of them detects correctable or uncorrectable).
- Performance Monitoring Counters (Correctable HEC Errors, Uncorrectable HEC Errors).

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Resources

Framer (Tx)	
FFs	660
LUTs (4-Input)	760
Memory (kbit)	46.1
Deframer (Rx)	
FFs	720
LUTs (4-Input)	1070
Memory (kbit)	0
OH Processor	
FFs	200
LUTs (4-Input)	200
Memory (kbit)	2
Total (1)	
FFs	1580
LUTs (4-Input)	2030
Memory (kbit)	48.1
Fmax (2)	
> 170 MHz	

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.
Memory implementation is device dependent and figures may increase on less memory efficient architectures.
Memory figures may be reduced at the expense of logic on some architectures.
2 - Guideline Performance figures are based on the slowest Speed Grade of the high performance devices and may be less for slower, lower cost, devices.

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