Wafer Test
Value & Future

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Value

"What is Wafer Test Creates"

- Pass / Fail Result
- Wafer MAP Generation
- Fuse Repair
- Calibration

Circuit / Mask Design

- Yield Data
- All Test Data

Wafer Fab

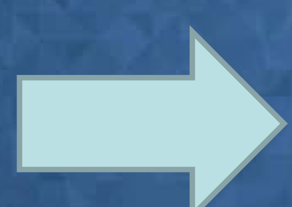
- Yield(Pass/Fail)
- Fail BIN
- Wafer MAP
- Failure Analysis

PKG/Direct Mount

- Save Yield Loss
- KGD Solution
- Wafer MAP

Value of Wafer Test

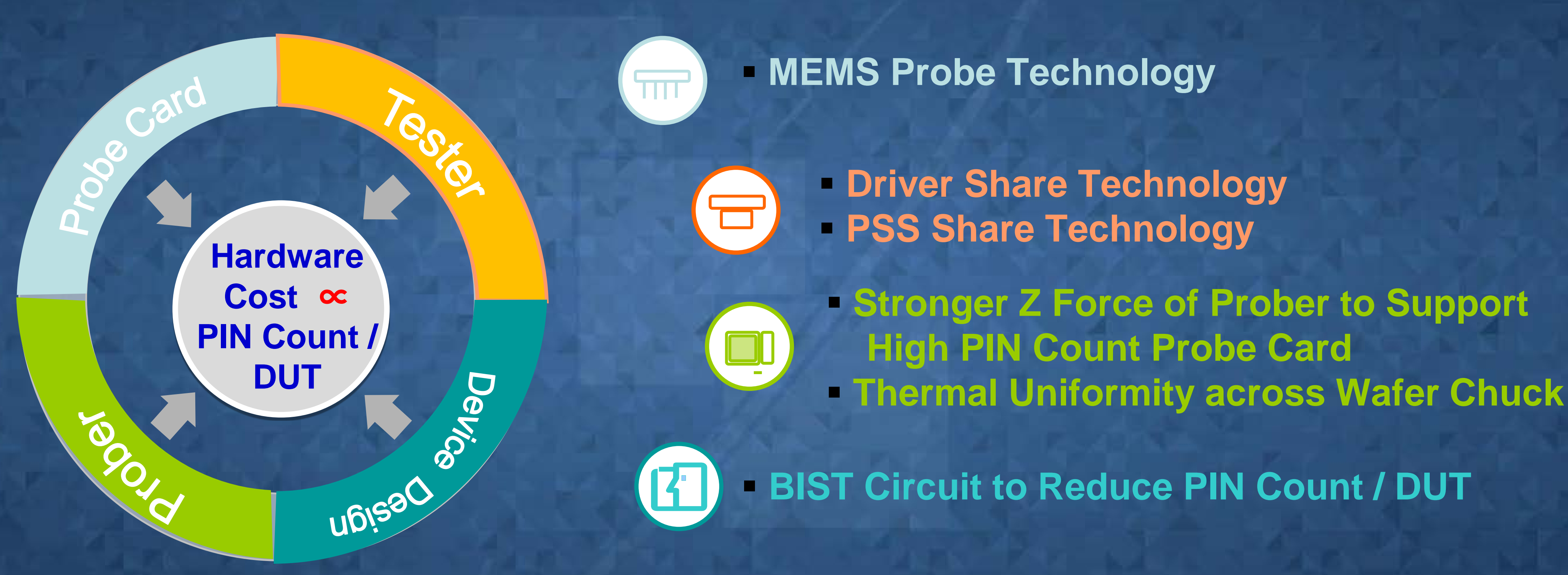
Always Under Pressure of Test Cost Reduction



- **Provide Data for Wafer Fab. Condition**
  - Until wafer test is completed, hard to tell which is good die.
- **Provide Data to Improve Circuit Design & Mask Layout.**
- **Keep High Yield by Repair**
- **Make Adjustment by Calibration**
- **Realize High Density Multi Die PKG by KGD Testing Solution**
- **Minimize Yield Loss at Final Test**

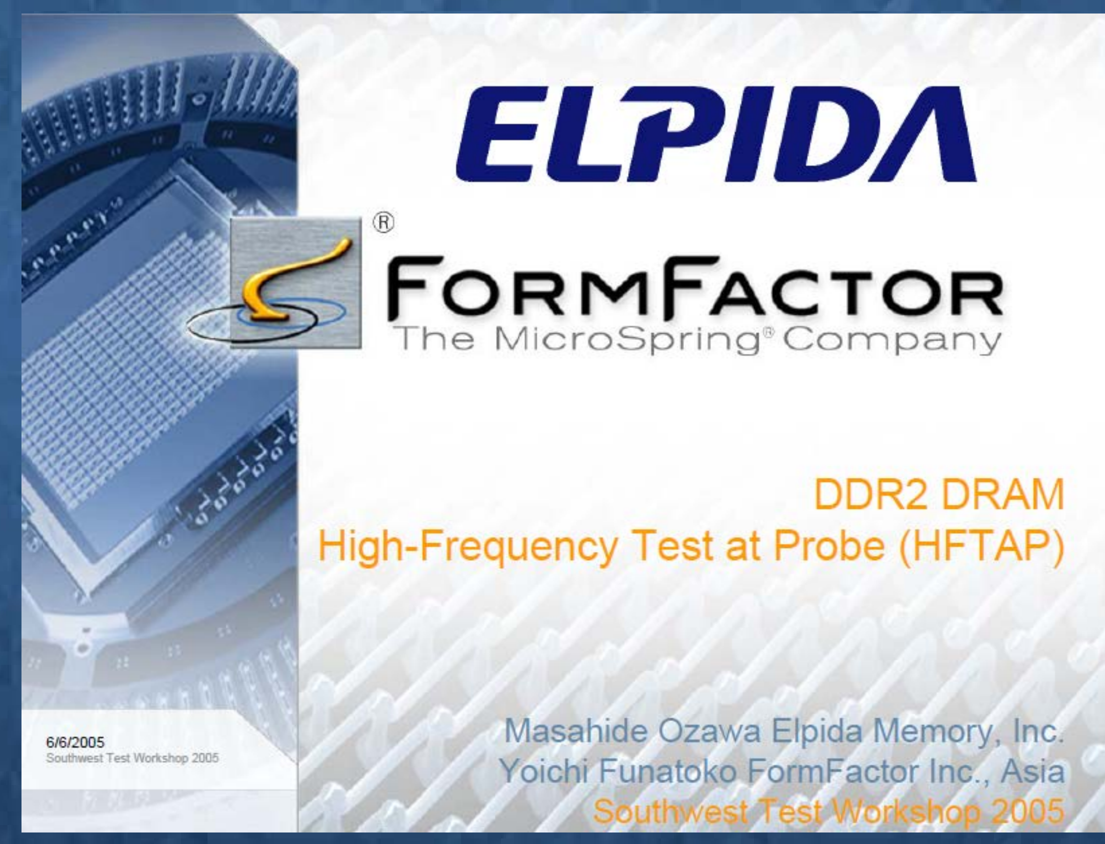
Multi DUT & High-Speed Testing

Technologies for Multi- DUT



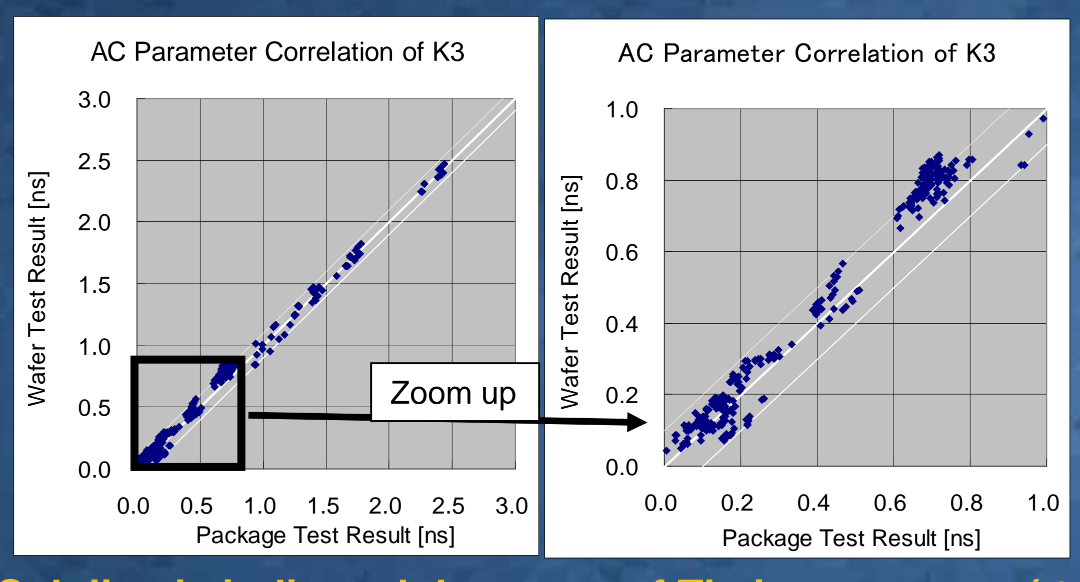
SWTEST 2005

DDR2 DRAM
High – Frequency Test at Probe (HFTAP)



Elpida Evaluation: Correlation (AC parameters)

- **Test Item: AC Parameters (setup, hold, TCK etc.)**



These are evaluated at high temperature with Vdd set in 3 points.

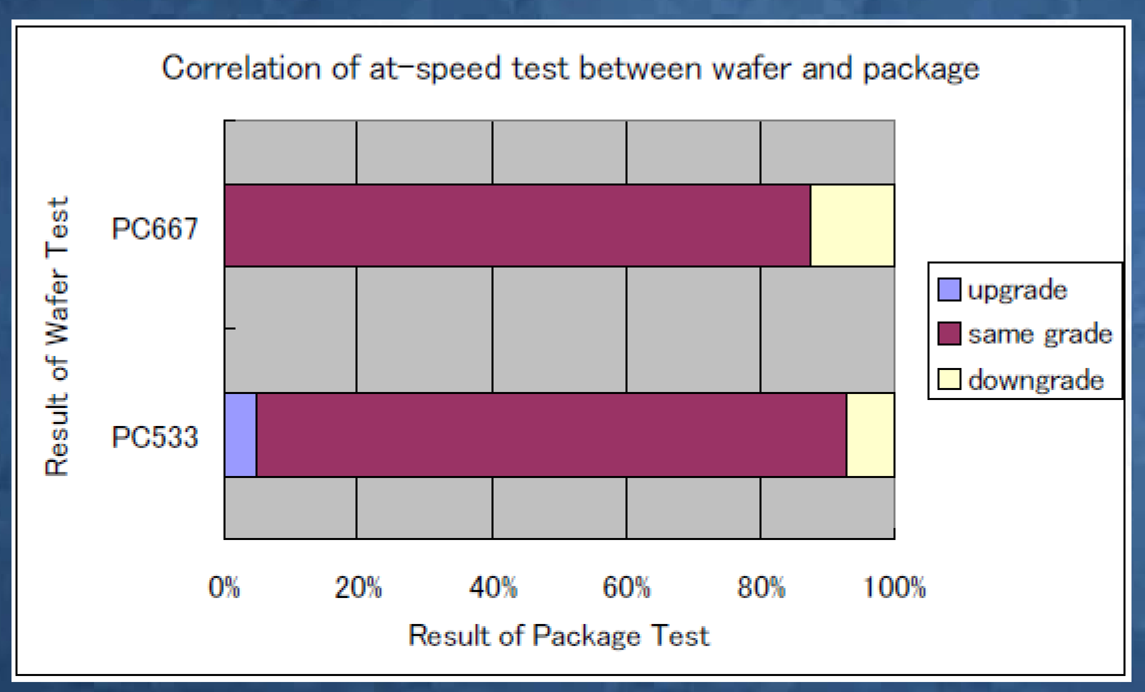
※Sub line is indicated the range of Timing accuracy (±100ps)

Compared by package test result
Different 100ps～150ps for some test items.

Available for testing with adjustment.

Elpida evaluation: At-Speed Test

Correlation Result

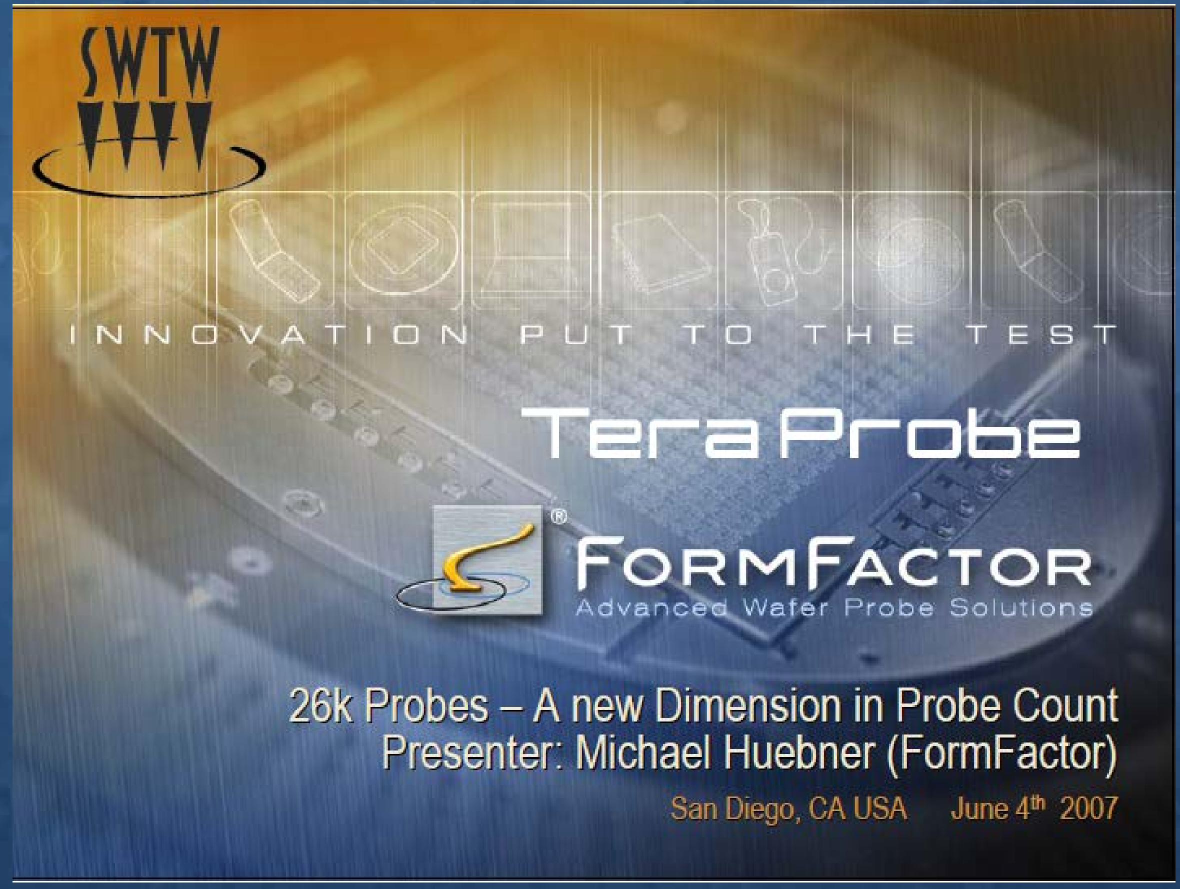


Correlation test result was similar with Final Test.

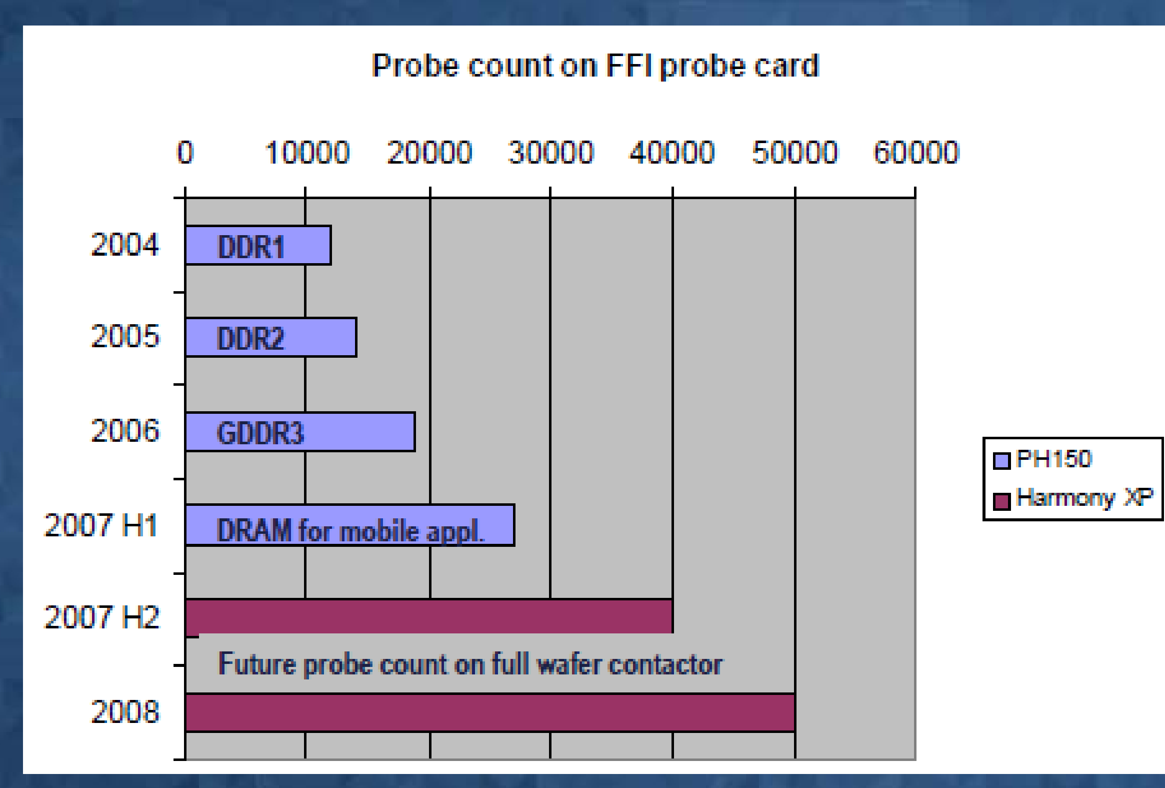
K3	Correlation Ratio
	87.0%

SWTEST 2007

26k Probes – A New Dimension in Probe Count



Industry Probe Count Trend

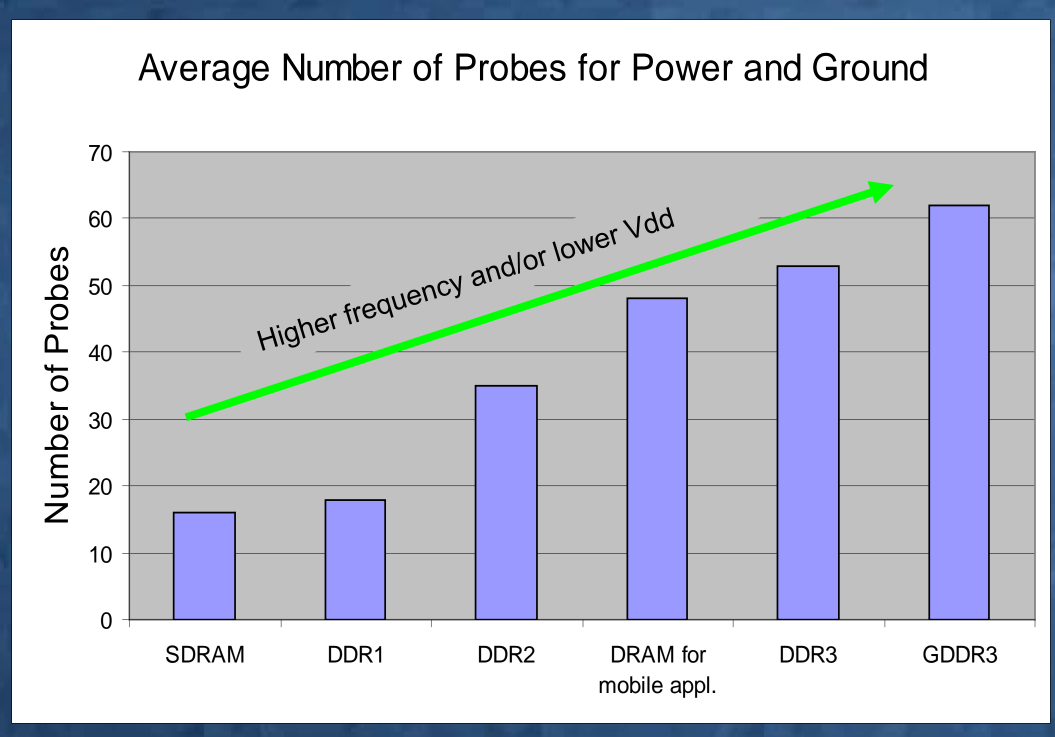


※This data is based on FFI's whole customer base

- Total probe count has increased significantly over the last years
- This increase was not driven by increasing parallelism
- However parallelism is expected to increase to 384 DUT and higher
- This will act as a multiplier on the total probe count leading to 40 - 50k probes

Industry Probe Count Trend

- Number of probes per DUT is increasing



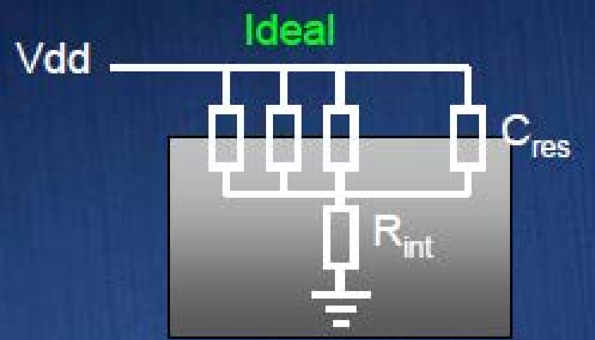
※This data is based on FFI's whole customer base

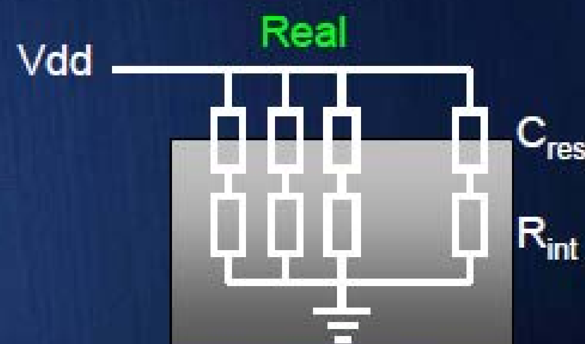
Mainly Power and GND
– especially VDDQ and VSSQ (Output driver)

Number of signals used for high parallel wafer sort has not changed significantly for most applications

Improved Power Delivery *Static (DC) Case*

- Low and stable Contact Resistance (C_{res}) is a must
- Use all power and ground pads available on the chip
  - $C_{res} = 1/(1/C_{res1} + 1/C_{res2} + \ldots 1/C_{resN})$ - this assumes perfect power distribution on chip
  - In reality some probes carry most of the current
  - Bad contact performance can be compensated by high probe count only to some extent





- Voltage drop is function of C_{res} and current: $\Delta V = C_{res} \times I_{dd}$
  - With lower Vdd the tolerable voltage drop ΔV is also decreasing

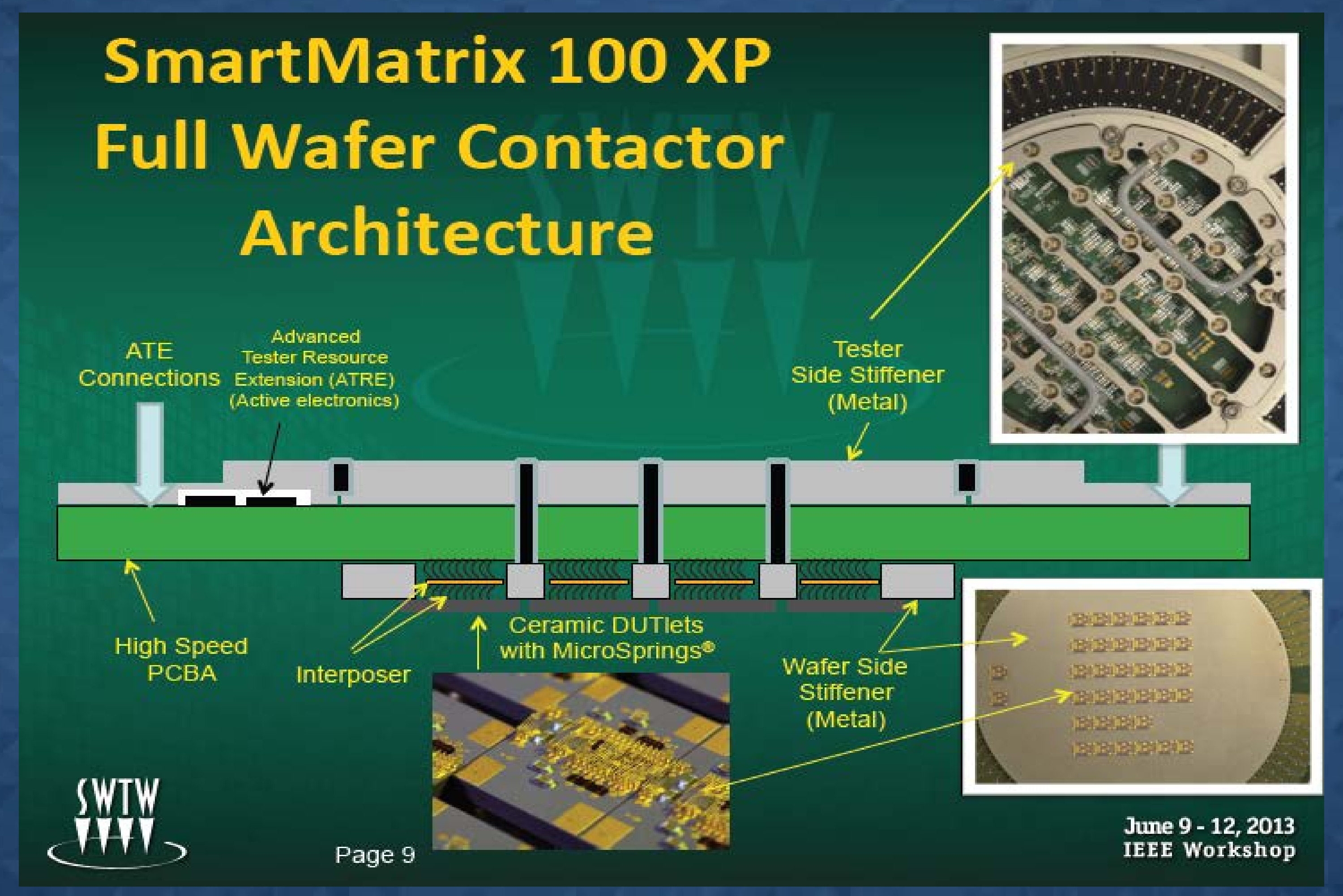
Need full spring population and low C_{res} on every single probe for best performance

SWTW 2007 - 9 - Tera Probe and FormFactor

SWTEST 2013

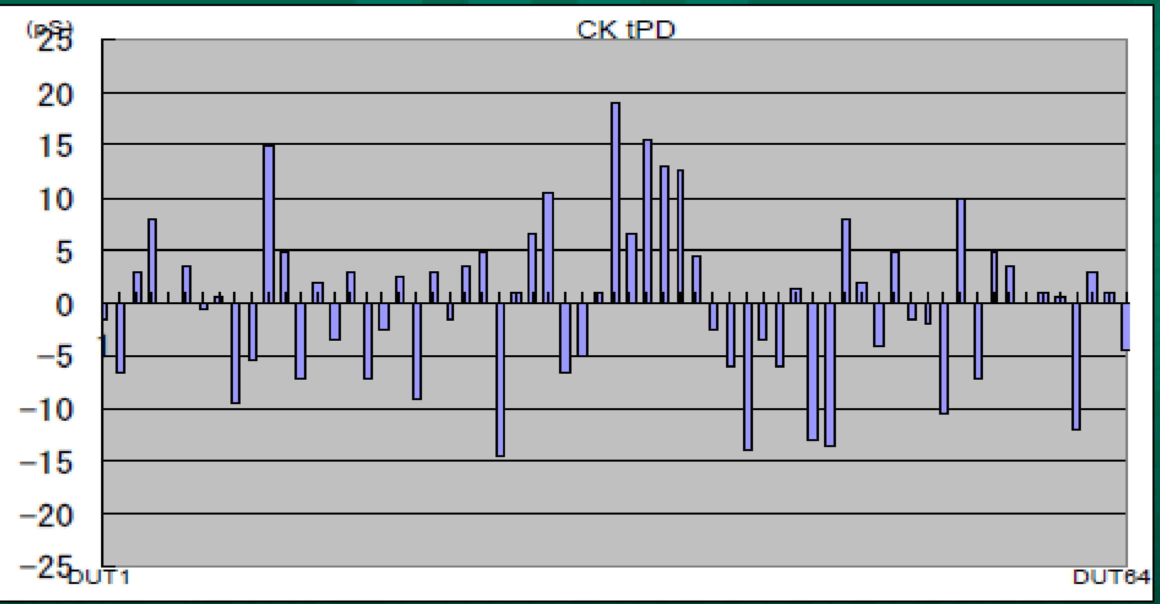
LPDDR2 and LPDDR3 High Speed Wafer Test for KGD

Smart Matrix 100 XP Full Wafer Contactor Architecture



Skew

- Probe card skew specification
  - ±50pS for single ended signals

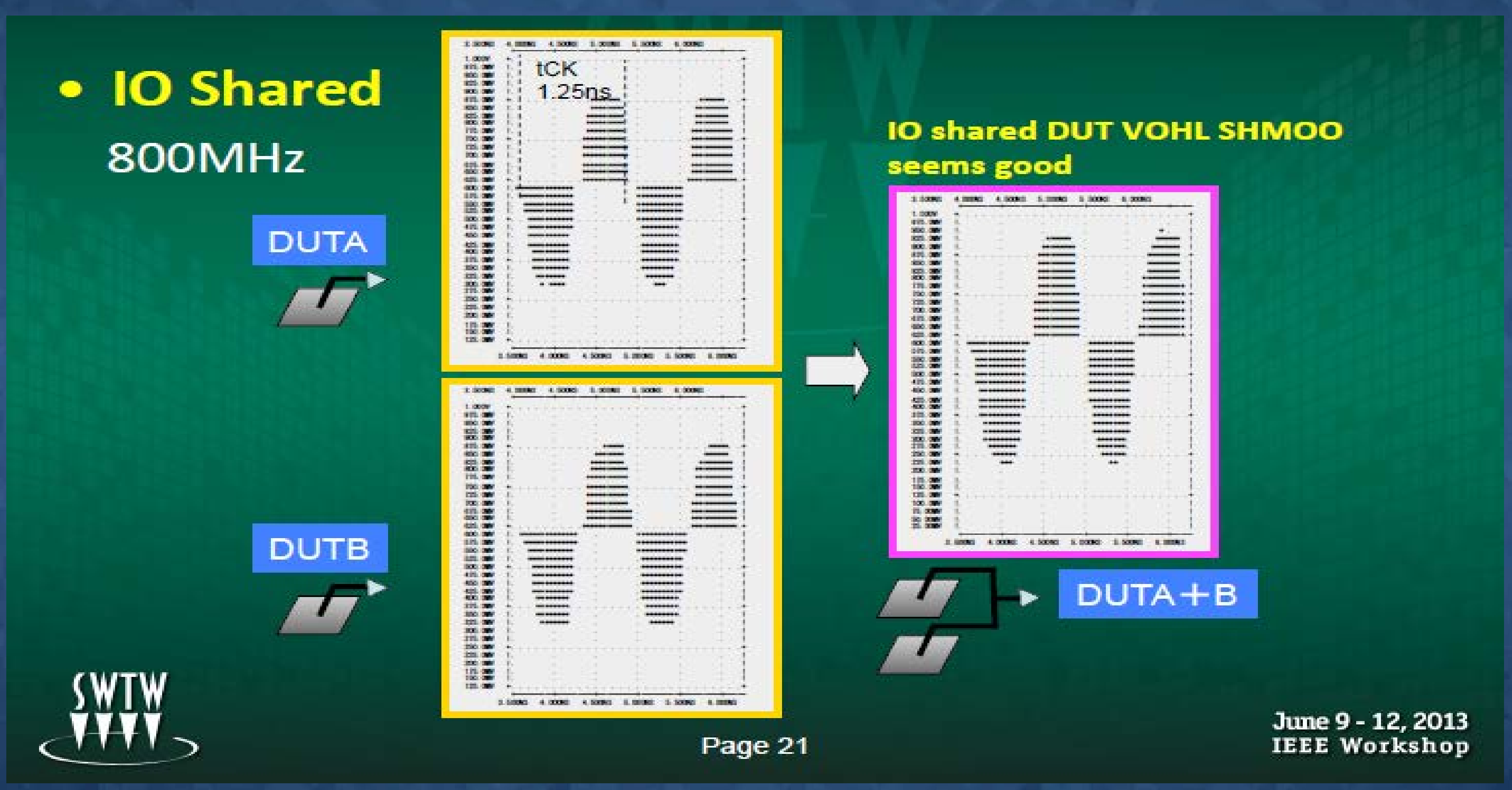


CK TPD is within 20ps for this Card(LP2).

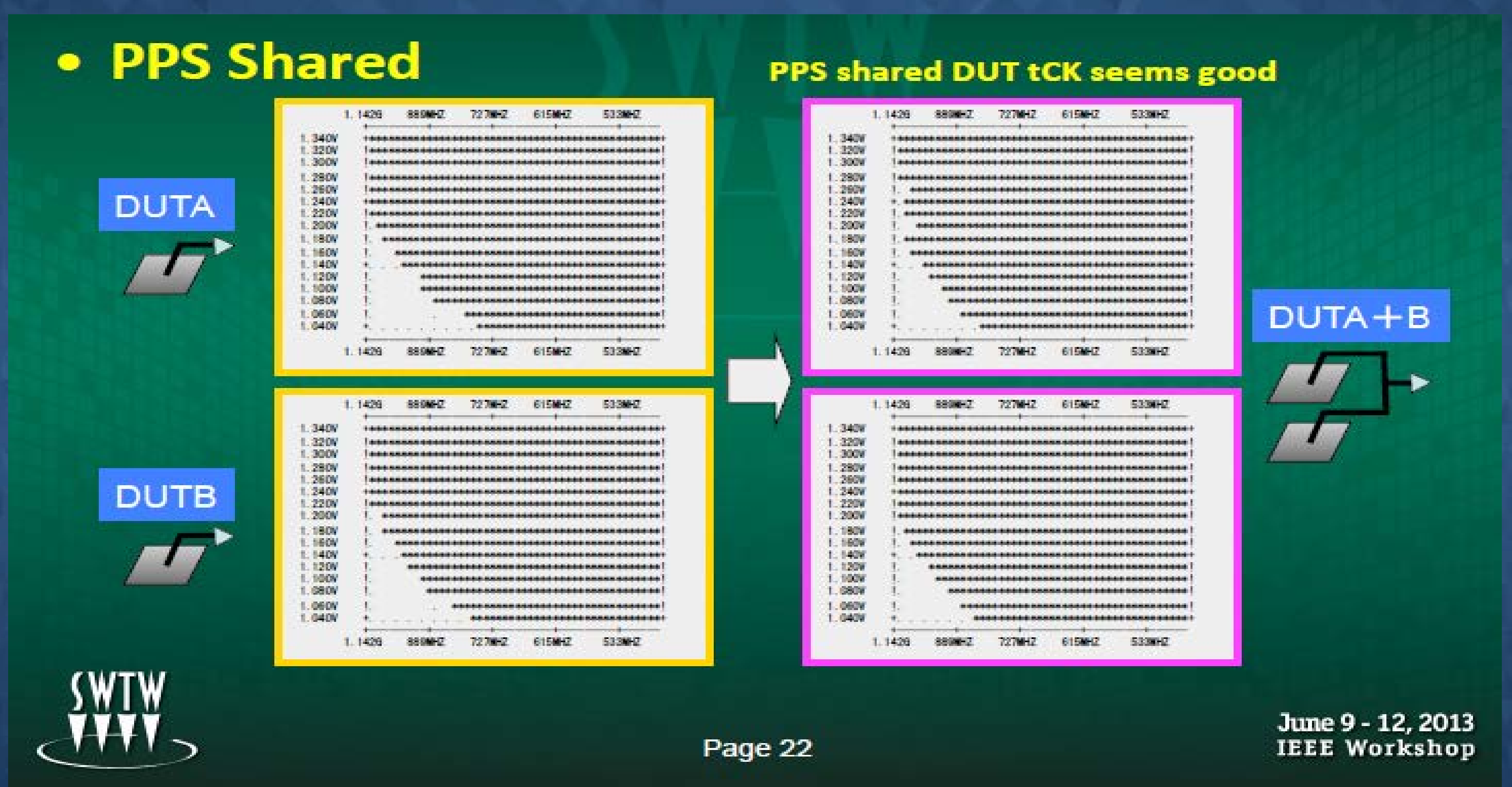
Page 16

June 9 - 12, 2013
IEEE Workshop

Enhance Parallel DUTs



Enhance Parallel DUTs



How Multi-DUTs Probing Worked

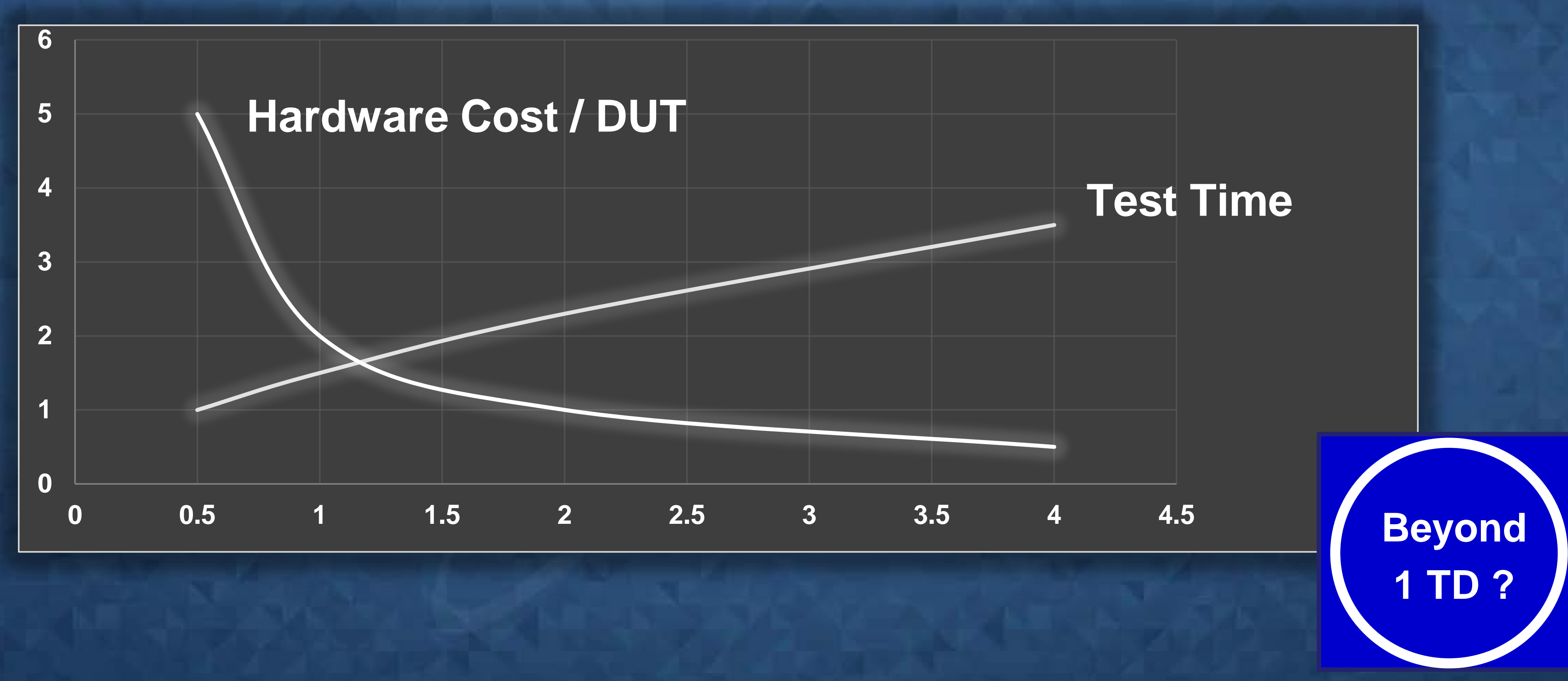
Hardware cost was reduced ~90%/DUT.

1TD was achieved for NAND Flash first and in few years for DRAM.

Beyond 1TD technology had been one of the big concerns and Multi - Stage prober was developed.

Multi DUTs Test for Memory

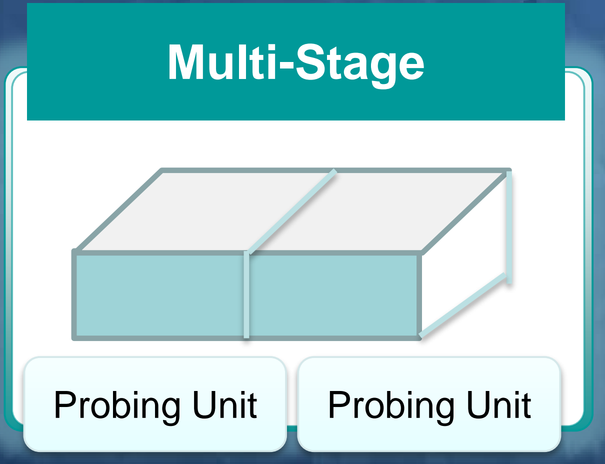
Hardware Cost / DUT were reduced to 1/10 from late 1990 to 2010 by Multi DUTs Technology

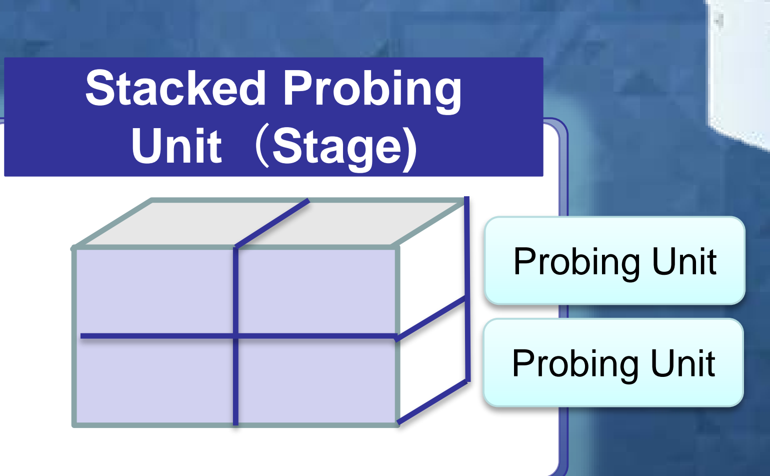


Multi Stage Test

Beyond 1TD

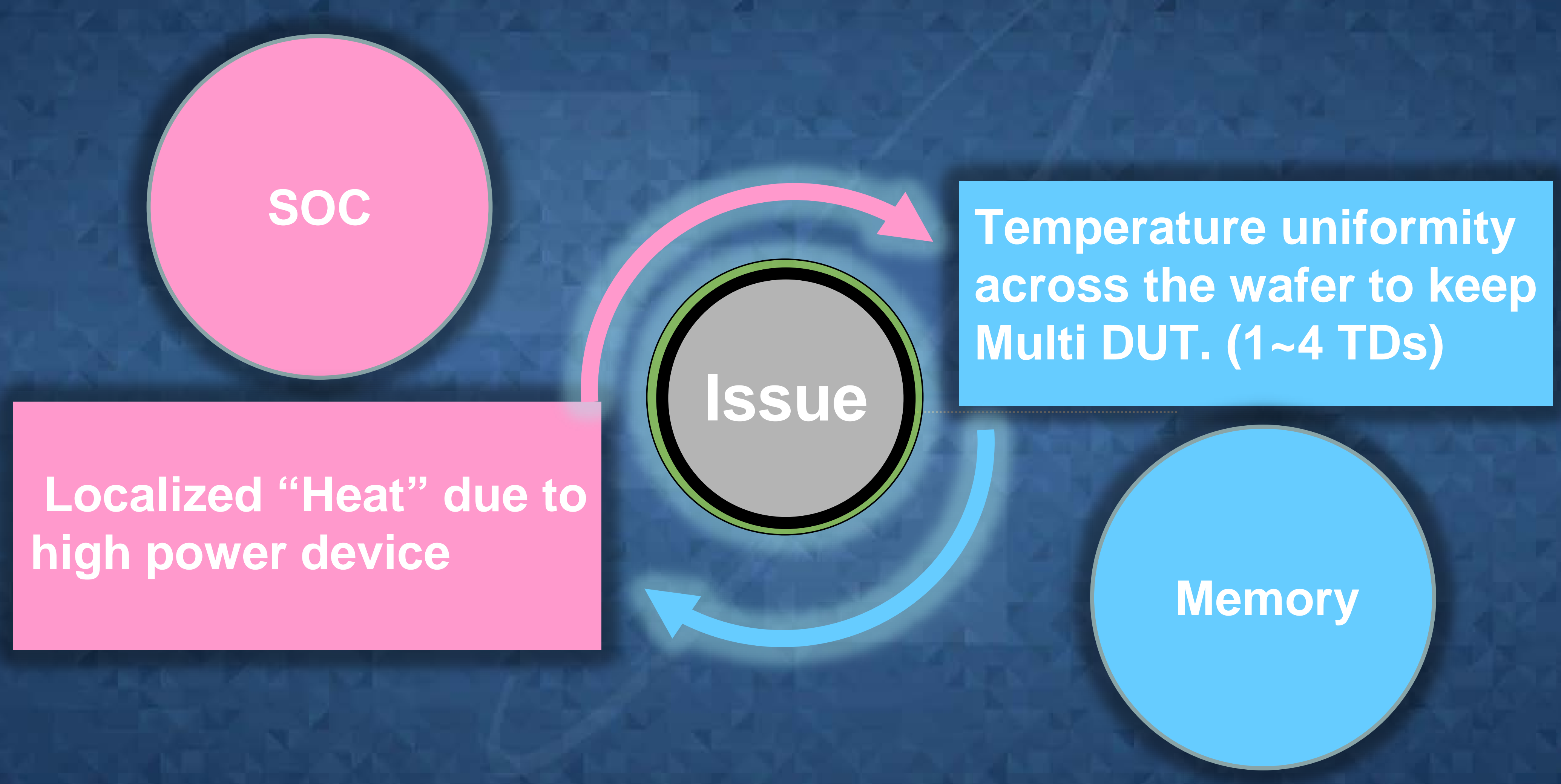
Multi-Stage Probing





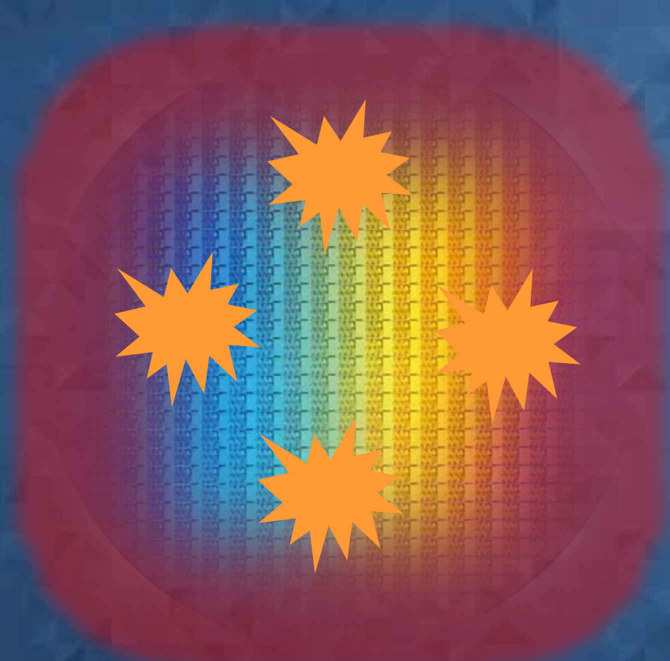
Required Technology for Future

Issues for “High Power” Device

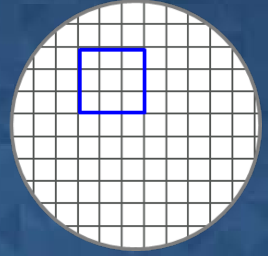


Issue of Multi DUTs Testing

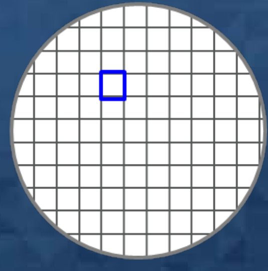
(For High Power High Pin Count Device)



Heat of 1 Die Affects Testing Temperature effect to of Other Die

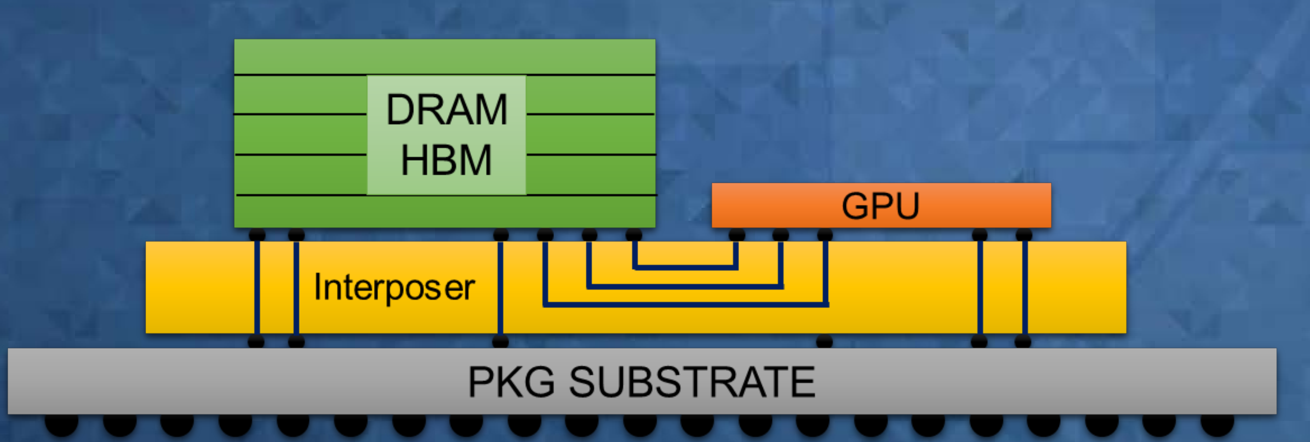


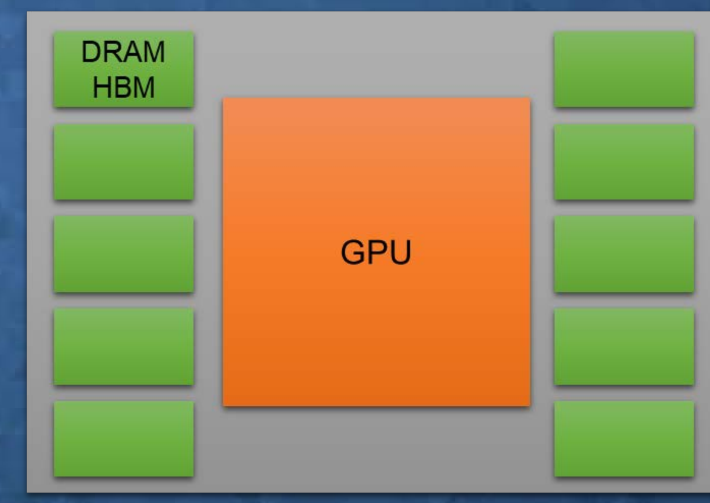
High Power Device Tends to Be Single Die Probing



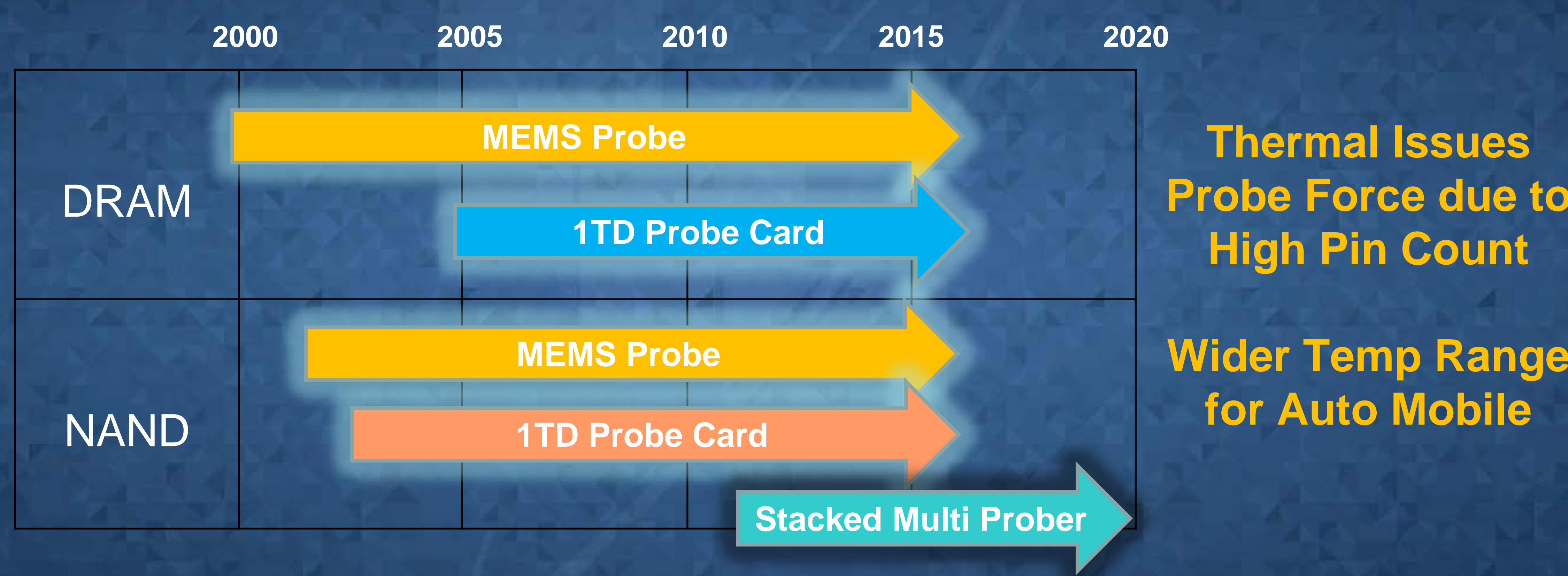
Demand for "KGD" Solution

System Is Getting Smaller and Heat Density & Cost Is Higher



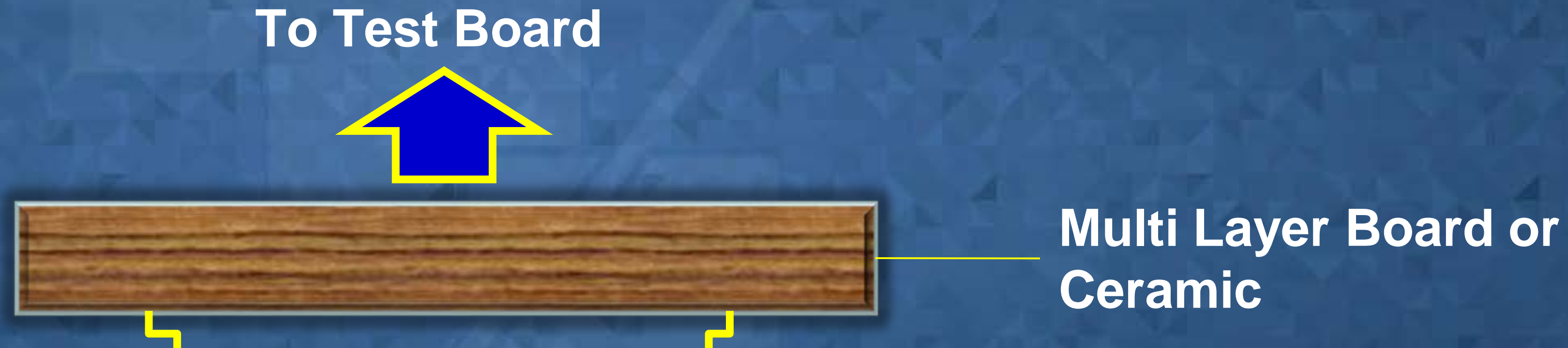


Trend of Memory Device Wafer TEST



Single Board Probe Card

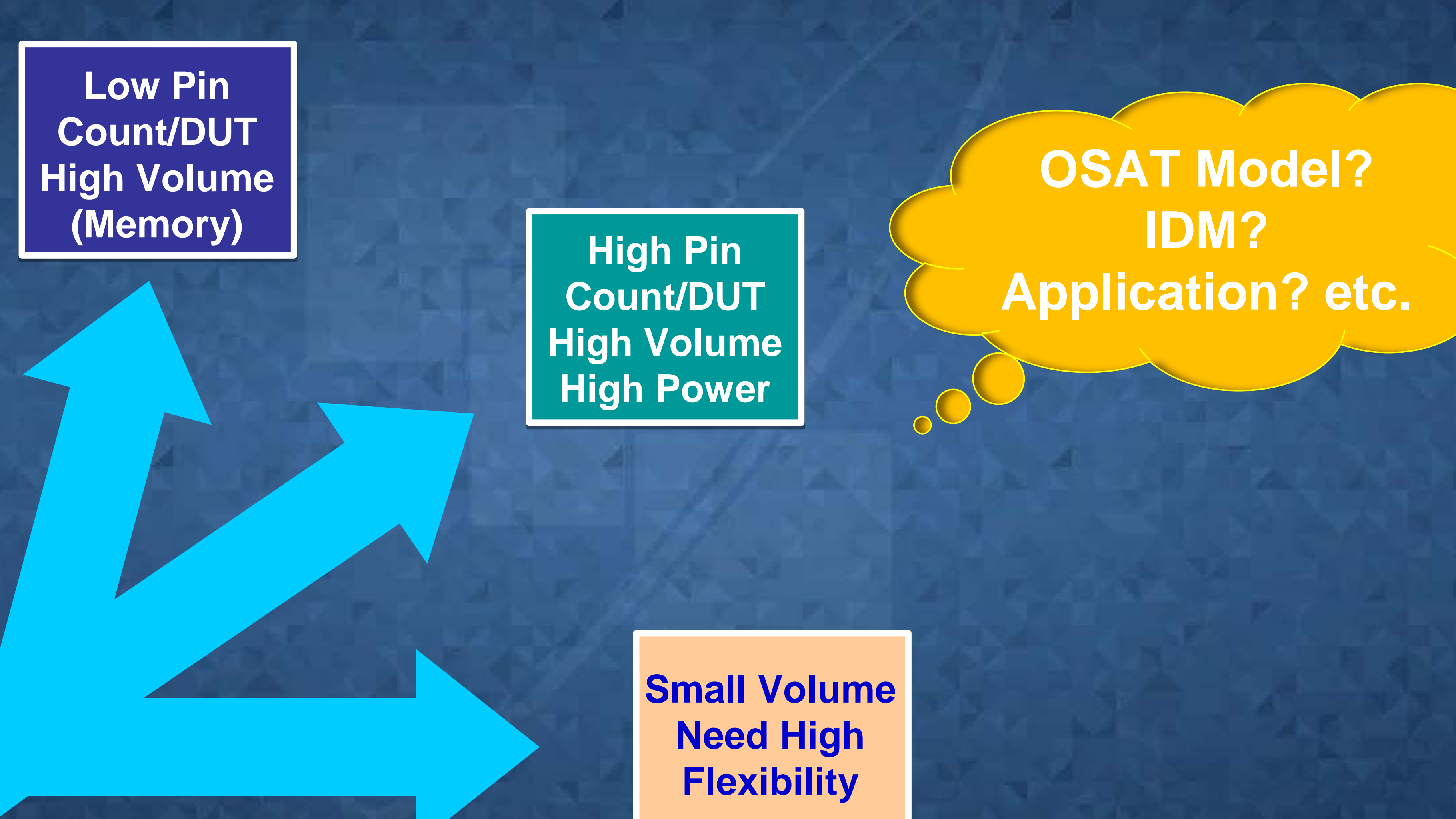
Lower Cost Test Board Has to Have Flexibility for Multi Product



Increasing Value of Wafer Test and Technical Variation

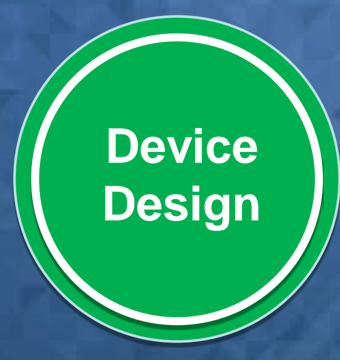
Tailor Made Equipment & Probe
Wide Variation of Probe Card

Variation of Technology Choice



Teamwork for Future

Strong Teamwork is Required For Future.



Friendship & Business

SWTEST Provides Great Opportunity to Establish New Friendship & Business Relation

Thank You !
Q&A !