Wettable-Flanks: Enabler for The Use of Bottom-Termination Components in Mass Production of High-Reliability Electronic Control Units

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Abstract

Driven by miniaturization, cost reduction and tighter requirements for electrical and thermal performance, the use of lead-frame based bottom-termination components (LF-BTCs) as small-outline no-leads (SON), quad-flat no leads (QFN) packages etc. is increasing. However, a major distractor for the use of such packages in high-reliability applications has been the lack of a visible solder (toe) fillet on the edge surface of the pins: Because the post-package assembly singulation process typically leaves bare copper leadframe at the singulation edge, which is not protected against oxidation, and thus does not easily solder-wet, a solder fillet (toe fillet) does not generally develop.

Solder-joint robustness is also increased by the presence of a robustly wettable singulation edge, but this is not the primary benefit (the number of cycles to failure under thermal cycling is typically decreased by up to about 20 %, in the absence of an outer, visible fillet). Users, primarily those involved in the mass production of high-reliability, mission-critical, e.g. automotive, applications, have insisted that a solder fillet be visible at the outer edge of each contact to enable a robust inspection for wetting failures by automatic optical inspection (AOI). The possibility to inspect the integrity of the solder joints by AOI avoids the need to employ X-ray inspection methods, which involve additional costs and layout restrictions, as certain keep-out zones for traces and components are necessary for avoiding disturbing effects in the solder joints X-ray images.

Package suppliers have responded to these needs with various pin modifications that enable a portion of the terminal-edge surface to remain plated after singulation, as two-step sawing or dedicated etching processes. However, for such pin modifications to be useful in the context of AOI under series production conditions, the pin modifications must meet certain geometrical requirements, in order to robustly distinguish a wetted pin (‘good solder joint) from a non-wetted pin (‘defective solder joint’) in AOI. These geometrical requirements will be investigated in this work considering also typical assembly-related process variations. The geometrical requirements enabling robust AOI of LF-BTCs in mass production will be derived.

Introduction

Lead-frame based bottom-termination components (LF-BTCs) are omnipresent in today’s consumer electronics. They combine various advantageous properties, as low mass-production costs, a low thickness (< 1 mm), a very compact footprint and excellent electrical and thermal performance. With packages sizes ranging from about 12 x 12 mm with about 100 I/Os down to less than 1 x 1mm with 4 I/Os , these packages can accommodate various electrical functions as microcontrollers, converters, bridge drivers etc. Provided that proper care is taken in printed-circuit board (PCB) and stencil design, these packages also exhibit a very robust processability, resulting in very low failure rates in production [1].

These advantageous properties make such packages also interesting candidates for use in high-reliability, mission critical applications, in particular if miniaturization is a main design driver. However, the absence of a visible solder (toe) fillet on the edge surface of the pins has been a major distractor for the use of such packages in high-reliability applications. The post-package assembly singulation process, i.e. either sawing or punching the individual devices from the processed leadframe strip, typically leaves bare copper leadframe at the singulation edge. As the bare copper resulting from the singulation operation is not protected against oxidation, and thus does not easily solder-wet, a solder fillet (toe fillet) does not generally develop: Depending on parameters like storage time and environmental conditions, wetting of the bare copper at the toe may occur for more than 90 % of the pins, but under standard mass production conditions a robust wettability of the bare copper

surfaces cannot be ensured. In fact, J-STD-001, recognizing absence of a continuous solderable surface, does not require the presence of a toe fillet for LF-BTC solder joints (cf. Section 7.5.15 of J-STD001F; [2]).

Even though a good solder joint, satisfying requirements imposed by J-STD001, may have developed on the bottom side of the pin, a toe fillet may be lacking. It is thus impossible to distinguish a good pin solder joint from a defective solder joint, where a wetting failure has occurred (i.e. the pin has not been wetted by solder), by checking the presence of a toe fillet with automatic optical solder-joint inspection (AOI); see Figure 1 for an example. Scrapping or reworking all components where outer fillets are missing is not an acceptable option, as it would result in unacceptably high costs - the lack of a toe fillet can occur for even a few percent of the pins (see above).

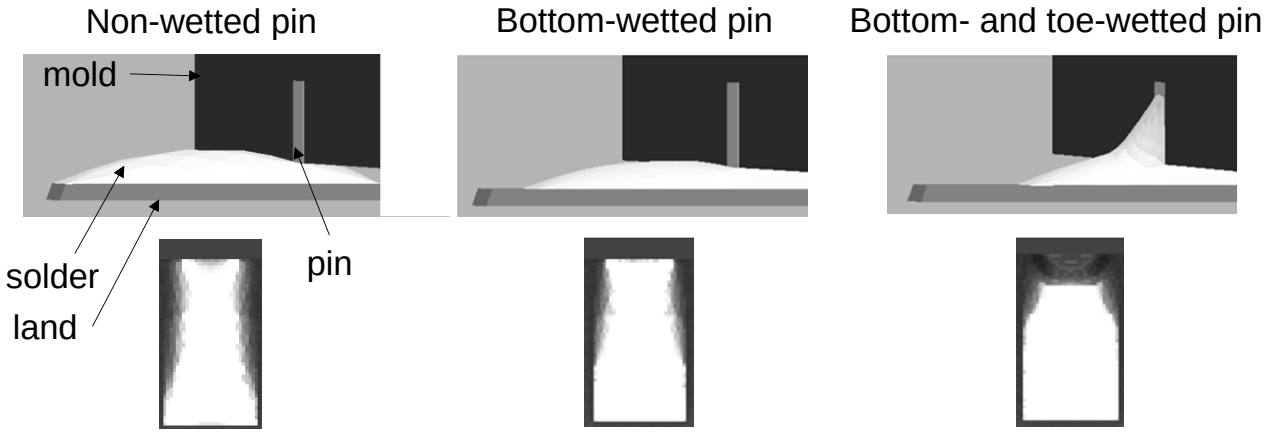

Figure 1: Perspective, side views of differently wetted LF-BTC pins (top, from left to right): Non-wetted, only bottom-wetted and bottom- and toe-wetted pins. Corresponding AOI images for a gray-scale camera (bottom, here: viewing direction opposite to surface normal of the PCB). The AOI images of non-wetted and bottom-wetted pins are indistinguishable for image analysis algorithms. The images of the solder joints and the AOI images have been obtained employing dedicated algorithms (for details, see Section 'Automatic optical solder-joint inspection (AOI)').

Automatic X-ray inspection (AXI) can be employed instead of AOI for solder-joint inspection. However, dedicated land designs are required, and high throughput X-ray inspection generally requires the presence of taboo zones for e.g. components on the opposite assembly side to avoid overlapping X-ray shadows disturbing robust pass/fail classification. Thus, the use of AXI imposes layout restrictions which partly annihilate the size advantage of LF-BTC components.

Electrical tests may be used to verify electrical connectivity, but a full electrical test of all terminations may not be possible for many applications. Moreover, electrical contact at a given temperature for which the test is conducted cannot assure that a good solder joint has developed, as a pin, even if it is not wetted, may rest on and thus have electrical contact with solder on the pin land. When temperatures changes, device and/or board warpage may result in an electrical discontinuity and therefor a failure.

An additional point to consider in addition to design for inspectability comes from a design for reliability perspective: Solder-joint robustness is increased by the presence of a robustly wettable singulation edge. The number of cycles to failure under thermal cycling is typically increased by up to about 20 %, in the presence of an outer fillet.

Package suppliers have recognized the above discussed benefits and responded by the refinement of the lead-frame design or the singulation process that enable a lead modification such that a portion of the outer pin termination remains plated after singulation. Various approaches for such pin modifications have been devised, and a few will be discussed in the following subsection.

Wettable flanks

As a mechanical singulation process, i.e. either sawing or punching, is required in the mass production of LF-BTCs, any surface of the leadframe generated by this singulation process will be composed of Cu without plating. Post-singulation plating using electrodeposition is possible, but can be employed only for certain dual-flat no-lead packages (in fact, these devices are only partially singulated at the time of plating, so that an electrical connection of all pins is possible). In general, the key to the generation of wettable flanks lies in the separation of a part of the flank from the plane of cutting or sawing. Different strategies have been devised for accomplishing this. Without excluding the possibility to use other pin modifications for the purpose of solder-joint inspection as described in this paper, the following two modifications represent commonly used examples.

(i) Step-cut leadframe (see Figure 2): The step-cut leadframe enables the encroachment of a plated portion of the pin flank. To this end, a small step feature can be established at the end on the copper terminals by application of an only partial (with respect to the sawing depth) sawing operation, following package assembly, mold and cure processes. The final process step before singulation plates the exposed copper terminals with a solderable surface finish. The plating facilitates solder wetting to take place during the reflow solder attachment process.

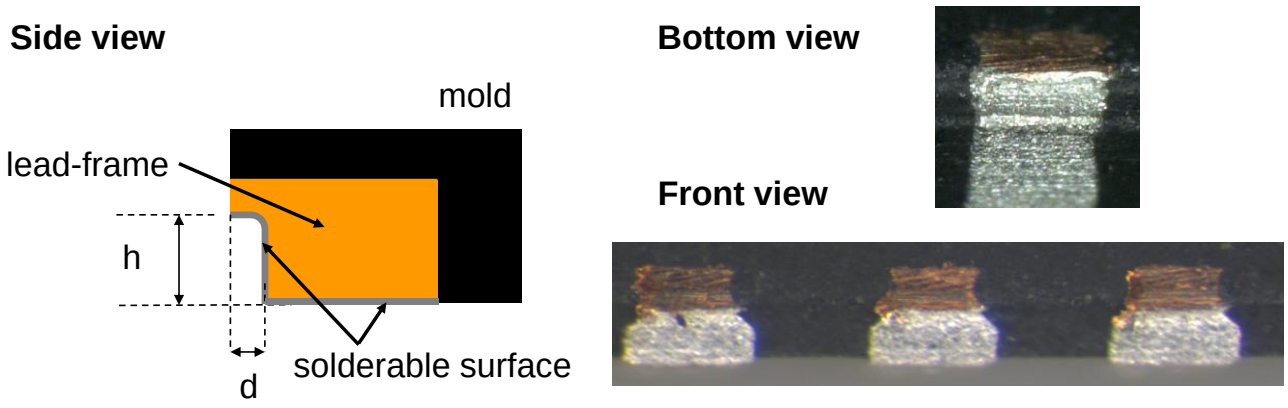

Figure 2: Schematic side view of a step-cut leadframe (left side) and optical micrographs of step-cut pin modifications viewed from the component's bottom side (right top side) and viewed from the front of the pins (right bottom side) .

(ii) Hollow-groove lead frame (see Figure 3): Following the chemical etch or stamp process of the copper leadframe array the bottom surface within the contact area is masked to enable a secondary chemical etch process to form a shallow concave depression ('dimple'), in which the plating remains intact during the final singulation operation. In this case, the singulation process can be either sawing or punching (see also [3] [4]).

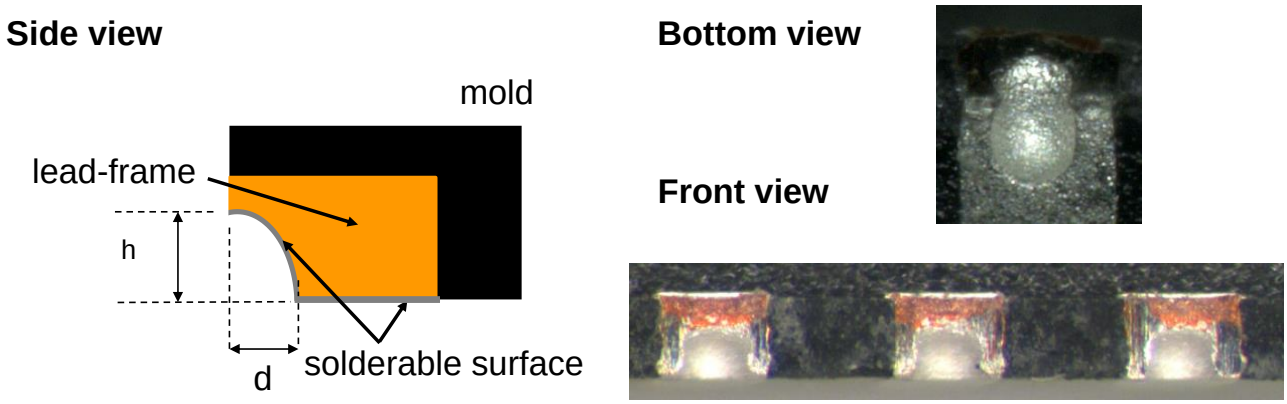

Figure 3: Schematic side view of a hollow-groove lead-frame (left side) and optical micrographs of hollow-groove pin modifications viewed from the component's bottom side (right top side) and viewed from the front of the pins (right bottom side) .

Images of solder joints with the above discussed features obtained employing scanning-electron microscopy have been gathered in Figure 4.

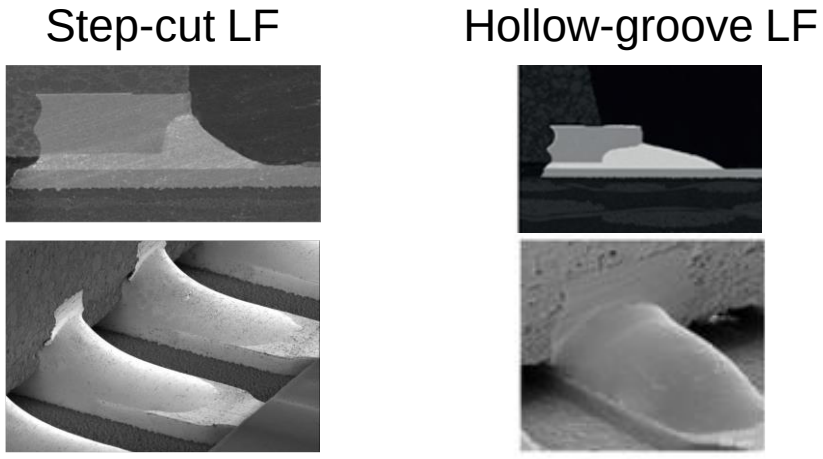

Figure 4: Scanning-microscopy images of cross-sections (top) of solder joints and of solder joints (bottom) for step-cut (left) and hollow-groove (right) lead frames (taken from [5]**).**

In order to correctly assess pin wetting based on the detection of a toe fillet, it is obvious that both the pin edge (flank) and the pin bottom must have the same type of plating deposited during one plating step. Otherwise, the detection of a toe fillet would not enable drawing the conclusion that wetting has occurred also underneath the pin.

Automatic optical solder-joint inspection (AOI)

Pass/fail classification in AOI

Automatic optical solder-joint inspection (AOI) is a standard post-soldering inspection method employed to check assemblies for potential soldering failures as bridging, shifted or skewed components etc. Different AOI systems exist in the market, but it is common to all systems that an optical gray-scale or color image of a solder joint, recorded with a camera system under one or even different conditions of illumination and/or viewed from different directions is subjected to an image analysis procedure which quantifies image features as color, gray value, gradients etc. These feature values can then be compared against certain threshold values to arrive at a pass/fail classification for a particular solder joint.

Detection of wetting failures – ideally wetted/non-wetted terminations

A key inspection step for surface-mount components is the detection of proper wetting of a components termination by solder and the following discussion will be focused on this inspection step. For LF-BTCs, ideal cases of wetted and non-wetted terminations are shown in Figure 5. The images of the solder joints correspond to actual solder-joint shapes and have been calculated from the solder volume and the known surface tension of solder by employing an algorithm which determines the solder surface contour by minimizing the total energy of the system (solder and termination). The images on the right-hand side are images of the respective solder joints as they would be detected by the camera in an AOI system. To obtain these images, a ray-tracing algorithm, which takes into consideration the camera position (here: viewing direction opposite to surface normal of PCB), the illumination (here: main light from camera direction) and the surface reflectance of the solder, has been employed. The light is reflected from the surface of the solder, which has been determined by energy minimization (see above). For such ideal cases of wetting and non-wetting, a pass/fail classification would for example be easily possible by determining an average gray value in an inspection window, as indicated in Figure 5.

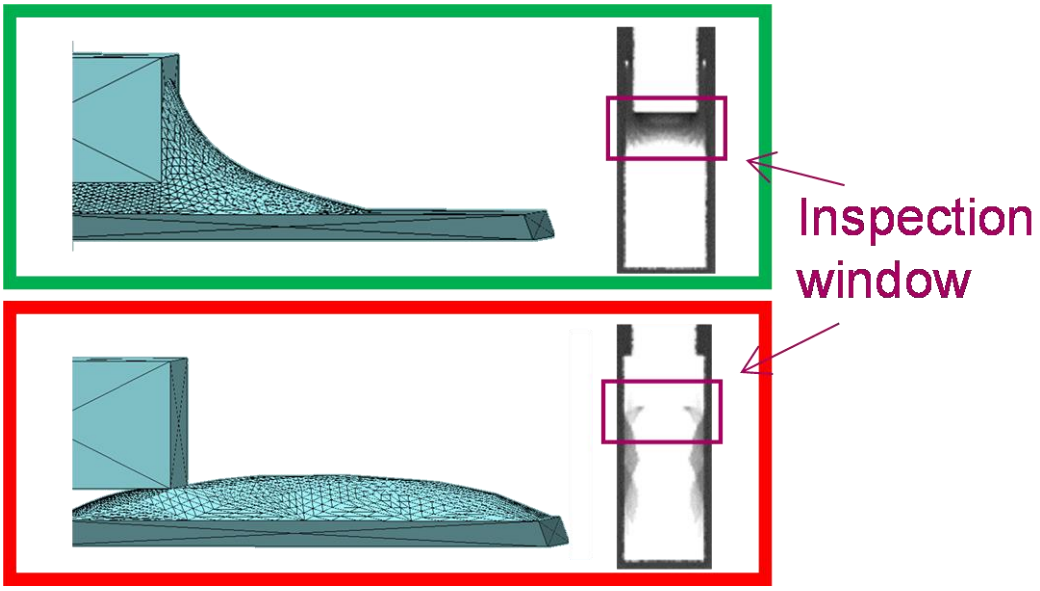

Figure 5: Perspective, side views of a wetted (top) and a non-wetted (bottom) termination of a LF-BTC. The surface of the solder has been obtained by surface-energy minimization. The insets on the right-hand side show the images as they would be obtained in a gray-scale camera in an AOI system viewing the solder joints from the top.

In mass production, such automatic inspection must result in a very low number of false calls (i.e. the inspection returns a 'fail' even though there is no defect). Any false call results either in additional scrap costs (if an assembly is dispositioned upon detection of a defect) or additional effort related to post inspection by a trained operator, to verify the AOI classification (see Figure 6). For assemblies featuring hundreds of components and thus thousands of solder joints and cycle times of only tens of seconds per assembly, the false-call rate must be less than, say, 0.1 % for AOI to constitute a robust inspection method. At the same time, the rate for escapes (i.e. the inspection returns a 'pass' even though there is a defect) must be kept as low as possible. This usually, requires a trade-off, as lower false-call rates result in increased escape rates and vice versa, if only the evaluation threshold is adjusted (see what follows).

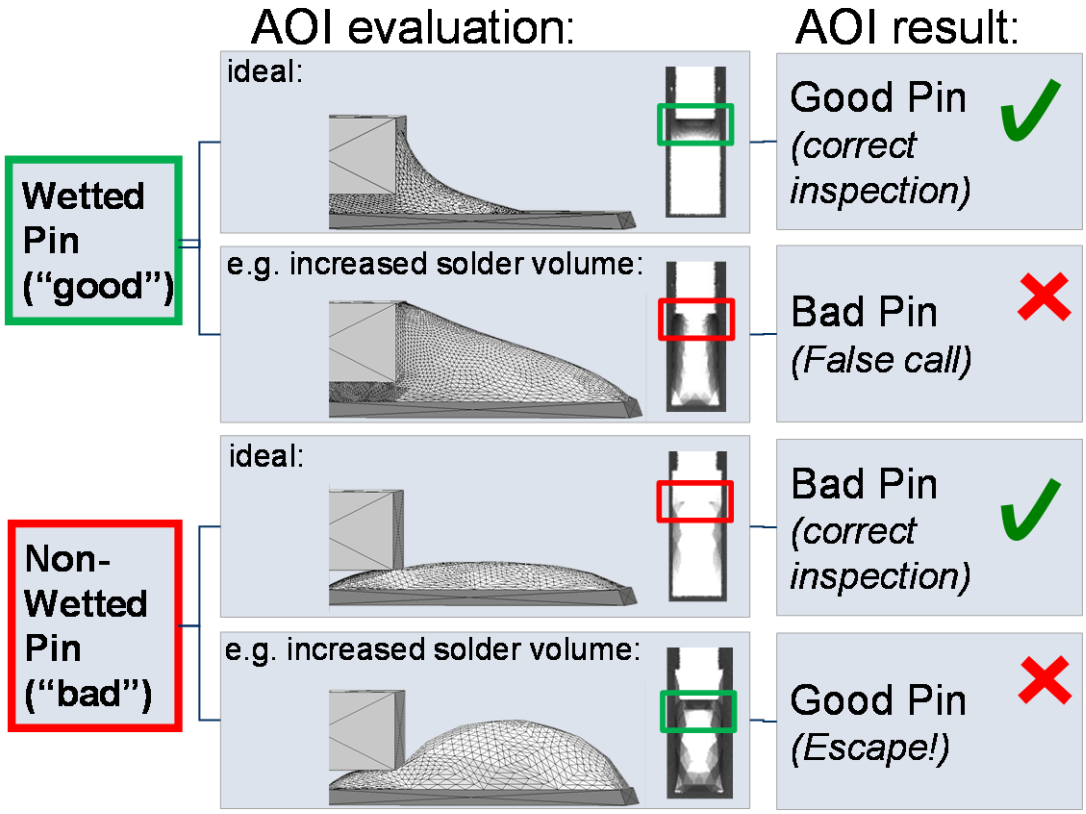

Figure 6: Perspective, side view of wetted (top two) and non-wetted (bottom two) terminations of LF-BTCs. The surface of the solder has been obtained by surface-energy minimization. The insets on the right-hand side show the images as they would be obtained in a gray-scale camera in an AOI system viewing the solder joints from the top. For cases of increased solder volume, the appearance of the solder joints in the camera images results in an erroneous pass/fail classification, i.e. a wetted pin is classified as defective (false call) and a non-wetted pin is classified as good (escape).

Obviously, for a robust automatic optical inspection 'defective' solder joints must look distinctly different from 'good' solder joints. The notion 'look distinctly different' can be rephrased more technically as follows: For a given inspection feature (e.g. a gray value), the inspection algorithm will return a certain distribution of feature values for both good and defective solder joints. These distributions result e.g. from the scatter of the components termination and the land geometries, the scatter of solder volume, instrumentation etc (cf. Figure 7). A robust inspection can only be assured if the distributions overlap only to a very limited extended, as all overlap results inevitably in false calls and escapes, the proportions of which depend on the setting of the pass/fail threshold value. In Figure 7, an increase of the threshold value would result in a decreased escape rate, but an increased false-call rate, and vice versa.

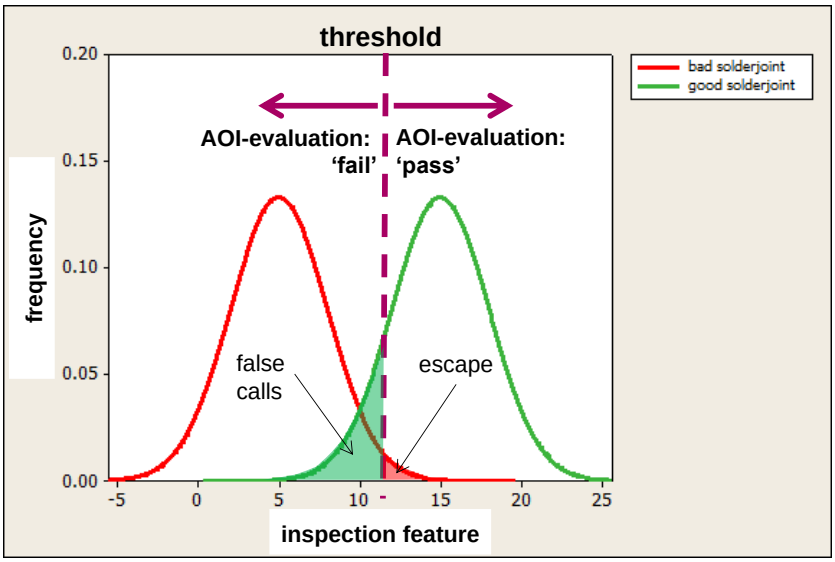

Figure 7: Pass/fail classification in solder-joint inspection. The distributions for good and defective ('bad') solder joints result from geometry, process and instrumentation scatter. The tail of the frequency distribution of good solder joints under the threshold results in false calls, whereas the tail of the frequency distribution of bad solder joints above the threshold results in escapes.

Detection of wetting failures – partly wetted terminations

For LF-BTCs, the ideal situations of an almost fully wetted flank depicted in Figure 5 (top) cannot generally obtained, as the pin modifications discussed above generally enable solder wetting up to a certain wetting height h, which is smaller than the termination height denoted in the following as H (in compliance with J-STD-001G, [2]). Obviously, in the limit $h \rightarrow 0$, a termination with proper wetting will not exhibit a toe fillet, and thus its detection with AOI will become impossible (as shown in Figure 1). This implies that there will be a value of h between 0 and H, which represents a threshold value h_t for enabling a robust AOI inspection. An experimental assessment of this value h_t would be very cumbersome, as it would require the availability of components with different heights of the wettable part of the termination. Even if such components would be available, the resulting wetting heights would be influenced by randomly occurring wetting of the bare copper area at the pin side, so that a precise control of the wetting height would become impossible.

Fortunately, an alternative approach is possible: Using the above discussed algorithm for the calculation of the surface contour of a solder joint and the ray-tracing approach for the calculation of images as they would be obtained with a camera in an AOI system, the influence of the wetting height h as well as the influence of other relevant parameters as solder volume can be easily explored without the need to refer to costly and time-consuming experimental investigations, subject to uncontrollable process variations complicating the statistical assessment. A very high degree of accuracy in matching both solder-joint geometries as well as AOI images is obtained in the simulations discussed: For a visual representation of the quality of the computational approach, see Figure 8.

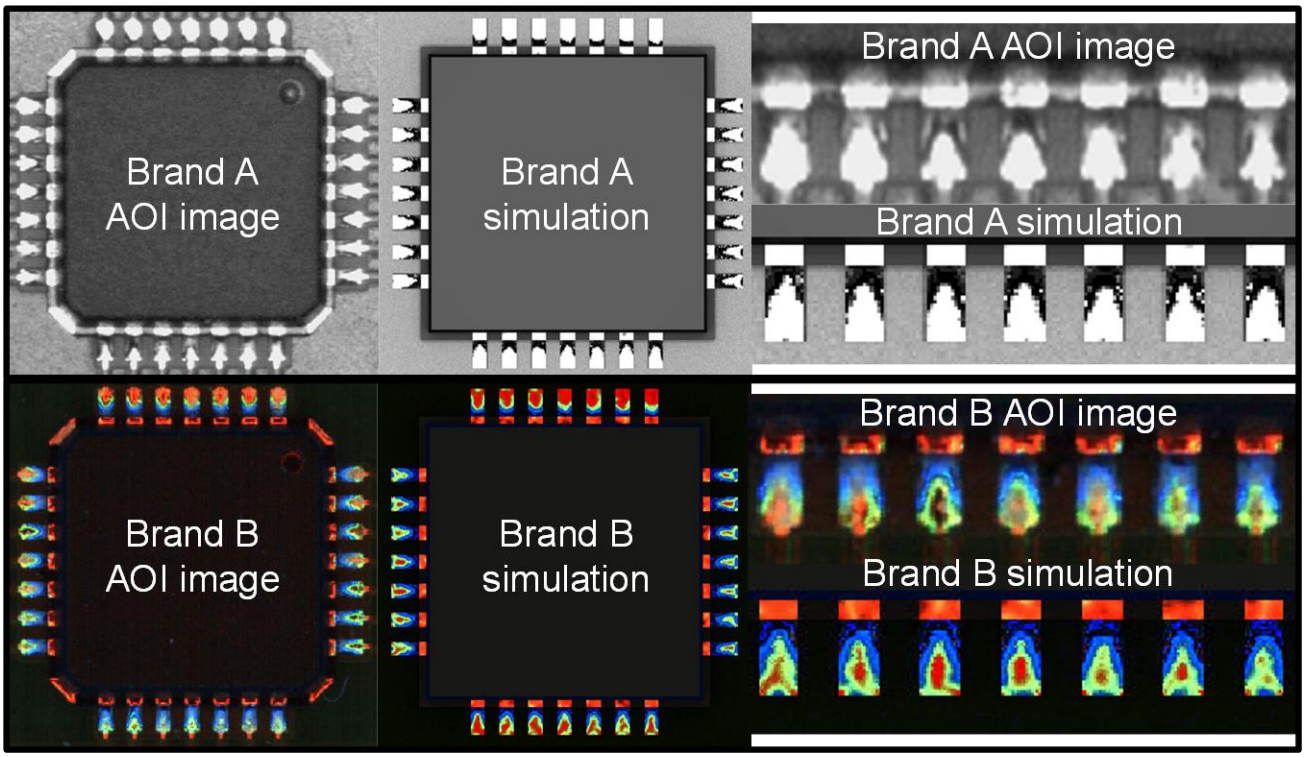

Figure 8: Comparison of actual AOI images of LF-BTCs and simulated images for two different brands of AOI systems: AOI Brand A, with monochromatic illumination and gray-scale camera; AOI Brand B, with color illumination and color camera. A very high degree of accuracy in simulating the AOI images is obtained.

Results of such a computational exploration of the effect of wetting height *h* have been gathered in Figure 9, which shows both a few exemplary images of the actual solder joints as well as the corresponding AOI images for a gray-scale camera (here: viewing direction opposite to surface normal of PCB). These calculated images (with noise added to make them as realistic as possible) can then be fed to the image-analysis software of the respective AOI system, to determine feature values. The outcome of this has been depicted in Figure 10 for two brands of AOI systems. AOI brand A uses a gray-scale camera and different monchromatic illumination modes, brand B uses a color camera and illumination with differently colored light. For each wetting height, a cloud of data points is obtained, where each data point corresponds to a certain feature value (further details cannot be revealed here in view of the proprietary nature of the detailed algorithm settings) obtained from the image-analysis algorithm. The scatter results from repeated image analyses for solder joint geometries representing the actual process scatter which would occur in the inspection of assemblies due to variations in solder volume, geometry etc. (but note that the wetting height has been kept fixed for each 'cloud' of data points). Now a threshold feature value for a pass/fail classification has to be set such that a sufficiently low escape rate is achieved. For such a threshold value it is immediately obvious that a wetting height of 100 µm would already result in a very large fraction (exceeding 75 %) of false-calls, i.e. the actual wetting height of components in real assemblies must be well above 100 µm. In fact, this and similar analyses suggest that wetting heights below 100 µm should be excluded even considering tolerances, i.e. 100 µm should represent the absolute minimum wetting height. The fact that very similar results are obtained for two AOI systems from different brands underlines the general validity of this assessment of the minimum wetting height: Below a wetting height *h* of 100 µm, good and defective solder joints become undistinguishable irrespective of the particular illumination and image detection strategy adopted in different brands of AOI systems.

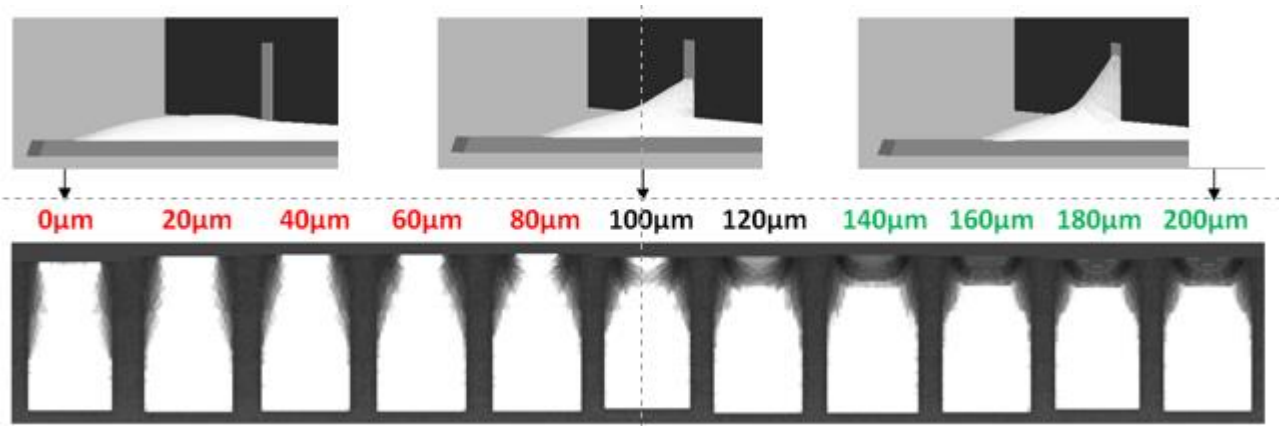

Figure 9: Exemplary images of the actual solder joints for different wetting heights (0 µm, 100 µm and 200 µm, top, from left to right) well as the corresponding AOI images for a gray-scale camera (bottom, here: viewing direction opposite to surface normal of PCB).

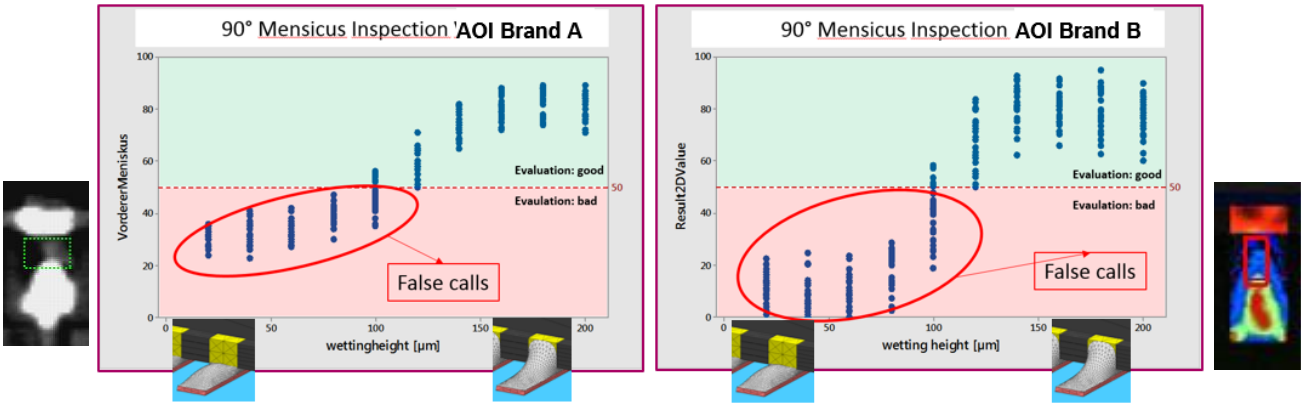

Figure 10: Feature values obtained from image-analysis algorithms applied to solder joints with different wetting heights. Left: AOI Brand A, with monochromatic illumination and gray-scale camera. Right: AOI Brand B, with color illumination and color camera. The scatter results from repeated image analyses for solder joint geometries representing the actual process scatter which would occur in the inspection of assemblies due to variations in solder volume, geometry etc.

The first parts in mass production confirm the accuracy of the computational assessments: A low false-call rate (< 400 ppm) without escapes has already been confirmed for a part, for which an AOI ramp-up has been backed-up by 100 % X-ray inspection to confirm the AOI assessment.

Conclusion

The influence of the wetting height of lead-frame based bottom-termination components (LF-BTCs) with wettable flanks on the performance of automatic optical solder joint inspection (AOI) has been investigated. Stable wetting up to a certain height can be achieved by using certain pin modification, as step-cut or hollow-groove type modifications, which enable parts of the pin edges to remain plated after singulation. Whereas an experimental assessment of the effect of wetting height on AOI performance would be cumbersome, if not impossible, a simulation-based approach enables a thorough and efficient tool to assess the AOI performance. Various analyses involving also AOI systems from different brands, which make use of different detection principles and image analysis algorithms, demonstrate that wettable flanks must have a minimum wetting height of 100 µm in order to enable robust AOI in the mass production of high-reliability electronic assemblies, where low escape rates and low false-call rates are both required.

References

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[2] J-STD001F, Requirements for Soldered Electrical and Electronic Assemblies, IPC, 2014.

[3] H. J. Fogelson, L. E. Bancod, S. Ahmer, T. Davis, P. A. Palasi und W. M. Anderson, „Lead Frame with Plated End Leads“. US Patent 6,608,366, 19 August 2003.

[4] H. J. Fogelson, L. E. Bancod, A. Syed, T. Davis, P. A. Palasi und W. M. Anderson, „Lead Frame with Plated End Leads“. US Patent 7,183,630, 27 February 2007.

[5] NXP, „Application Note 1902 Rev 7.0,“ 2014.