VISION
公司愿景

Become First Ranking OSAT

建成全球数一数二的半导体封测企业

MISSION
公司使命

Provide Customer Satisfied OSAT Service with Best Value, and Maximize Payback to Employee, Shareholder and Society

提供客户满意的半导体封测服务，
为客户创造最大价值，回馈员工、股东和社会

JCET

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Tel: 0086-510-86854189
Fax: 0086-510-86854550
E-mail: cdkj@cj-elec.com
http://www.jcetglobal.com

2018.2

JCET

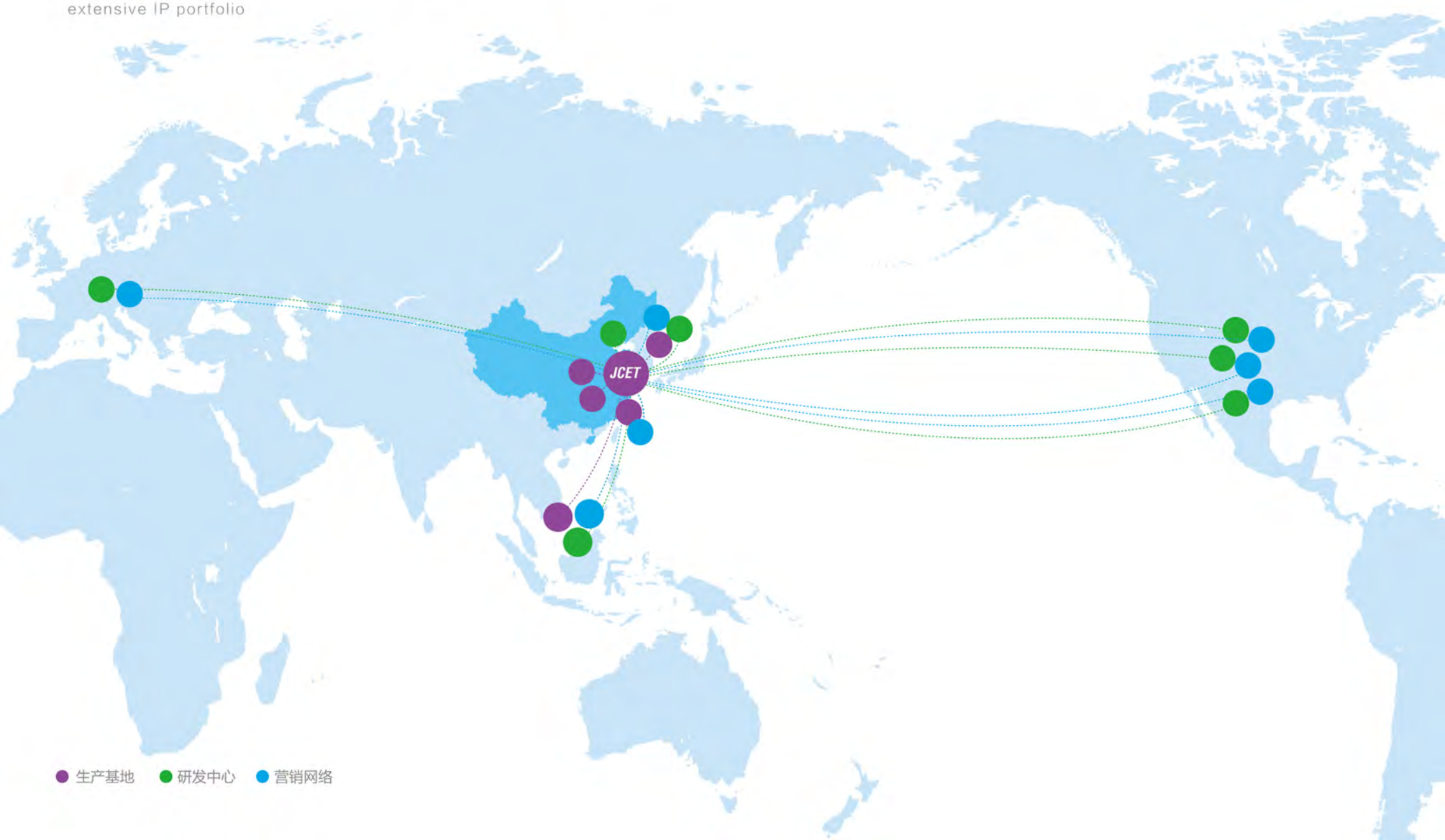
WORLD-CLASS SEMICONDUCTOR PACKAGING ASSEMBLY AND TEST COMPANY

世界级半导体封装测试企业

OUR 我们的企业
COMPANY

- Largest OSAT in China and the 3rd largest OSAT worldwide
- Worldwide locations with six sites in Jiangyin, Chuzhou, Suqian, Singapore and Korea; and two major R&D centers in Singapore and mainland China
- A global leader in semiconductor packaging & test technologies with extensive IP portfolio

- 中国大陆排名第一、全球第三
- 在江阴、滁州、宿迁、新加坡以及韩国拥有6处生产基地
- 主要研发中心在新加坡和中国大陆
- 封测技术及专利位列全球领导地位



JCET 发展历程
MILESTONES

1972

Jiangyin Transistor factory
江阴晶体管厂成立

1986

Discrete production
分立器件
自动化生产线

1989

IC production
集成电路
自动化生产线

1990

The workers' Congress in his inaugural speech
就职演说

1994

JV with Phillips
与飞利浦合作
创办合资公司

2000

Restructured to
公司改制
长电科技

2003

JCET IPO on Shanghai Stock Exchange
上海交易所上市

2003

jcap
长电先进
成立

2005
JCAP offered WLCSP
JCAP提供晶圆级
芯片尺寸封装
技术服务

2007

D3 (IC) (SiP)
长电科技集成电路厂
和Sip厂成立

2009

Chairman of NAAT
国家集成电路封
测产业技术创新
联盟理事长单位

2010

MIS
MIS封装材
料厂投产

2011

D8 Suqian
长电科技（宿迁）
公司成立

2012

D9 Chuzhou
长电科技（滁州）
公司成立

2014

JV with SMIC
与中芯国际
合资成立公司

2015

JCET acquired STATS ChipPAC
长电科技收购
STATS ChipPAC

2016

The 3rd largest OSAT worldwide in 2016
跻身全球前三大
封测企业

2017

JCET Shanghai
长电科技
上海分公司成立

2000
STATS IPO on Singapore & US stock exchanges
STATS在新加坡和
美国证券交易所上市

1994
ST Assembly Test Services
STATS
建立封装测试服务

2004
STATS merges with ChipPAC
STATS 与ChipPAC 合并

2007

R&D Center established in Singapore
新加坡
研发中心成立

2009
Expansion of China operation
中国工厂扩产

2010

300-330mm eWLB mfg in Singapore
300-330mm
eWLB技术
在新加坡厂应用

2013

Expansion of Singapore factory
新加坡工厂扩展

2014

New Korea factory
韩国新厂投产

2017

SCC relocated to Jiangyin
星科金朋上海厂
搬迁至江阴

OUR BUSINESS 我们提供的服务

Outsourced Semiconductor Assembly and Test Services(OSAT)

Full turnkey packaging and test solutions

提供一站式半导体封装测试服务

Wafers from foundry

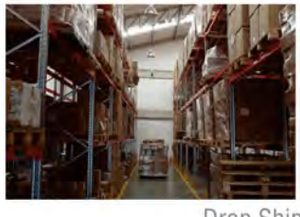
Bump

RDL/TSV/IPD

Probe

Assembly

Final Test



Drop Ship

GLOBAL 全球制造基地
MANUFACTURING BASE

滨江厂区
地　　址： 滨江中路
占地面积： 62,321平方米
建筑面积： 58,300平方米
主要产品： 凸块、晶圆级封装及测试

JCET D1 JCAP-1
Address: Binjiang Road
Floor Area: 62,321 sqm
GFA: 58,300 sqm
Main Products: Bumping, wafer level pkg & test

滁州厂区
地　　址： 世纪大道
占地面积： 169,263平方米
建筑面积： 85,000平方米
主要产品： 小功率器件引线框封装、分立器件及测试

JCET D9
Address: Century Avenue
Floor Area: 169,263 sqm
GFA: 85,000 sqm
Main Products: Leaded, discrete package and test

城东厂区
（包含长电集成电路事业中心、长电先进、新顺、星科金朋江阴、中芯长电）
地　　址： 长山路
占地面积： 374,882平方米
建筑面积： 372,500平方米
主要产品： 晶圆级封装、凸块、倒装及测试、引线框封装、基板封装、SiP

JCET D3, JCAP-2, xinshun, JSCC, SJsemi
Address: Changshan Road
Floor Area: 374,882 sqm
GFA: 372,500 sqm
Main Products: WLCSP, bumping, flip chip, Leaded, laminate, SiP, test and MIS

韩国仁川厂区
地　　址： 191 Jayumuyeok-ro Jung-gu, Incheon
占地面积： 110,117平方米
建筑面积： 110,200平方米
主要产品： SiP，芯片堆叠PoP、倒装及测试

SCK, JSCK
Address: 191 Jayumuyeok-ro Jung-gu, Incheon
Floor Area: 110,117 sqm
GFA: 110,200 sqm
Main Products: Sip, Flip chip, BGA, CSP, stacked die, probe, assembly and final test

宿迁厂区
地　　址： 紫金山路
占地面积： 84,122平方米
建筑面积： 53,700平方米
主要产品： 大功率器件引线框封装测试

JCET D8
Address: Purple Mountain Road
Floor Area: 84,122 sqm
GFA: 53,700 sqm
Main Products: Power package and test

新加坡厂区
地　　址： 5 Yishun Street
占地面积： 29,894平方米
建筑面积： 73,600平方米
主要产品： 晶圆级封装、eWLB、测试

SCS
Address: 5 Yishun Street
Floor Area: 29,894 sqm
GFA: 73,600 sqm
Main Products: Advanced wafer level packaging, laminate, QFN & test

晶圆级封装

WAFER LEVEL PACKAGE

Fan-in (FIWLP)

- WLSCP
- (Bumping, Repassivation, RDL)
- eWLCSP
- (encapsulated WLCSP)

Fan-out (FOWLP)

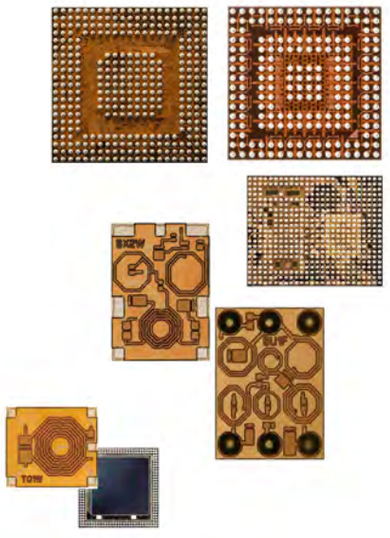
- eWLB
- (embedded wafer level BGA)
- 2.5D and 3D SiP eWLB

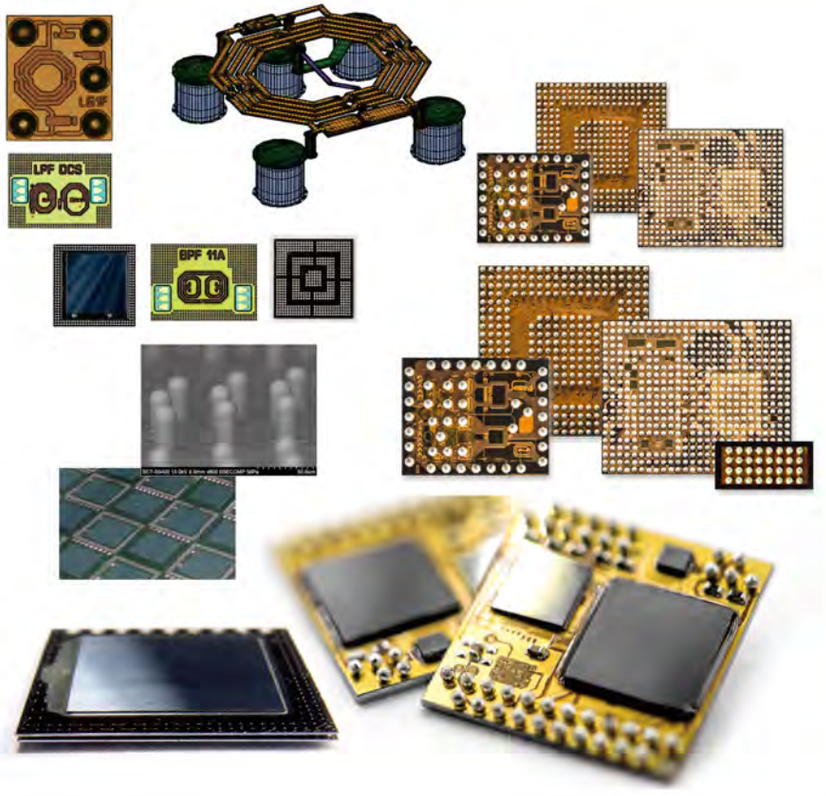
Integrated Passive Devices

- IPD

Through Silicon Via

- TSV for CIS
- TSV for 3D IC





Highlights

- Compact, high performance packages for rapidly shrinking product form factors
- Proven leadership in innovative FOWLP solutions with over 1.7 Billion units shipped
- Innovative 2D/2.5D/3D FOWLP packages with size, performance and cost advantages
- Enhanced performance and size reduction with silicon IPDs
- 3D TSV capabilities covering mid-end-of-line through backend assembly and test

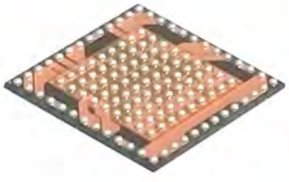
技术优势

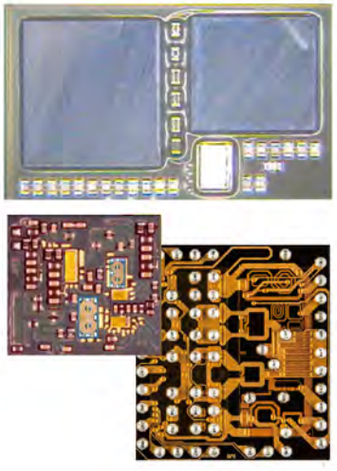
- 中国晶圆级封装技术及FOWLP技术的领导者
- WLCSP产品出货量已超过360亿颗
- FOWLP产品出货量已超过17亿颗
- 在晶圆上集成的无源IPD器件，更轻薄短小且性能更优异
- 作为TSV技术的先驱者，具备完整的3D TSV封装技术开发与量产能力

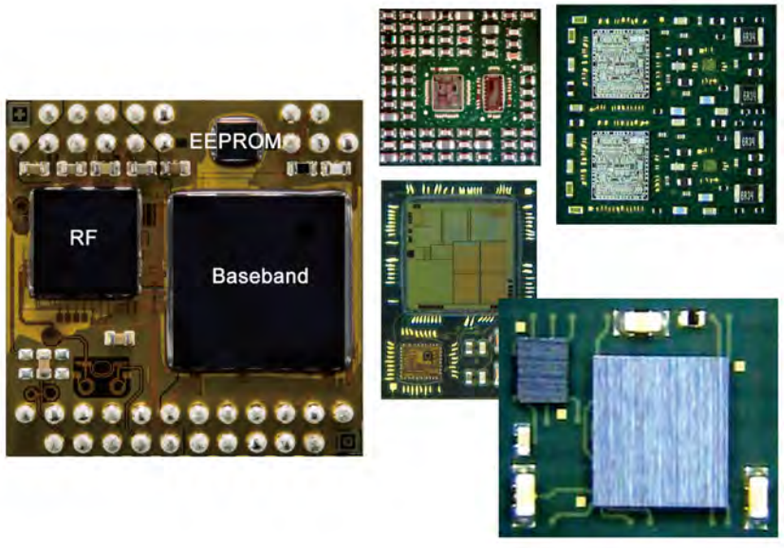
系统级封装

SYSTEM IN PACKAGE

FOWLP SiP
Laminate FC SiP
Laminate FC + WB SiP
SiP Modules
Leadframe WB SiP
Laminate Stack Die WB SiP







Highlights

- Electronic system or sub-system integrates multiple active and passive components for higher performance, functionality, processing speeds and low cost
- Leading SiP technology portfolio incorporates all the key technical building blocks
  - -- Advanced design rules for 2.5D and 3D FOWLP or SiP configurations
  - -- High density SMT with high accuracy component placement
  - -- Advanced mold tech for complex topography SiP applications
  - -- Highly automated process modules
  - -- Tight process control to ensure consistency and high yield
- One stop turnkey solution - wafer to fully tested SiP modules

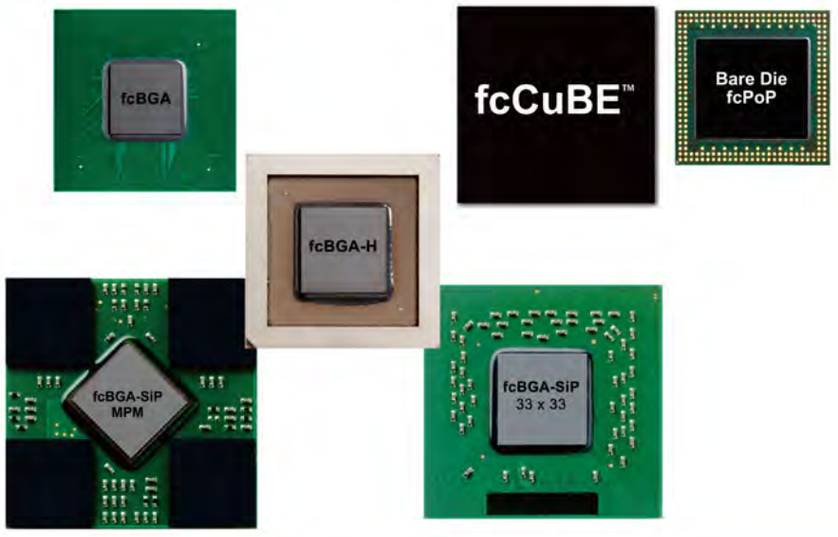
技术优势

- 射频模组封装测试出货量位居全球前三
- 具备超薄被动元件及多颗异质芯片的高精度表面贴装
- 针对复杂高密度贴装表面的先进塑封技术
- 包含溅射EMI电磁屏蔽层在内的自动化制程等全工艺生产能力
- 提供从晶圆到系统模组的一站式封装测试服务

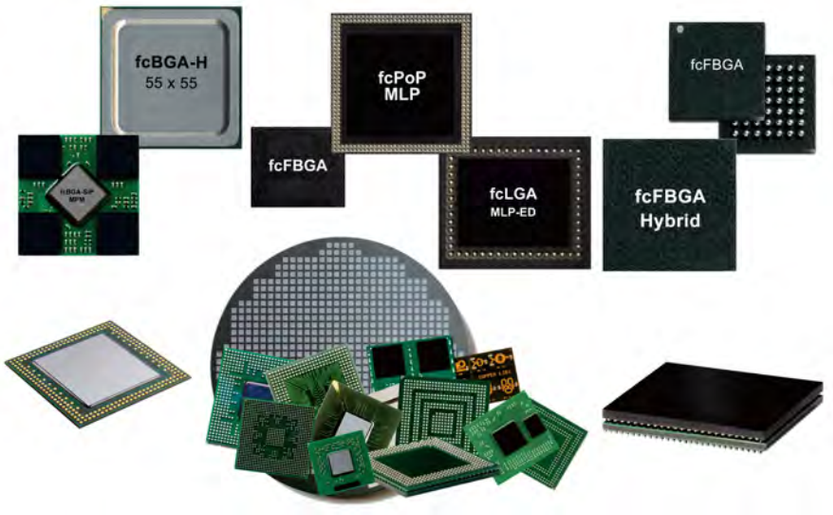
倒装芯片基板封装

FLIP CHIP PACKAGE

fcCuBE
fcFBGA(fcCSP)
fcBGA(FCBGA)
Bare die fcPoP
- (flip chip package-on-package)



Molded Laser fcPoP
- (flip chip package-on-package)
flip chip on Leadframe
- (FCOL)
fcMIS
- (flip chip on Molded interconnect System)



Highlights

- Patented fcCuBE : proven low cost, high performance advanced flip chip technology
  --Fine pitch Cu pillar and Bond-on-Lead (BOL) interconnection for higher routing density at a lower cost
  --Scalability to finer bump pitches, higher I/O and advanced fab nodes at a lower cost
- High speed fcBGA-H offering for network/communication market
- fcPoP and hybrid flip chip + wirebond configurations for increased functional integration in a smaller
- form factor, and Pre-stacking of memory on logic for PoP packages
- Leadership in low cost substrate technologies – Embedded Trace Substrate (ETS), Molded
- Interconnect System (MIS) and Single Layer laminate substrate

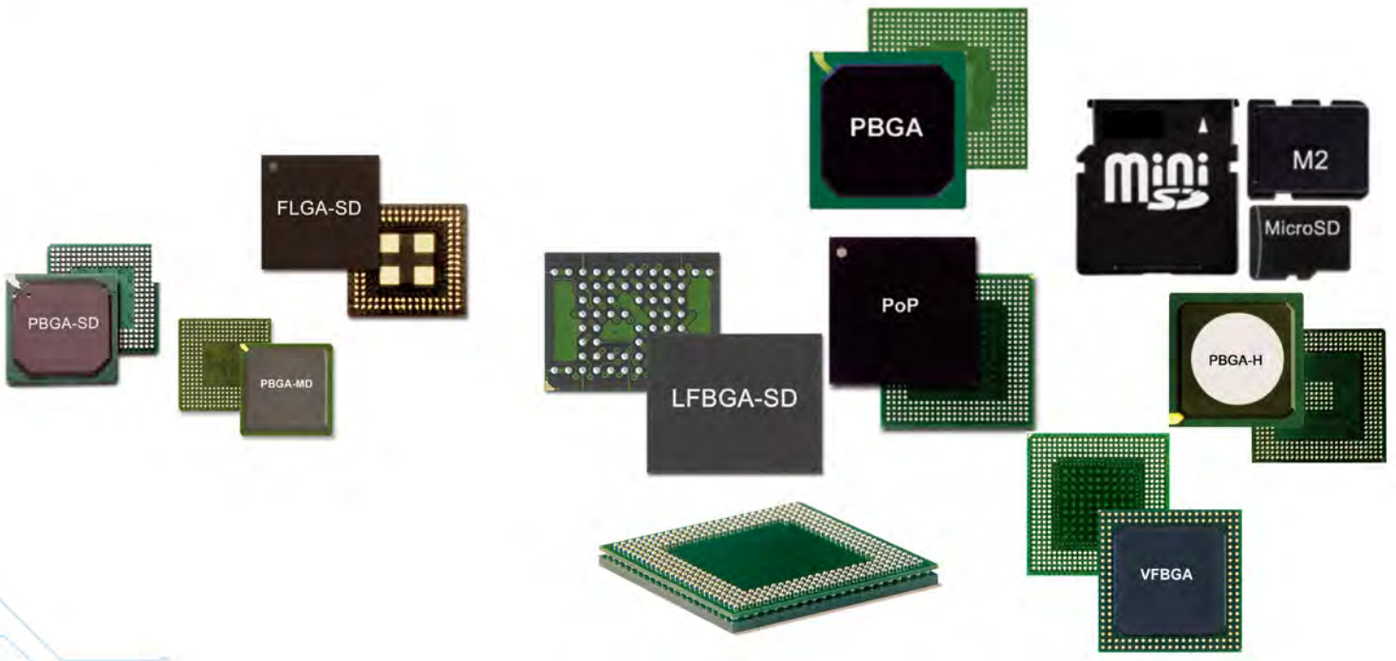
技术优势

- fcCuBE作为独特的倒装芯片封装专利技术，在提升性能的同时，有效地降低封装成本
- 针对高速网络、高性能计算和消费类芯片市场，我们提供完整的fcBGA封装解决方案
- 先进PoP封装技术可有效缩短内存芯片和逻辑芯片之间的互联，提高运算速度并降低功耗
- 基于引线框或MIS和铜凸块的FCOL专利倒装封装技术提供优异的导热导电性能

引线基板封装

WIRE BOND PACKAGE

- ▶ PBGA
- ▶ FBGA(Side by Side, Stacked Die)
- ▶ Package-on-Package(PoP)
- ▶ MEMS
- ▶ Memmory Card
- ▶ LGA



Highlights

- Advanced wirebond technology in a cost competitive manufacturing location
- Comprehensive range of single die, multi die, thermally enhanced and stacked die packages
- Thin outline LGA suitable for high performance and/or portable applications
- Low profile PoP provides flexibility in mixing and matching IC technologies in a thin package
- Innovative process capabilities to enable MEMS and sensors chipset integration and fusion
- Cost effective package approach for memory card formats

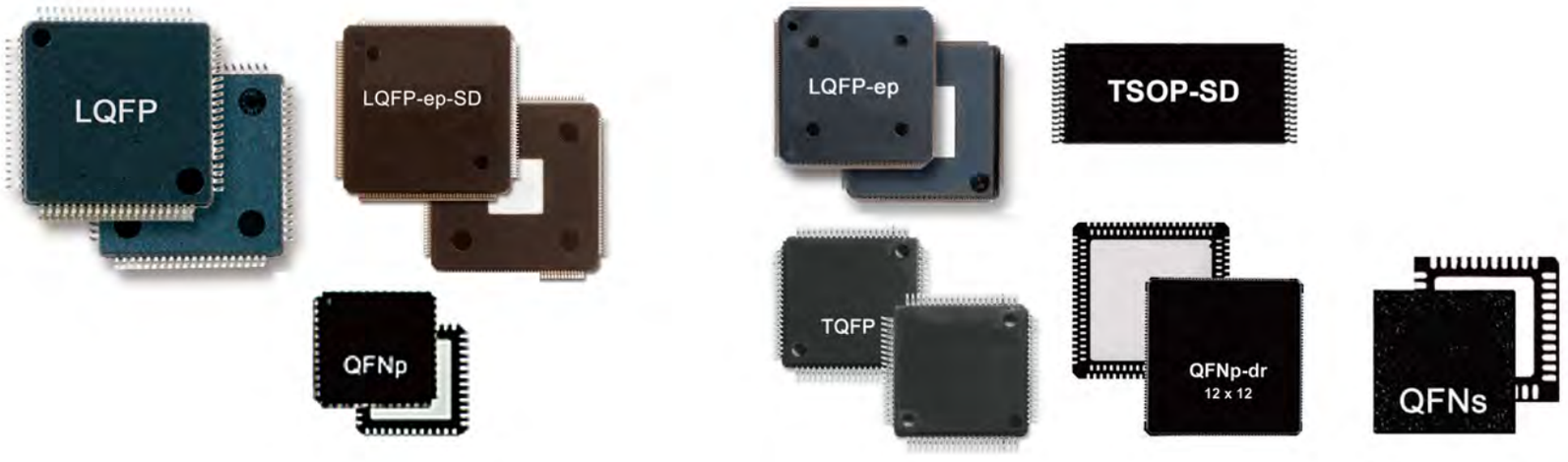
技术优势

- 具备量产各种超薄封装体的焊线类封装技术能力
- 提供包括PBGA在内的全系列BGA封装测试服务。其中PBGA-H技术通过集成单个散热片或在热压塑封制程中贴装整张金属片，使得封装体散热能力显著提升
- 通过采用开创性的芯片侧装技术，扩展了MEMS产品的应用

引线框架封装

LEAD FRAME

Discrete Packages:TO,SOD,FBP	DFN
Flip Chip on Leadframe(FCOL)	QFP
DIP	QFN-mr
SOP	QFN-dr
SOT	QFN



Highlights

- Extensive experience in leadframe and discrete packages for a wide range of applications
- Patented FCOL on MIS lead frame offers leading-edge QFN package for proven better electrical and thermal performance, particularly in power management applications

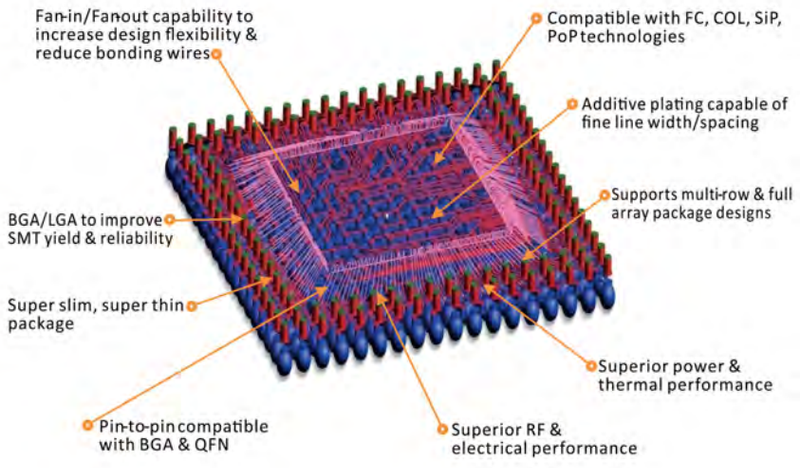
技术优势

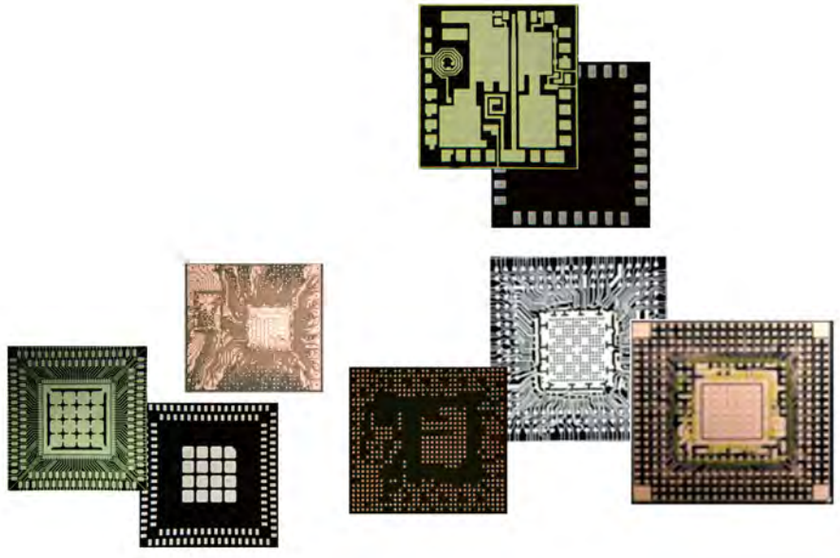
- 种类齐全各种应用的QFN封装
- QFNs-st技术可提供多排引脚以实现更多的I/O互联
- 引线框倒装技术提供最佳综合性能

高性能MIS专利封装技术

MOLDED INTERCONNECT SYSTEM (MIS)

Patented molded interconnection technology that achieves higher density and performance for a wide range of packages with superior reliability





MIS advantages

- Ultra small, thin technology achieves product miniaturization
- Superior RF, electrical, thermal and reliability performance
- Fine line routing for high density I/O
- Supports a wide range of wirebond, flip chip, SiP and PoP package configurations
- Proven substrate technology with over 1B units shipped since 2010

MIS的优点

- 超小、超薄的加工工艺使得产品更加微型化
- 优异的射频、导电性、导热性及可靠性
- 通过精细布线，实现更高的I/O引脚数
- 可应用于倒装、系统级封装等各种封装形式
- 自2010年以来，基于MIS基板技术的封装产品出货量已超过10亿颗

全面系统的测试服务

INTEGRATED TEST SOLUTIONS

As one of the largest test outsourcing providers, we offer a full suite of test platforms and engineering services to support a broad range of mixed signal, RF, analog and high-performance digital semiconductor devices for the communications, digital consumer and computing markets. we combine operational efficiencies with proven test capabilities to achieve the lowest cost of test with the highest possible throughput and faster time-to-market.

我们提供全套的测试平台和技术服务，支持通讯类、消费类及电脑类的半导体芯片，主要包括混合信号、射频、逻辑及高性能数字芯片等。我们充分结合制造效率和测试能力，以最低测试成本提供最高产能，使产品可以更快投入市场。

Full Turkey Services from Bump, Wafer Probe, Assembly, Final Test,Post Test To Drop Shipment

Test Engineering Services

- Test program development, debug, optimization and validation
- Device characterization
- First silicon characterization (Wafer Probe)
- Load board design, fabrication and qualification (Final Test)
- Prototype evaluation
- Multi-site migration to higher parallel testing
- Test program conversion to new tester platform