The powerful combination of flying probe test and JTAG test speeds up testing

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The lack of physical access at board level makes a mixed test approach, based on combining flying probe testing with boundary scan techniques, attractive -- provided that test development and optimization are carried out early in the design cycle via a testability analysis. The factory of Alcatel CIT at Eu applied this method to its boards with great success.

The circuit board test situation looks like it is headed for disaster: on one side you have complex electronic boards that are becoming increasingly dense, on the other side quality requirements for production tests that are becoming more and more stringent. So the evolution of technologies poses a new challenge: design testable boards in spite of a drastic reduction in the number of physical accesses. The level of integration is rapidly increasing – miniaturization of the component package (surface mounted technologies, BGA) as well as higher density of circuit board interconnects (including buried via, micro via, MOV technology). The size of a traditional test point is now that of a passive component! The consequence: we've run out of space for all the test points. The surviving test points will have to be smaller and have to be where we need them.

Still today, the technique primarily used in production is in-circuit test which requires a physical access for each net. However, its traditional interface (bed of nails), with the associated cost penalty induced by small probes ensuring contact with 50 mil test points, as well as the generation time of a test program highlight the advantages of the flying probe tester. Flying probe testing allows a first level of test after quick program development (just a few days) and does not require a bed of nails. Obviously, there is a flip side to this coin: the probes have to move to carry out each test step, so testing a board with 2000 nets can take more than 45 minutes.

A powerful union: the best of both approaches

Unfortunately, there is no miracle solution. Each test technique has its advantages and its disadvantages. From this challenge, a simple idea was born: why not combine several techniques to benefit from the best of each? The Alcatel factory located at Eu (Seine-Maritime – France) sought to combine the attractions of the flying probe test and the boundary scan test (or JTAG). To obtain the best possible results in having the flying probe test run faster, Alcatel CIT teamed up with ASTER, creator of TestWay™ testability analysis software (available from Acugen software in the USA).

Boundary scan is a low cost test approach which requires digital components compatible with the IEEE-1149.1 standard. An electrical testability analysis, at the schematic capture level, extends the possibilities of this kind of test to components without boundary scan functionality (such as EEPROM, RAM, buffer, PLD, glue logic). This boundary scan test is carried out under power and does not require a physical access except from the test bus (4

or 5 wires). A strong point of this particular testability analyzer is that the development of the JTAG test programs can start right after schematic capture without waiting for layout. It is thus possible to have the JTAG tests for the prototype phases; they could then be re-used during the production test, even for maintenance.

The flying probe test uses the measurement techniques of the in-circuit systems, or rather MDA (manufacturing defect analyzer), since it is generally carried out not under power. Its advantages? The flying probes are able to reach very small test areas and, unlike the in-circuit test, do not need a bed of nails. The manufacturing time for a bed of nails (approximately 2 weeks) is no longer an incompressible limitation. The flying probe test is of obvious interest for prototypes tests. On the other hand, the low speed of this technique makes it unsuitable for production test.

Combining these two approaches meets a double objective: to supplement the flying probe test in the areas where there are no physical access; and to reduce its duration since now it need not be executed any more on the entire board.

Testability analysis, the key to optimal test results

TestWay software carries out an electrical testability analysis at schematic capture. This analysis takes several forms: design and testability rules checking before layout, boundary scan analysis, number of test points optimization, test strategies combination, back-annotation in layout or CIM tools (such as Trilogy5000 or FabMaster). In this context, the generation processes of the boundary scan test and flying probe test are combined to maximum advantage (figures 1 and 2).

Generation of the Boundary-Scan data from the schematic capture

Figure 1

The boundary-scan configuration provided by TestWay gathers the complete set of data useful to startup the boundary scan ATPG: netlist, identification of the boundary-scan chains, component models.
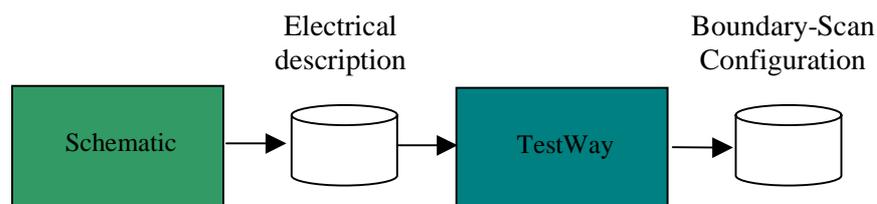
Generation of a program for flying probe tester using the layout data.

Figure 2

Physical *description, available in a CIM software like FabMaster, is enough to create a test program for a flying probes tester.*
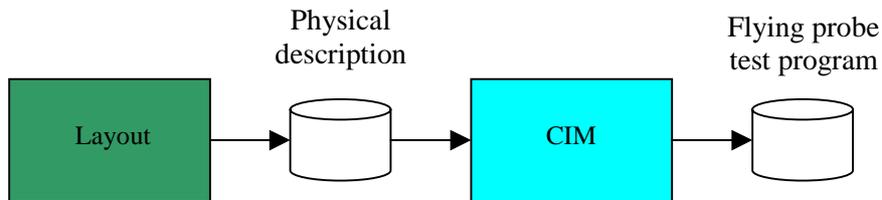
To start the process of optimizing the flying probe test, the TestWay software produces a testability analysis and predicts the fault coverage based on the testability analysis and/or uses the list of the actually detected faults if the boundary scan test program is already available. Next, TestWay is run again to analyze the test program for the flying probes step by step in order to remove redundant test steps (figure 3).

Combination of the test strategies

Figure 3

TestWay analyzes the program of the flying probe tester and allows the elimination of the redundant stages of test with a later boundary-scan test (those are placed in comments).
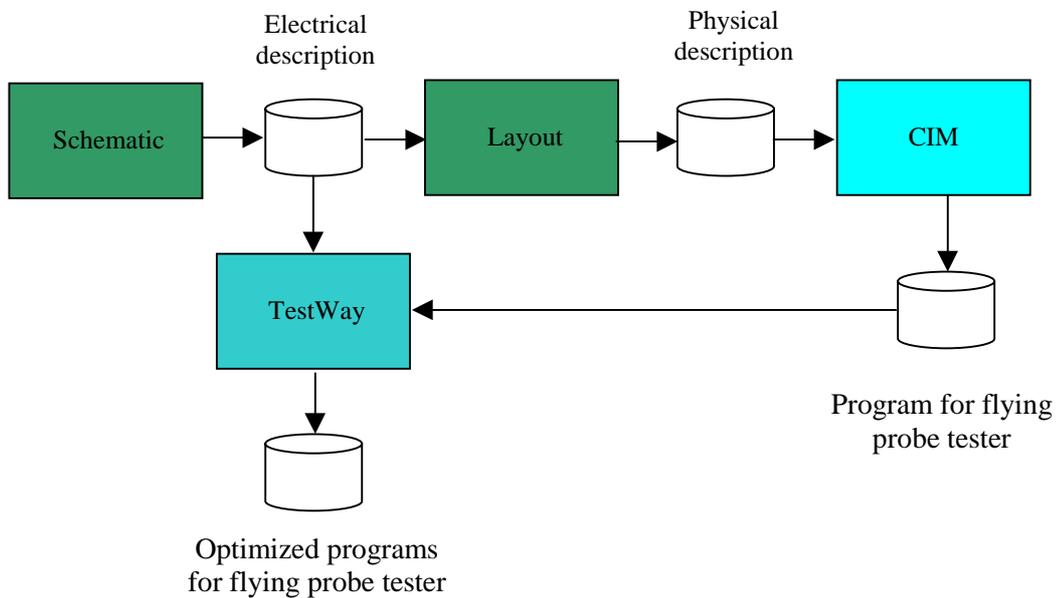
The TestWay testability analyzer generates two optimized programs for the flying probe tester: both have the same ability to detect a defect in combination with a boundary scan test. The difference between the two lies in the diagnostic resolution. The program version called Optimist considers that the JTAG tester will certainly be

able to diagnose the short-circuits between a boundary scan net and a net without boundary scan. The version called Pessimist, on the other hand, preserves all the tests concerned with the flying probe tester in case of doubt about this diagnosis ability.

Tables I and II show the results of this two-pronged approach on two Alcatel CIT boards. They reveal consequent economies on the flying probe tests, regardless which TestWay version is employed; and yet, in both cases, the proportion of JTAG-compatible components is low. Thus, with only 1 % of integrated circuits in conformity with the IEEE-1149.1 standard, TestWay saved between 39 and 67 % of the flying probe test's on the flying probe test system!

I - Results of the two-pronged approach on a board with 2 000 nets equipped with 0,4 % of JTAG components	
Board A	1700 components including 7 JTAG components, 2000 nets.
Package	1 BGA with the step of 50 mil, many QFP with the step of 20 mil
Layout	8 layers
Complete Takaya test	8950 test steps
Version "Optimist"	42% of economy, remain 5100 test steps
Version "Pessimist"	22% of economy, remain 7000 test steps
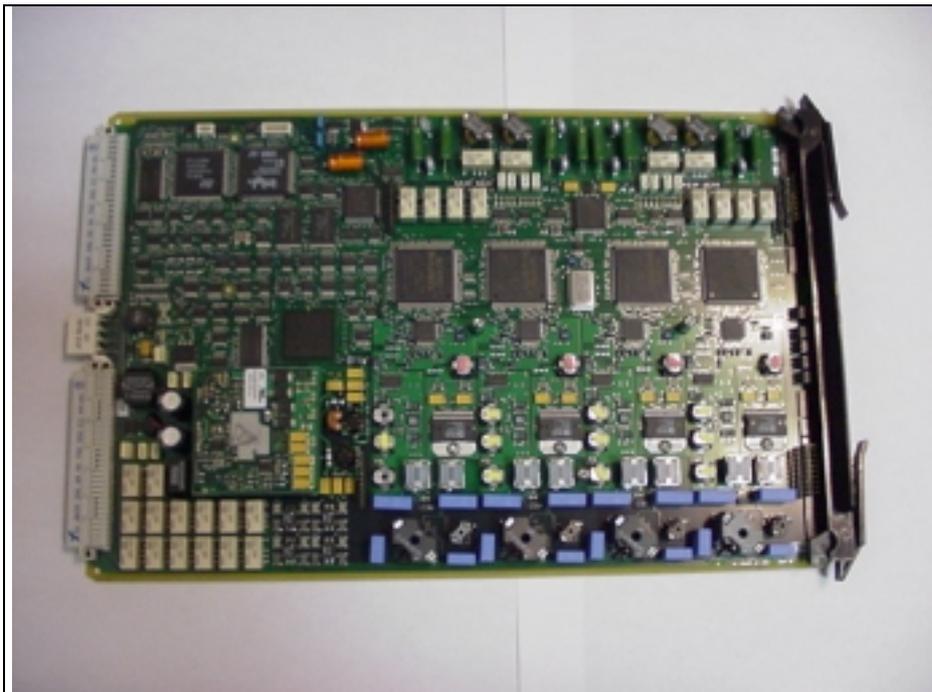
On this board with 8 layers (board A of table I), there are 1700 components, of which several QFP with the step of 20 mil. In spite of the small proportion of JTAG components (0,4%), the time saving carried out on the flying probe test exceeds 20% with the optimized program in its Pessimistic version.

II - Results of the two-pronged on a board with 3 500 nets equipped with 1 % of JTAG components	
Board B	1900 components including 20 JTAG components, 3500 nets.
Package	1 BGA with the step of 50 mil, 14 BGA with the step of 40 mil, 5 micro-BGA with the step of 30 mil, many QFP with the step of 20 mil
Layout	10 layers, micro-via, via In-Pad
Complete Takaya test	17430 test steps
Version "Optimist"	67% of economy, remain 5700 test steps
Version "Pessimist"	39% of economy, remain 10700 test steps

This board with 10 layers (board B of table II) includes many BGA and QFP with pin spacing of 50 mil and less. The combination of boundary scan test and flying probe test produces a minimal saving of 39% on the number of test steps.

The degree of optimization is primarily related to the characteristics of the studied board and the care taken at the time of the design to obtain an adequate implementation of the boundary scan functionalities. A testability analysis is essential at the schematic stage if one wishes to benefit most from this test technique.

The reader might wonder about the value of a test which limited diagnostic capabilities, namely TestWay's Optimist version. Actually, if the two versions provide comparable test time reduction results, adopting the Optimist version would without a doubt, make a lot of sense. Assuming that the difference between the results from the Optimist version and the Pessimist version is significant, it would be worthwhile to evaluate the consequences for an organization where the Optimist test is used to detect the faultly boards with a diagnostic limitation. In that case, the batch of faultly boards should be tested a second time with the Pessimist program for an accurate diagnosis. Indeed if the rate of defects is relatively low and the difference between the two versions sufficiently significant, it is clear that the tester will be definitely be utilized less and, therefore will have a better profitability. ∎