SWTEST ASIA

PROBE TODAY, FOR TOMORROW

2019 CONFERENCE

Thursday, October 17
Proceedings

Welcome to SWTest Asia 2019

2nd Annual SWTest Asia Conference

On behalf of the SWTest Asia Team it is our great pleasure to welcome you to the Second Annual SWTest Asia EXPO at the Sheraton in Hsinchu, Taiwan. We would like to thank all our sponsors (8-platinum, 8-gold, and 8-silver), the 42 exhibitors, and the committee members as well as the volunteers for their support to make SWTest Asia a valuable event for the Asian wafer test industry.

Last year, the inaugural SWTest Asia Conference drew over 450 attendees with more that 45% of attendees from outside of Taiwan. More than 35% of the registered attendees were key engineers, managers, and decision makers from IDM, Foundry, and OSAT companies.

For 2019, we are pleased to have expanded the conference schedule into a two-day Technical Program with six themed sessions as well as a sold-out EXPO with 42 booths. The top probe card, probe equipment, and related service suppliers will have an opportunity to showcase their latest product offerings and technical services. Our goal with the focused EXPO is to provide our attendees with unprecedented access to the premier suppliers of technologies and services for the wafer test industry.

The popular “Tech Showcase” track will be held during the EXPO hours but will not conflict with the technical session schedule of the conference. SWTest Asia Conference and EXPO is rapidly becoming a must-attend event for the Asia wafer test industry.

New for SWTest Asia 2019, we started the “1st Annual Sponsors and Exhibitors Golf Tournament” to facilitate relaxed technical discussions, networking, and support our student travel grant awards.

Once again, thank you for being a part of the 2nd Annual SWTest Asia Conference and EXPO; and we hope that you enjoy your time in Taiwan and the Hsinchu area.

Jerry Broz, Ph.D.
General Chair
SWTest Asia

Clark Liu
Program Chair
SWTest Asia

Rey Rincon
Technical Program Co-Chair
SWTest Asia

Maddie Harwood
Finance Chair &
Conference Management
SWTest Asia

2019
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PROGRAM SCHEDULE

SWTest Asia 2019 - Platinum Sponsors

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PROGRAM SCHEDULE

SWTest Asia 2019 - Gold Sponsors

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2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

"Program Overview At A Glance"

Day One	Thursday, October 17th, 2019
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Chair's Opening Remarks*** ***Thursday Keynote Presentation in General Session Room*** Prof. Chen-Fu Chien, Ph.D. *Tsinghua Chair Professor & Micron Chair Professor at National Tsing Hua University*
10:15 – 10:45	Tea Break in the Registration Lobby
10:45 – 12:15	**"*Challenges for Next-Gen of Wafer Test*" in General Session Room** Full Conference Only
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions
14:00 – 15:30	**"*Big Data, Big Future*" in General Session Room** Full Conference Only – Expo Open
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall
16:00 – 17:30	**"*Challenges in Process Control Monitoring*" in General Session Room** Full Conference Only – Expo Open
17:30 – 18:30	Welcome Reception in Expo Hall

Day Two	Friday, October 18th, 2019
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Chair's Opening Remarks*** ***Friday Keynote Presentation in General Session Room*** Masahide Ozawa *Technical Consultant* at *Tokyo Electron Technology Solutions*
10:15 – 10:45	Expo Open & Tea Break in the Registration Lobby and Expo Hall
10:45 – 12:15	**"*Full Speed Ahead with 5G Solutions*" in General Session Room** Full Conference Only – Expo Open
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions
14:00 – 15:30	**"*Temperature Handling & Space Transformation*" in General Session Room** Full Conference Only – Expo Open
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall
16:00 – 17:30	**"*Advanced Probing Interface Solutions*" in General Session Room** Full Conference Only – Expo Open
17:30 – 17:45	Presentation Awards Ceremony
17:45 – 18:45	Closing Reception in Expo Hall

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

SWTest Team is proud to announce the 2nd Annual SWTest Asia conference to be held in Hsinchu, Taiwan, October 17-18, 2019. This two-day conference is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas. SWTest Asia promotes a friendly atmosphere with Technical Sessions, an EXPO, and a Tech Showcase, as well as our signature relaxed environment for "informal discussion and networking".

This event attracts attendees from the local and regional semiconductor industry that include ASE, TSMC, Ardentec, KYEC, SPIL, Micron, ChipMOS, UMC, Winbond, PTI, and more. Visitors to the conference will come from Japan, Korea, China, Singapore, India, Philippines, and Malaysia. Conference registration includes all meals, refreshments, social activities, and technical program and exhibit attendance, as well as the eProceedings.

Thursday, October 17th, 2019	
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Welcome to SWTest Asia 2019 – Day 1*** Dr. Jerry Broz, SWTest Asia General Chair Clark Liu, SWTest Asia Technical Program Chair
	Thursday Keynote Presentation ***"Industry 3.5" to Empower Intelligent Manufacturing and Empirical Studies in Taiwan***  **Prof. Chen-Fu Chien, Ph.D.** **Tsinghua Chair Professor & Micron Chair Professor** Department of Industrial Engineering & Engineering Management National Tsing Hua University, Taiwan
10:15 – 10:45	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Thursday Program Overview

Technical Session 1 **10:45 – 12:15**	**Challenges for Next-Gen of Wafer Test** **Session Chair**: Dr. Jerry Broz, General Chair (International Test Solutions)
10:45 – 11:15	**Advanced Packaging — It's Changing The World Of Wafer Test** Amy Leong (FormFactor Inc. – USA)
11:15 – 11:45	**Methodology of VCSEL Probing and Testing** Hector Lin, Douglas Tsai, and Gary Liu (MPI Corporation – Taiwan)
11:45 – 12:15	**Probing Technology Challenge: Now and Future** Clark Liu, Henry Tseng, and Jason Sung (PTI – Taiwan)
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions

Technical Session 2 **14:00 – 15:30**	**Big Data, Big Future** **Session Chair:** Joey Wu (SWTest Member at Large)
14:00 – 14:30	**Wafer Defect Diagnosis With Test Big Data Driven Techniques** Prof. Katherine Shu-Min Li (National Sun Yat-Sen University – Taiwan) Andrew Huang, Chau Cheung Cheng, Chengyen Tsai, Leon Chou, Yi Yu Liao, and Chen Hsun Lee (NXP Semiconductors - Taiwan)
14:30 – 15:00	**Probe Card Electrical Quality Enhancement Using Big Data Analytics** Kenny Huang, Fred Chou, Alex Wei, Steven Wu (MPI Corporation – Taiwan) Ying-Jen Chen (DALab Solutions x Associates Co., Ltd., Taiwan – Taiwan) Yu-Mei Ling, Yi-Yu Chen and Prof. Chen-Fu Chien (National Tsing Hua University – Taiwan)
15:00 – 15:30	**Testing the Spatial Pattern Randomness on Wafer Maps** Prof. Jwu E Chen, Prof. Hsing-Chung Liang, and Tung Ying Lu (National Central University – Taiwan)
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall

Technical Session 3 **16:00 – 17:30**	**Challenges in Process Control Monitoring** **Session Chair:** Nobuhiro Kawamata (FormFactor KK – Japan)
16:00 – 16:30	**Reducing Wafer Parametric Test Costs By High Speed Test Solution** Yu Cheng Su (National Instruments – Taiwan) Mark Lu (Semitronix – China)
16:30 – 17:00	**Advances In Position Measurement And Analysis For Guide Plate Microholes** Michael Cullimore and Dr. Alan Ferguson (Oxford Lasers – United Kingdom)
17:00 – 17:30	**Takumi CL – New 2D-MEMS Spring Introduction to Formfactor Parametric Probe Card and Comparison with 3D MEMS Spring** Takao Saeki (Formfactor KK – Japan)
17:30 – 18:30	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Friday, October 18th, 2019	
8:00 – 17:00	Attendee Registration Open
9:00 – 10:15	***Welcome to SWTest Asia 2019 – Day 2*** Dr. Jerry Broz, SWTest Asia General Chair Clark Liu, SWTest Asia Technical Program Chair
	Friday Keynote Presentation ***Wafer Test Value and Future***  **Masahide Ozawa** **Technical Consultant** Tokyo Electron Technology Solutions - Japan
10:15 – 10:45	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Friday Program Overview	
Technical Session 4 **10:45 – 12:15**	**Full Speed Ahead with 5G Solutions** **Session Chair**: Dr. Jerry Broz, General Chair (International Test Solutions)
10:45 – 11:15	**Getting Ready For The Next Wave Of Growth** John West (VLSI Research Europe – United Kingdom)
11:15 – 11:45	**5G Enhanced Micro-Cantilever Membrane Probing Solutions** Jed Hsu and Jordan Smalls (Translarity, Inc. – USA)
11:45 – 12:15	**How To Successfully Embrace The Era Of 5g Mmwave Test** Yu Cheng Su (National Instruments – Taiwan)
12:15 – 14:00	Expo Open – Lunch in Expo Hall – Two Sessions

Technical Session 5 **14:00 – 15:30**	**Advanced Thermal Handling & Space Transformation** **Session Chair:** Dr. Alan Ferguson (Oxford Lasers – United Kingdom)
14:00 – 14:30	**Ultra High Temperature Production Probe Card Solution for Automotive IC Testing** Alan Liao (FormFactor – USA) and Hirofumi Nagata (FormFactor – Japan)
14:30 – 15:00	**Space Transforming Probes** Gary Grube and Dominik Schmidt (Translarity Inc. – USA)
15:00 – 15:30	**Temperature Accuracy At High Wattage Wafer Test – A Novel Method To Control Device Temperature** Klemens Reitinger (ERS electronic GmbH – Germany)
15:30 – 16:00	Expo Open & Tea Break in the Registration Lobby and Expo Hall

Technical Session 6 **16:00 – 17:30**	**Advanced Probing Interface Solutions** **Session Chair:** Clark Liu (PTI – Hsinchu, Taiwan))
16:00 – 16:30	**Overview Of Specialized Testing For Mems Sensors; Wafer Probe & Final Test** Michael Ricci (Rika Denshi Group, LTD – Japan)
16:30 – 17:00	**Innovative Probe Card Analyzer Solutions For Next Generation Probe Cards** John Strom (Rudolph Technologies – USA)
17:00 – 17:30	**A New Framework to Manage Device Interface Complexity For The Next Decade** Steve Ledford (Teradyne – USA)
17:30 – 18:30	Expo Open & Tea Break in the Registration Lobby and Expo Hall

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

2019 EXHIBITORS

Advantest
ATT Systems GmbH
Celadon Systems Inc.
Chain-Logic International Corp.
CHPT
Dynamic Test Solutions Asia Pte Ltd.
ERS electronic GmbH
Feinmetall GmbH
Ferrotec Ceramics Corporation
FormFactor
Hermes Testing Solutions Inc.
Hitachi Chemical Co., Ltd.
Integrated Technology Corporation
International Test Solutions
inTEST EMS
ISC Co., Ltd.
IWIN Co., Ltd.
JEM Taiwan Probe Corp.
Laser Job, Inc.
MJC Taiwan
MPI Corporation
Nagase (Taiwan) Co., Ltd.
National Instruments
NHK Spring Co., Ltd.
Nidec SV TCL
Oxford Lasers
PLI Co., Ltd.
Posalux SA
Rudolph Technologies, Inc.
Saehan Microtech
SEMICS Inc.
Shyan Sheng Hitech
Specialty Coating Systems
STAr Technologies, Inc.
T.I.P.S. Messtechnik GmbH
Tanaka Precious Metals
Technoprobe America Inc.
Teradyne, Incorporated
Veco Precision
Wentworth Laboratories Ltd.
WinWay Technology Co., Ltd.
WONIK QnC Corporation

2019

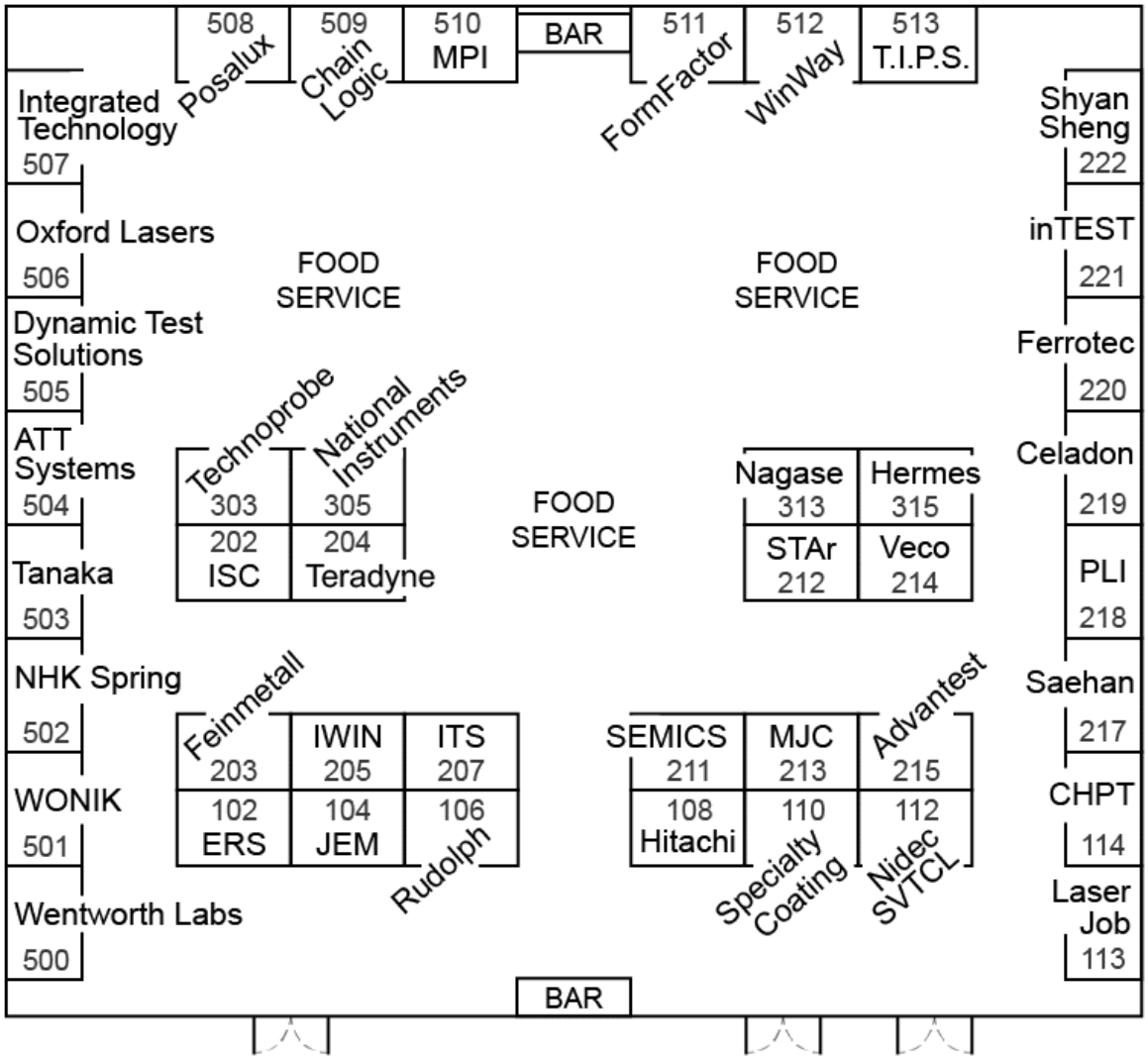
SWTest Asia Conference

SWTEST ASIA

PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

EXPO HALL



2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

3nd Annual SWTest Asia

Coming in October, 2020
(dates will be announced soon!)

2019
SWTest Asia
Conference

SWTEST ASIA
PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

30th Anniverary SWTest

June 7 to 10, 2020

Rancho Bernardo Inn

San Diego, California

Technical Program
SWTest Asia 2019

Thursday, October 17, 2019

Hsinchu, Taiwan, October 17-18, 2019

Thursday, October 17, 2019

9:00 to 9:15 – Welcome to SWTest Asia

Dr. Jerry Broz (SWTest Asia General Chair) and Clark Liu (SWTest Program Chair)

9:15 to 10:15 – Keynote Speaker

"Industry 3.5" to Empower Intelligent Manufacturing and Empirical Studies in Taiwan

Prof. Chen-Fu Chien, Ph.D.

Tsinghua Chair Professor & Micron Chair Professor
Department of Industrial Engineering & Engineering Management
National Tsing Hua University, Taiwan

Thursday, October 17, 2019

10:45 to 12:15 – Challenges for Next-Gen of Wafer Test

Advanced Packaging — It's Changing The World Of Wafer Test

Amy Leong (FormFactor Inc. – USA)

Methodology of VCSEL Probing and Testing

Hector Lin, Douglas Tsai, and Gary Liu (MPI Corporation – Taiwan)

Probing Technology Challenge: Now and Future

Clark Liu, Henry Tseng, and Jason Sung (PTI – Taiwan)

Thursday, October 17, 2019

14:00 to 15:30 – Big Data, Big Future

Wafer Defect Diagnosis With Test Big Data Driven Techniques

Prof. Katherine Shu-Min Li (National Sun Yat-Sen University – Taiwan)

Andrew Huang, Chau Cheung Cheng, Chengyen Tsai, Leon Chou, Yi Yu Liao, and Chen Hsun Lee (NXP Semiconductors - Taiwan)

Probe Card Electrical Quality Enhancement Using Big Data Analytics

Kenny Huang, Fred Chou, Alex Wei, Steven Wu (MPI Corporation – Taiwan)

Ying-Jen Chen (DALab Solutions x Associates Co., Ltd., Taiwan)

Yu-Mei Ling, Yi-Yu Chen and Prof. Chen-Fu Chien (National Tsing Hua University – Taiwan)

Testing the Spatial Pattern Randomness on Wafer Maps

Prof. Jwu E Chen, Prof. Hsing-Chung Liang, and Tung Ying Lu (National Central University – Taiwan)

Thursday, October 17, 2019

16:00 to 17:30 – Challenges in Process Control Monitoring

Reducing Wafer Parametric Test Costs By High Speed Test Solution

Yu Cheng Su (National Instruments – Taiwan) and Mark Lu (Semitronix – China)

Advances In Position Measurement And Analysis For Guide Plate Microholes

Michael Cullimore and Dr. Alan Ferguson (Oxford Lasers – United Kingdom)

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Takao Saeki (Formfactor KK – Japan)

Technical Program
SWTest Asia 2019

Thursday, October 17, 2019

Hsinchu, Taiwan, October 17-18, 2019

Welcome to the 2st Annual SWTest Asia in Taiwan

Jerry Broz, Ph.D.
General Chair, SWTest Asia
International Test Solutions

Clark Liu
Technical Program Chair, SWTest Asia
Powertech Technology, Inc.

Hsinchu, Taiwan, October 17-18, 2019

Welcome to the Sheraton, Hsinchu !

SWTest Asia and SWTest San Diego

- **SWTest Conferences are Probe Technology Forums …**
  - Premier Conferences for Wafer Test Professionals and Probing Technologists.
  - Balanced mixture of manufacturers and suppliers as well as collaborative presentations
  - Practical solutions to real problems that are faced by test engineers

- **Thirty-Two Combined Years of Probe Technology …**
  - 2nd SWTest Asia in Taiwan brings a "workshop style" conference to Asia Semiconductor community.
  - SWTest in San Diego has more than 9500 worldwide attendees to discuss probe technology.

- **Informal and Networking Conferences …**
  - Focused technical exchange
  - Great social activities and informal discussions
  - Meet new people and have a little fun !

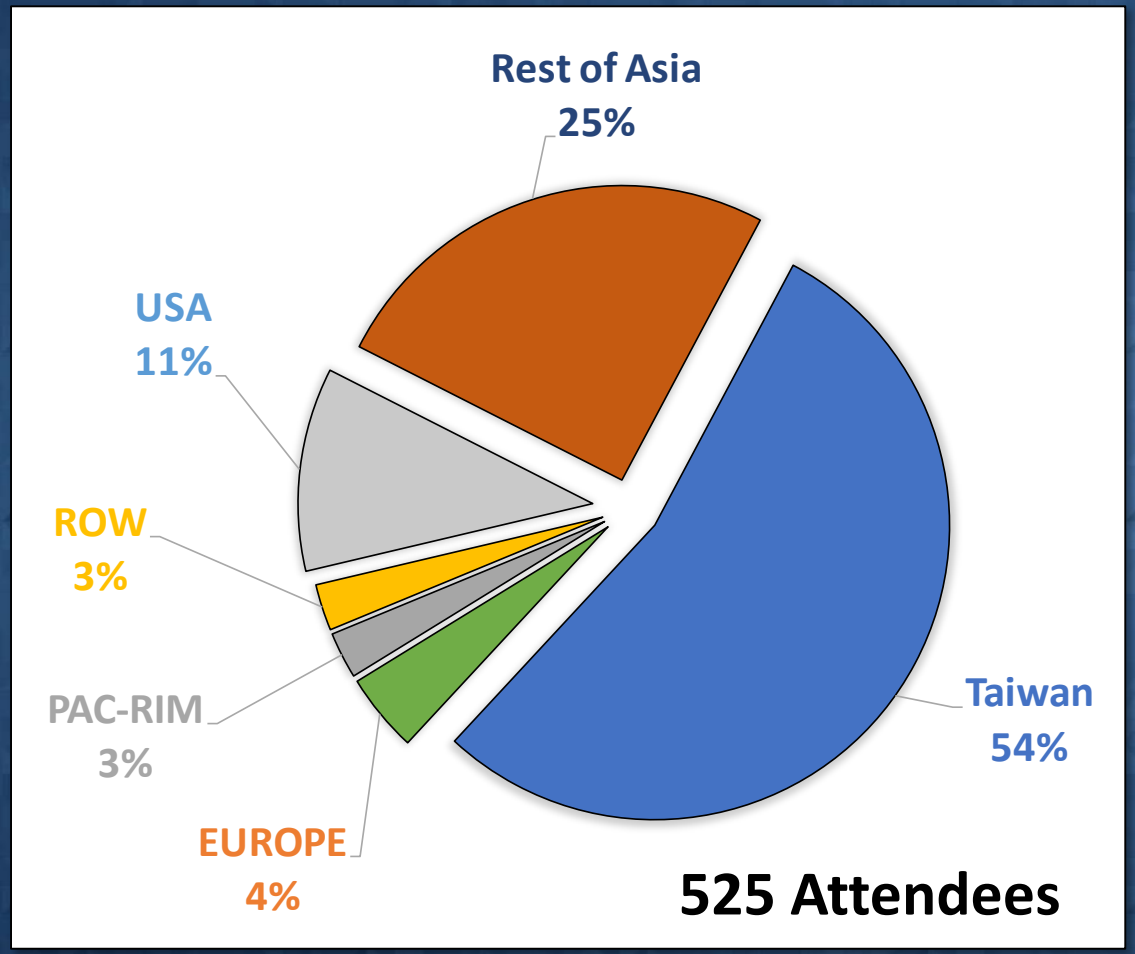
SWTEST ASIA

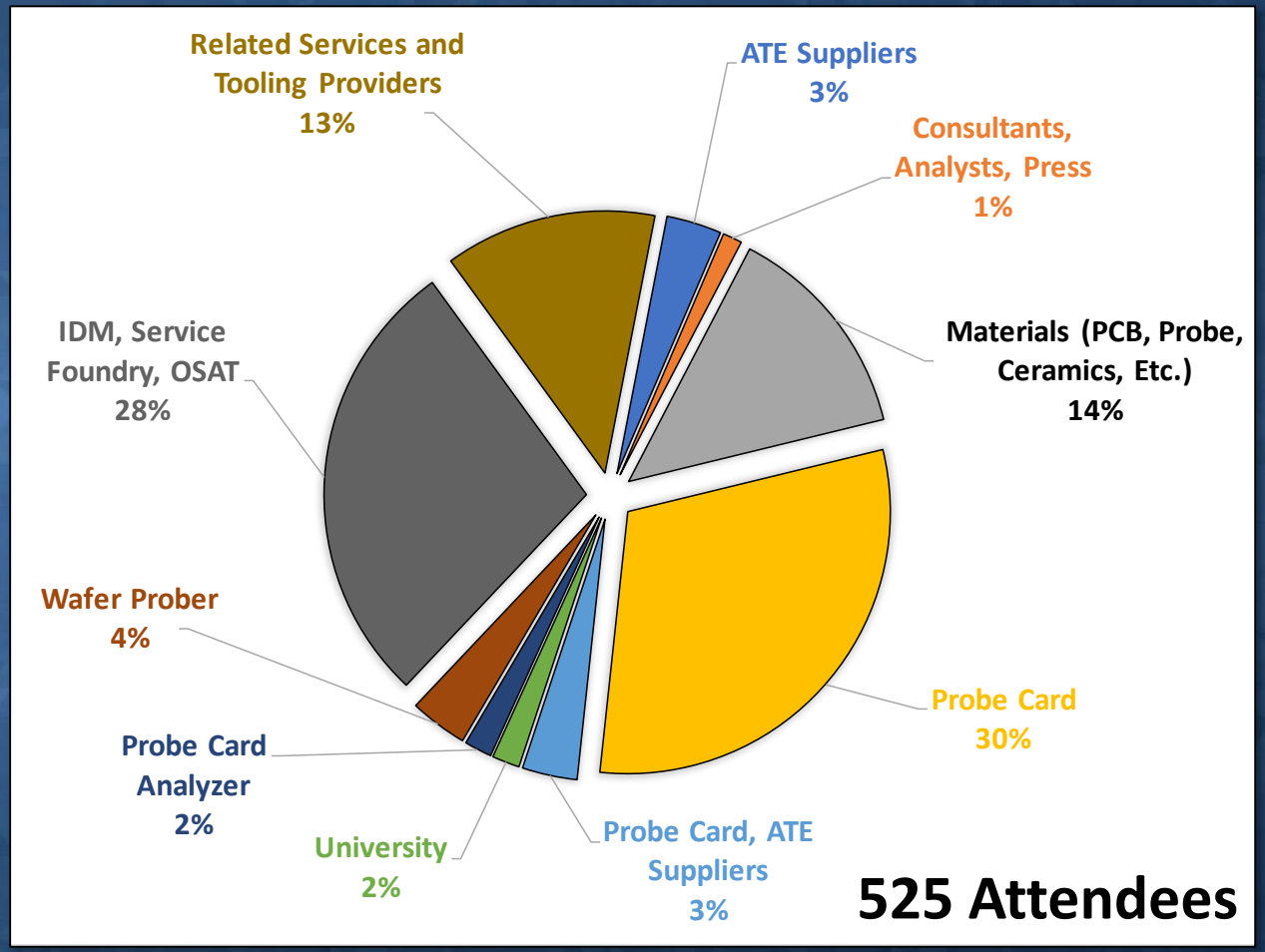
Held During
October
In Asia Region

SWTEST
PROBE TODAY, FOR TOMORROW

Held During
June
In San Diego, CA

SWTest Asia 2019 Demographics





SWTest Asia Chairs and Committee

- **SWTest Asia Chairs**
  - Dr. Jerry Broz, General Chair (International Test Solutions – USA)
  - Clark Liu, SWTest Asia Technical Program Chair (Powertech Technology, Inc. – Taiwan)
  - Rey Rincon, Technical Program Co-Chair (Translarity, Inc. – USA)
  - Maddie Harwood, Finance and Conference Management Chair (SWTest Conferences)

- **SWTest Asia Steering Committee**
  - Nobuhiro Kawamata (Formfactor, K.K. – Japan)
  - Alex Yang (MPI Corporation – Taiwan)
  - Alan Ferguson, Ph.D. (Oxford Lasers, Inc., United Kingdom)
  - Joey Wu (SWTest Member at Large – Taiwan)
  - Haruko Yoshii (Formfactor, K.K. – Japan)

SWTest Asia 1st Annual Benefit Tournament

老爺關西高爾夫球場
Royal Kuan-Hsi Golf Club

Wednesday, October 16, 2019

SWTest Asia 2019 on October 17 to 18, 2019

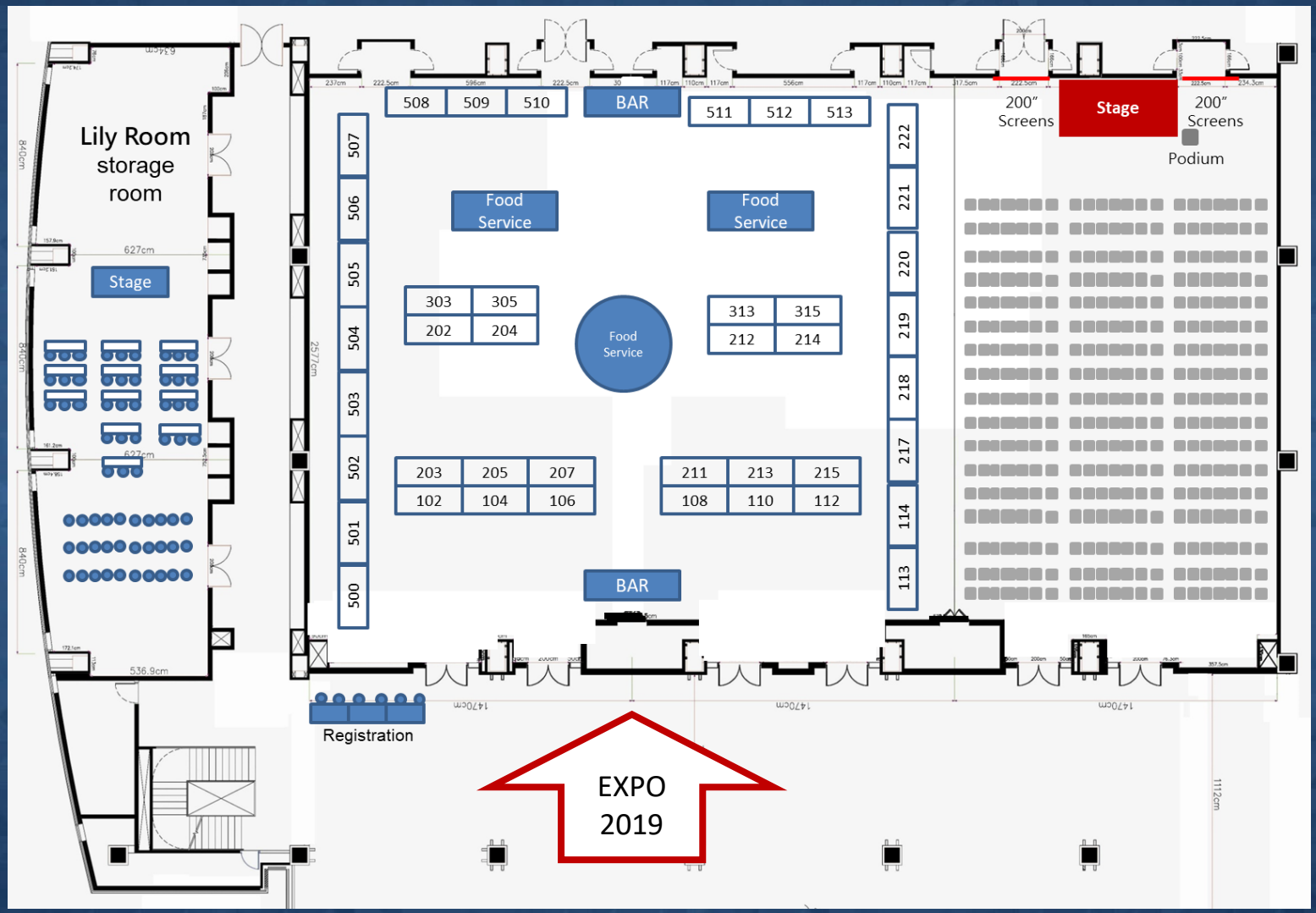
Thursday, October 17

- Keynote from Prof. Chen-Fu Chien, Ph.D., Tsinghua Chair Professor & Micron Chair Professor at National Tsing Hua University
- Technical Program with 3-podium sessions
  - 1045 – 1215: Challenges for Next-Gen of Wafer Test
  - 1400 – 1530: Big Data, Big Future
  - 1600 – 1730: Challenges in Process Control Monitoring
- SWTest Asia EXPO 2019 with 42-key suppliers
- Technology Showcase Presentations by Platinum Sponsors
- Welcome Reception in Expo Hall

Friday, October 18

- Keynote from Masahide Ozawa, Technical Consultant at Tokyo Electron Technology Solutions
- Technical Program with 3-podium sessions
  - 1045 – 1215: Full Speed Ahead with 5G Solutions
  - 1400 – 1530: Advanced Thermal Handling & Space Transformation
  - 1600 – 1730: Advanced Probing Interface Solutions
  - Awards for “Best Presentations” selected by committee.
- SWTest Asia EXPO 2019 with 42-key suppliers
- Technology Showcase Presentations by Platinum Sponsors
- Closing Reception in Expo Hall

Map of the Area



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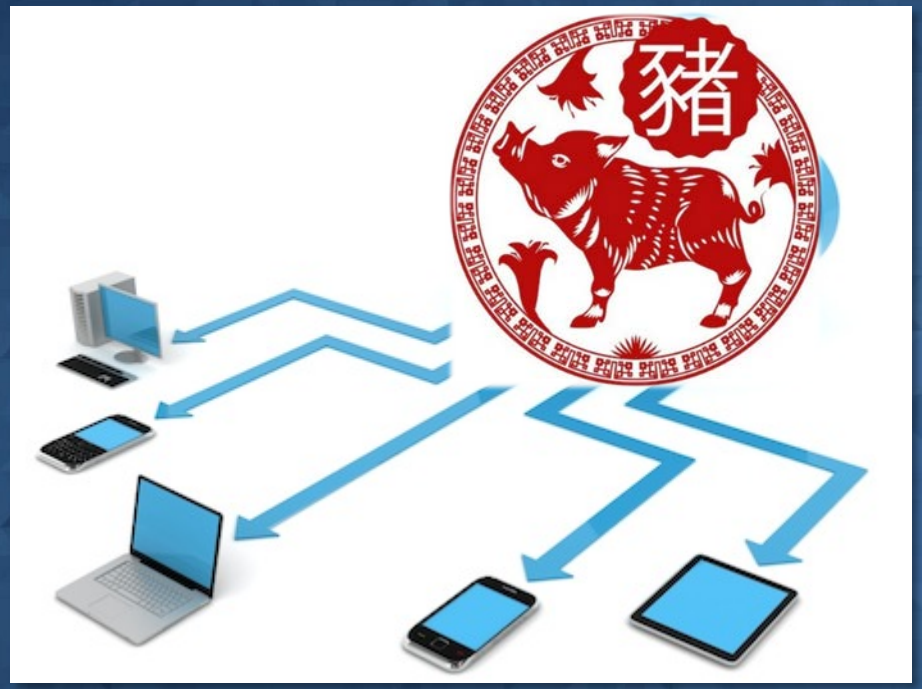
Tech Showcase

Technical
Program

EXPO
2019

SWTest Asia 2019 eProceedings



ePROCEEDINGS Password:

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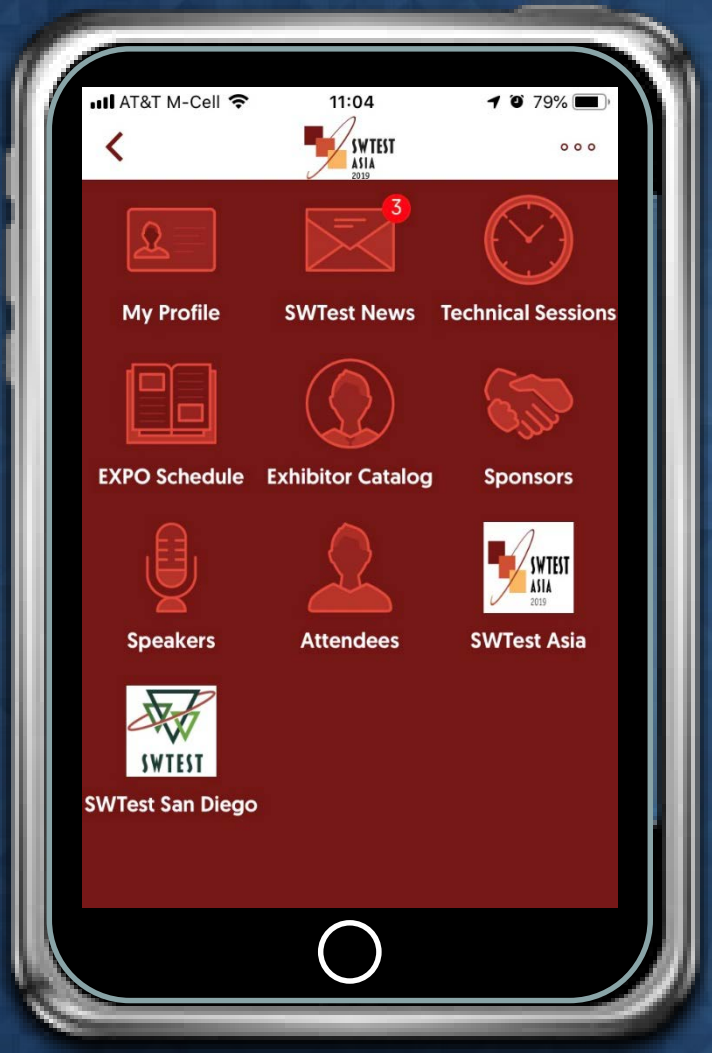
- **Conference e-Version is available for download in a password protected file.**
  - **Ballroom WiFi = SAP03**
  - **Go to … http://www.swtestasia.org … to download the daily eProceedings.**
- **Free WiFi access will be available during the entire conference to allow attendee access to the downloads.**
- **Password for the download files will be announced throughout each day and at the registration desk.**
- **Non-password locked files (including the Keynote presentations) will be made available in the SWTest Asia Archives after the conference adjourns.**

SWTest Asia App – “In the Palm of Your Hand”



- Up-to-the-minute updates in “SWTest News”
- Schedules of the “Technical Sessions”
- Meet with the “Exhibitors” and “Sponsors”
- Connect with the “Speakers”
- Attend the “Tech Showcase”
- Get oriented on the “Floorplan”
- Network with the “Attendees”
- Learn about “SWTest in San Diego”

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Platinum Sponsors

Gold Sponsors

Silver Sponsors

Thursday Keynote Speaker

"Industry 3.5" to Empower Intelligent Manufacturing and Empirical Studies in Taiwan

Prof. Chen-Fu Chien, Ph.D.

Tsinghua Chair Professor & Micron Chair Professor
Department of Industrial Engineering & Engineering Management
National Tsing Hua University, Taiwan

國立清華大學
National Tsing Hua University

Technical Program
SWTest Asia 2019

Thursday, October 17, 2019

Hsinchu, Taiwan, October 17-18, 2019

3rd Annual SWTest Asia Coming in October, 2019

(dates will be announced soon !)

Thanks for Attending SWTest Asia !

We Hope to See you at SWTest San Diego

June 7 – 10, 2020
Rancho Bernardo Inn San Diego, California

SWTEST
PROBE TODAY, FOR TOMORROW
2020 CONFERENCE

Join us in celebrating our 30th Anniversary

30 YEAR ANNIVERSARY

Thanks for your Support !

- **Contact the SWTest Asia Team with any questions**

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SWTEST ASIA 2019

Advanced Packaging – It's Changing the World of Wafer Test

Amy Leong, Mike Slessor
FormFactor Inc.

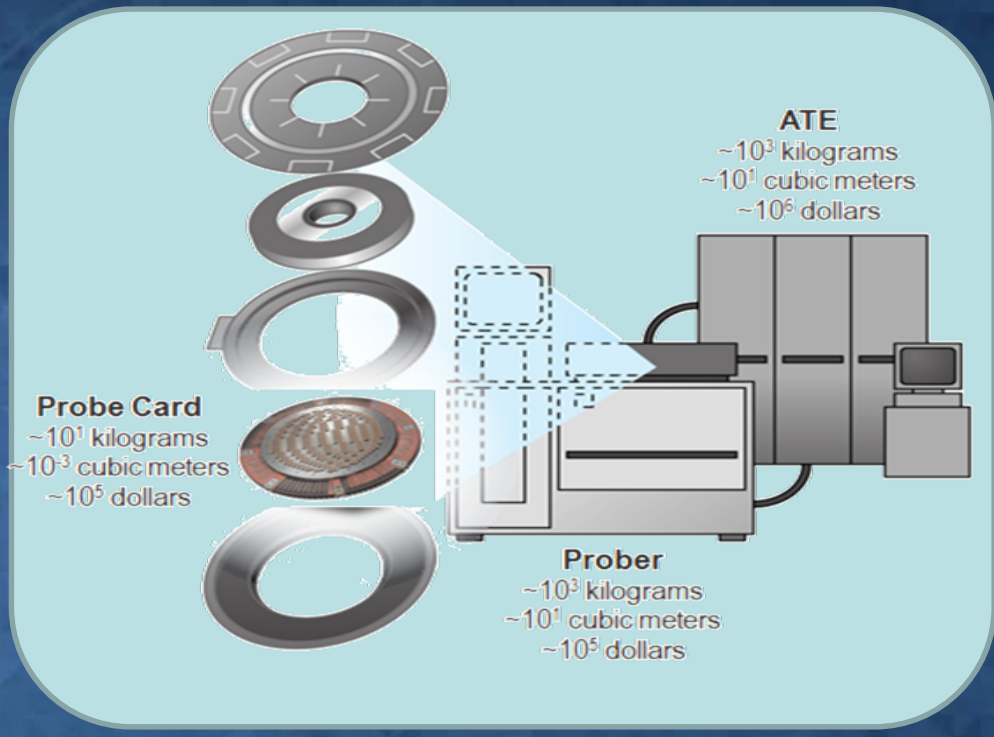
Hsinchu, Taiwan, October 17-18, 2019

The Next 25 Mins

- **Setting the stage**
  - What is “wafer test”?
  - What is “advanced packaging”?
- **Recognizing the challenges**
  - How does advanced packaging impact wafer test?
- **Responding with solutions**
  - What are some practical examples and options for advanced packaging wafer test?
- **Q&A**

What is Wafer Test?

- **Electrical test after wafer fab, prior to backend assembly / final packaging**
- **DUT(s)-to-ATE connection typically made through same contacts that connect die to package**
  - Wirebond pads, flipchip bumps, copper pillars, etc.
- **Key components of wafer-test cell:**
  - ATE: Instruments & power supplies to stimulate and interrogate the DUT(s)
  - Prober: Wafer (die) handling, positioning, and environment
  - Probe card: Device-specific interface providing DUT(s)-to-ATE connection



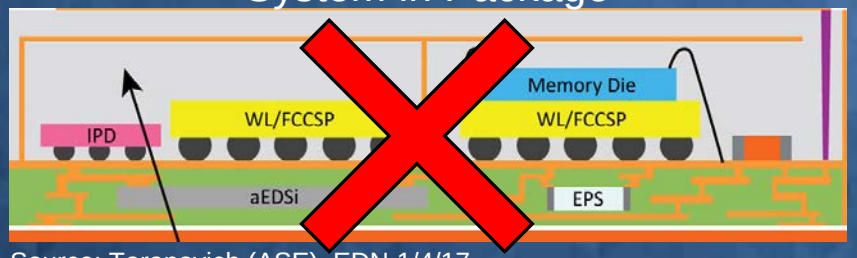
Why Do Customers Spend $$$ On Wafer Test?

- **Avoid wasted cost of packaging a bad die**
  - Valuable when yield low and backend cost high
  - Test cost must be << bad-die packaging cost
- **Inform an adjustment/trim/change**
  - Exercise redundancy (DRAM)
  - Feedback for frontend fab process changes
- **As outgoing QC for product title transfer**
  - Bare-die sales (or wafer-packaged die)
  - Foundry-fabless-OSAT handoffs

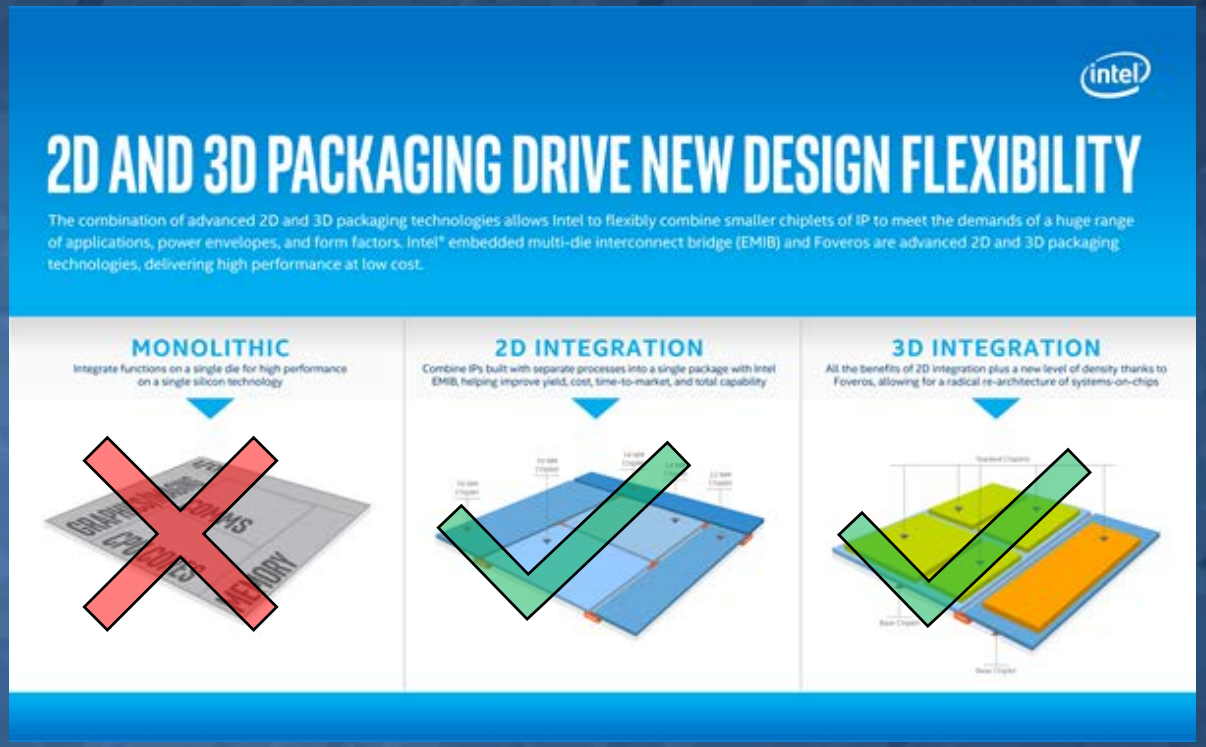
Wafer Test Coverage			
Die Yield	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

What Do We Mean By “Advanced Packaging”?

System in Package



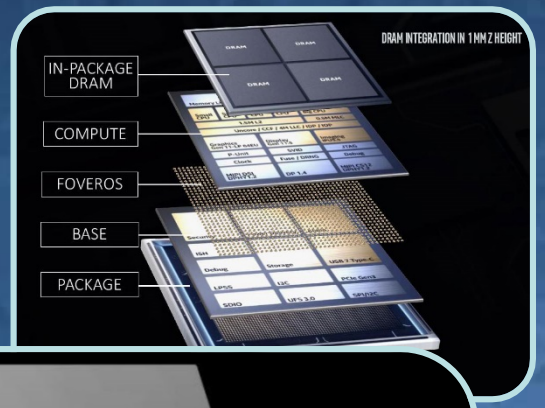
Source: Taranovich (ASE), EDN 1/4/17

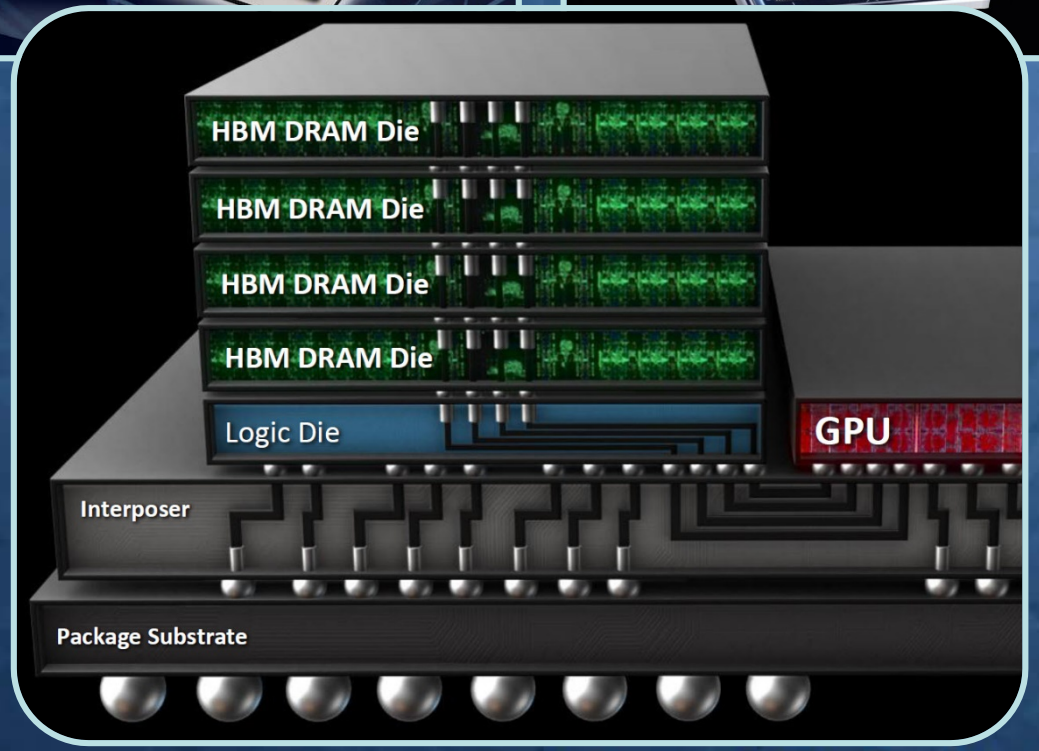


Source: https://newsroom.intel.com/wp-content/uploads/sites/11/2018/12/2d-and-3d-packaging-drive-new-design-flexibility.jpg

Advanced Packaging = Assembly of multiple die either directly to each other or through interfaces with interconnect densities and electrical performance comparable to that of the individual component die

Advanced Packaging Examples – FPGA, CPU, GPU

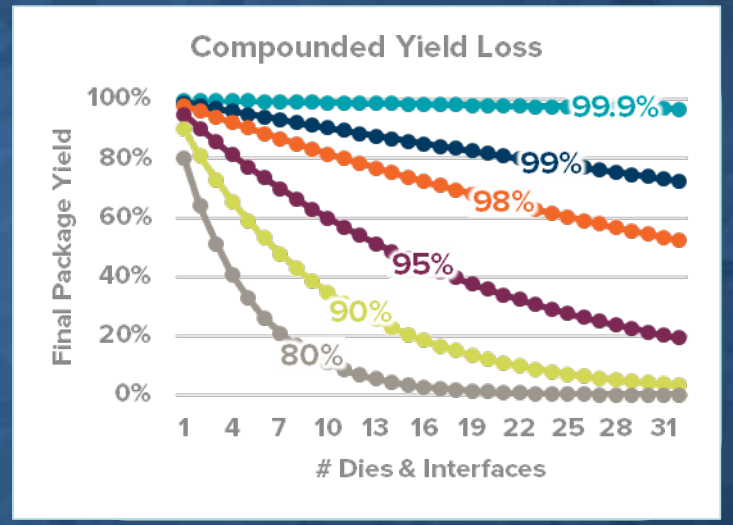




- **Heterogenous integration:**
  - 7nm/10nm high-perf core GPU, CPU, FPGA
  - 1Xnm/2Xnm lower-power cores
  - 1Ynm LPDDR/GDDR – up to 8 layers!
  - Other logic, display, comm, I/O functions
  - Mix/match best technologies
- **Silicon interposer density enables wide high-speed buses/interfaces**
- **10,000s vertical signal pipes (TSVs) at 40µm~60µm pitch**
- **Smaller, faster, lower-power, cheaper**

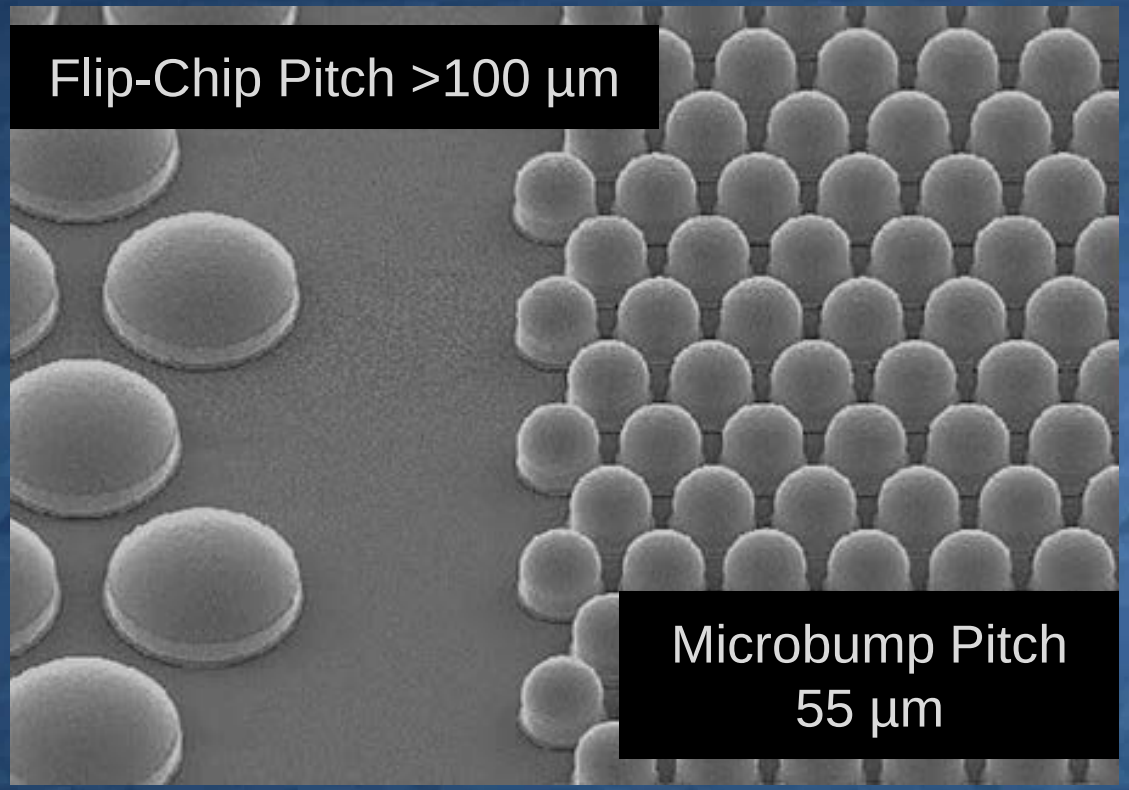
How Does Advanced Packaging Impact Test? Coverage!

- **Final test of assembled package is necessary, but provides limited insight to improve performance and yield**
- **Ideally, each component is good before integration**
  - Nirvana is Known Good Die (KGD)
  - Test every individual die, and every stacking step along the way?
- **Economics dictate something shy of KGD**
  - Pre-package wafer test is fundamentally scrap-cost avoidance
  - Final-test and system-test opportunities prevent escapes
  - Schedule, risk tolerance, etc. are other practical considerations
- **Cost vs. coverage optimization comes down to math**
  - Compromise = Probably Good Die (PGD)
  - Hedge bets – e.g., design interposers/ bridges with redundant vias, and build repairability into each HBM sub-die
  - Balance test coverage to catch higher-probability/impact issues, while accepting risk of lesser issues slipping through to final test

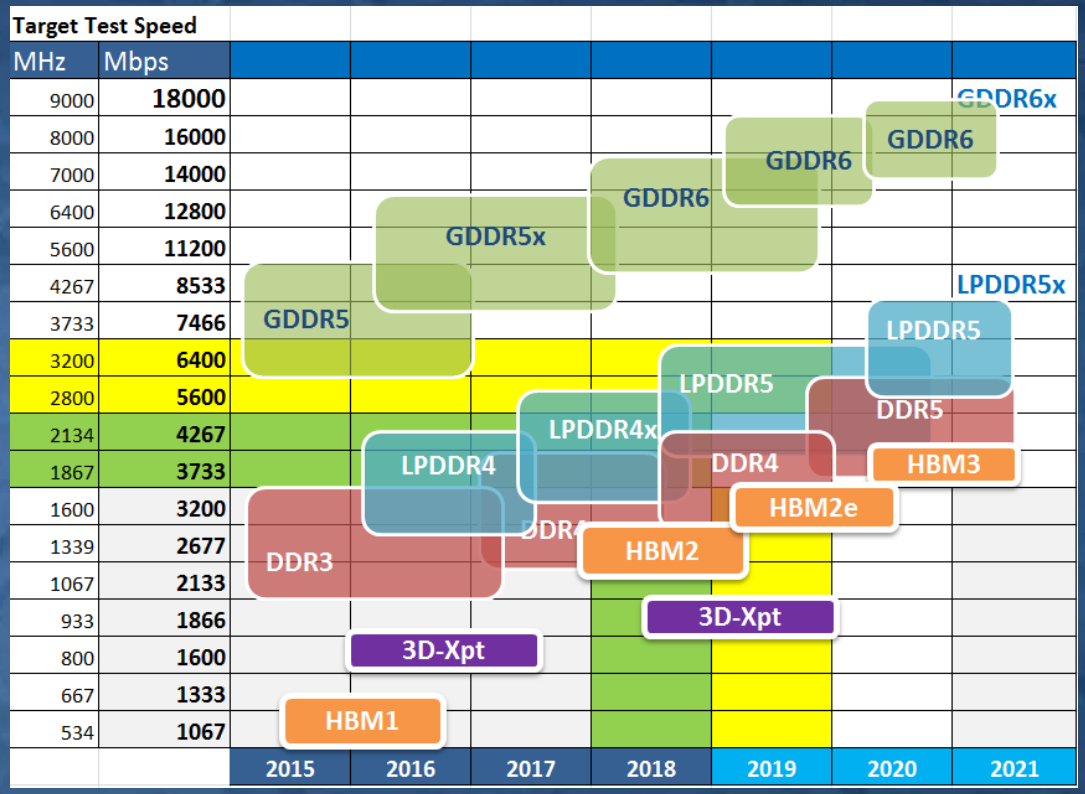


Wafer Test Coverage			
Die Yield	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

How Does Advanced Packaging Impact Test? Complexity!



https://www.tomshardware.com/news/intel-emib-interconnect-fpga-chiplet,35316.html



Spatial/Mechanical – Higher Density

- Smaller pitches and higher probe counts
- More delicate contacts (new materials)

Electrical – Higher Performance

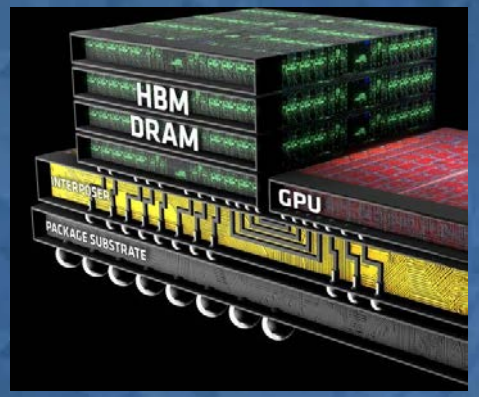
- Higher clock speeds, nearing RF frequencies
- Increased current per contact, higher power density

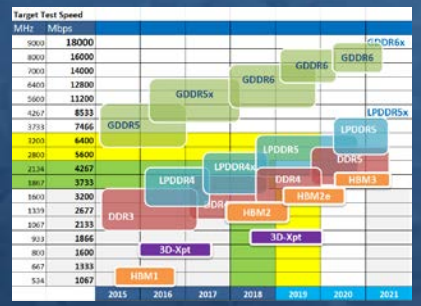
Finding A Balance Between Cost, Coverage, and Complexity

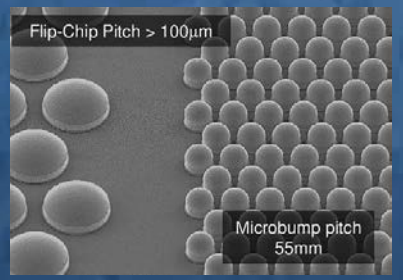
Coverage

Wafer Test Coverage			
Die Yield	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

KGD



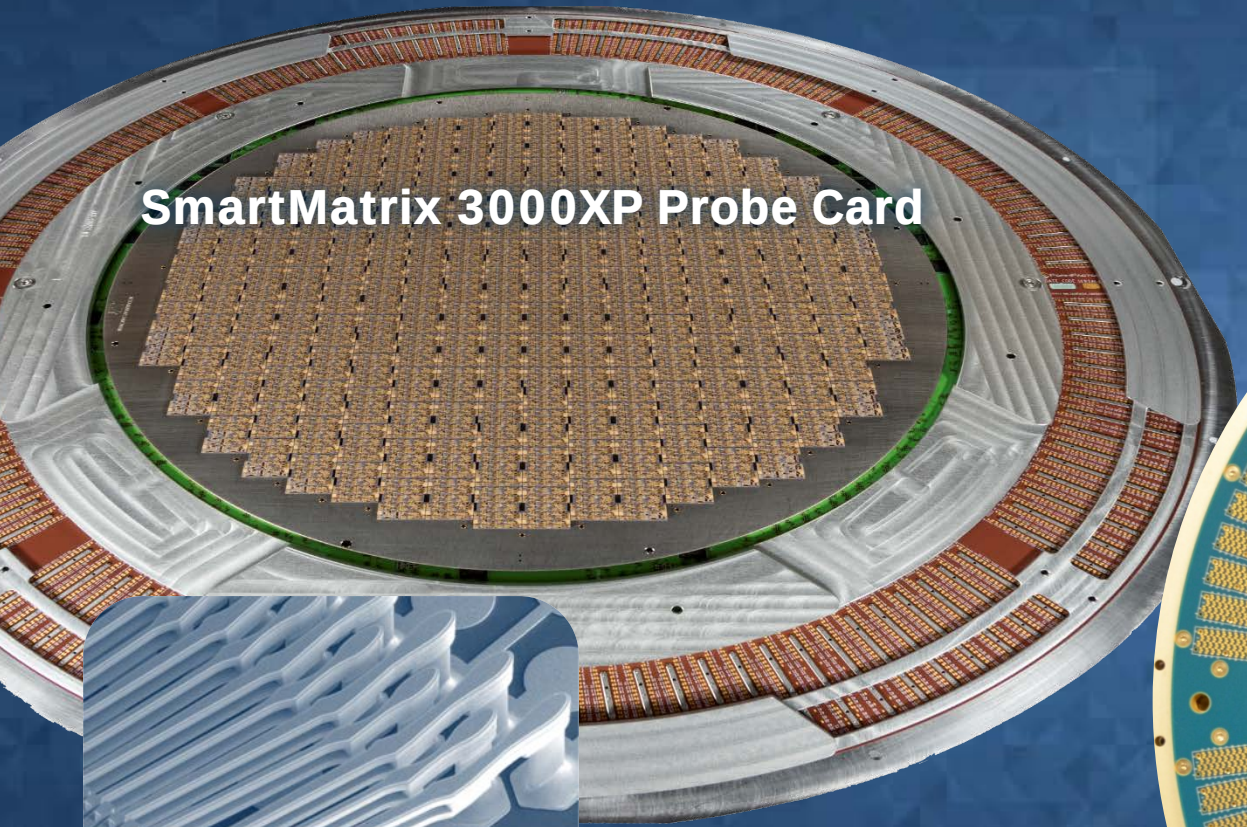


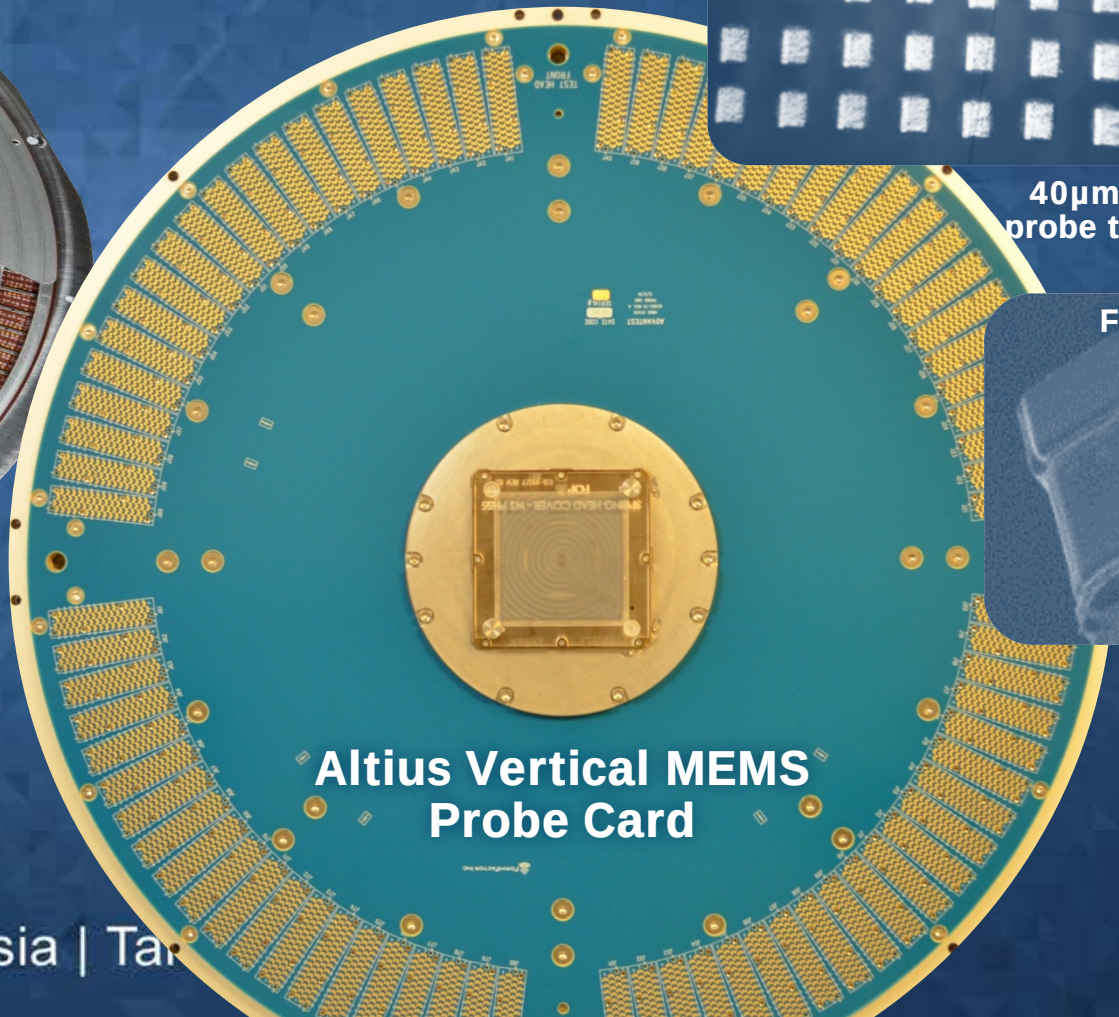


- **Test cost is a function of both coverage and complexity**
- **Increasing coverage almost always means increasing test times**
  - Lower unit throughput
  - Potential DFT/BIST offsets
- **More complexity always means more expensive test cells**
  - Novel approaches needed to break scaling, eg, single-die test

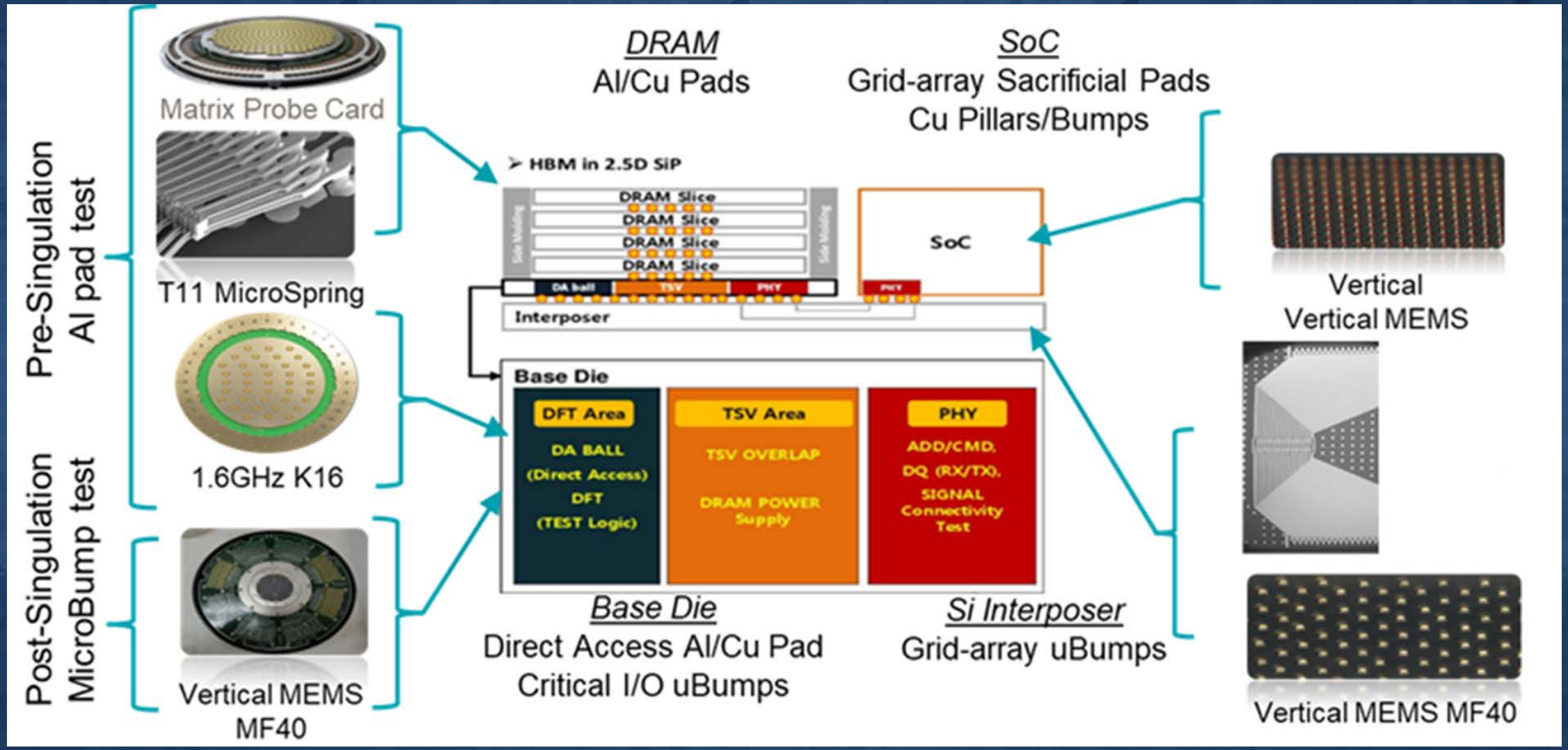
Complexity

Fortunately, Good Solutions Exist Today

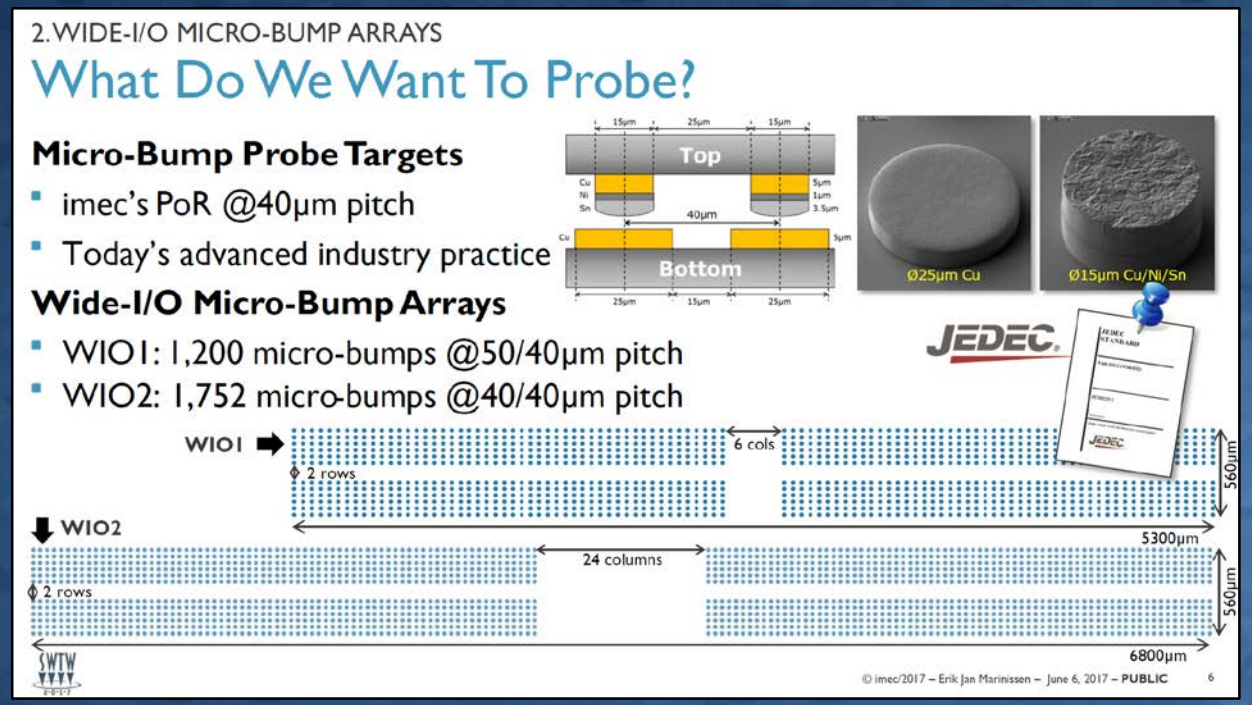


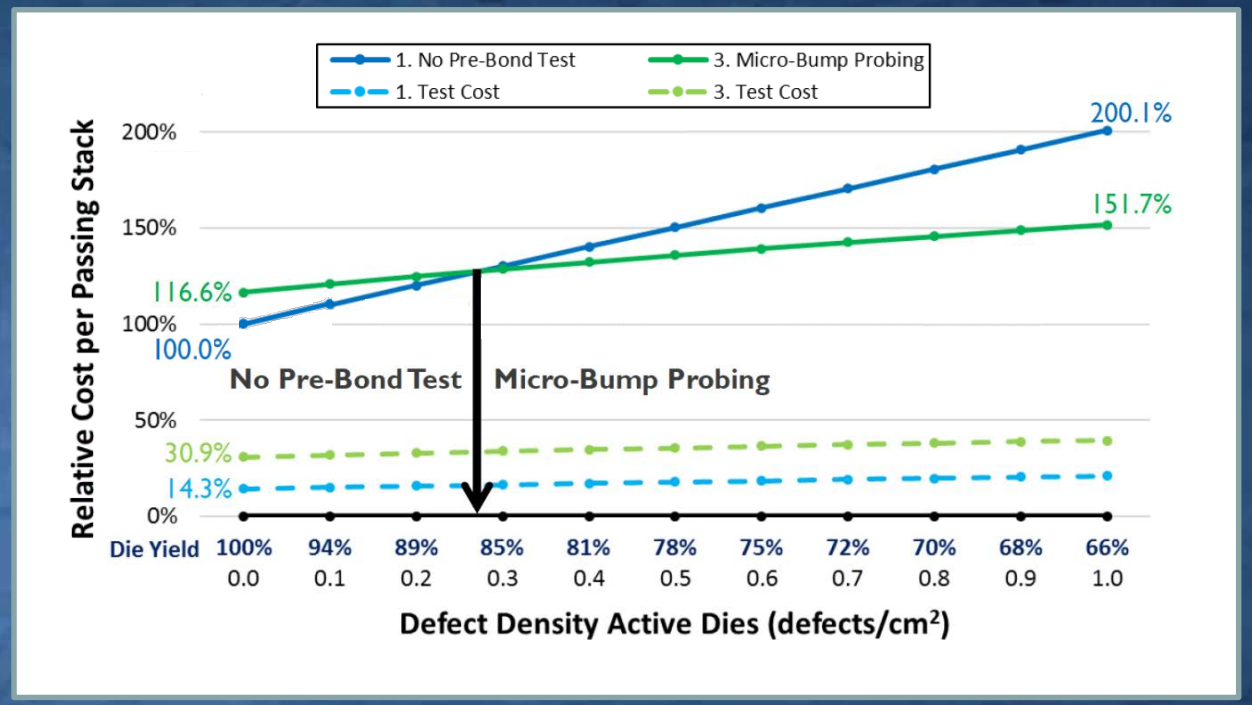


What to Test? So Many Possible Test Insertions…



Example – Directly Probing Microbumps On Interposer on Wafer





Probing directly on microbumps on wafer prior to packaging can be done

Depending on yield, it might (or might not) save money in the end – decide using data

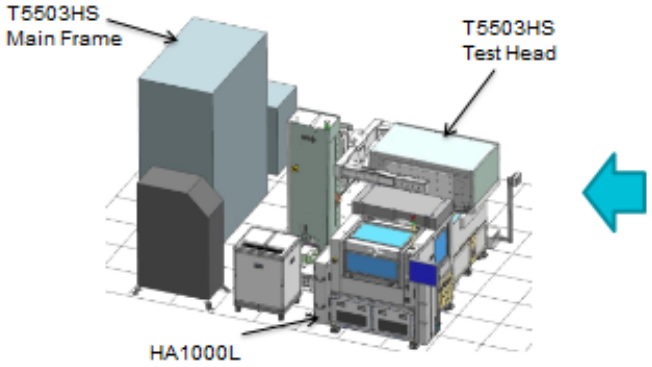
Example – Probing Microbumps on Singulated HBM for Die-level Functional Test

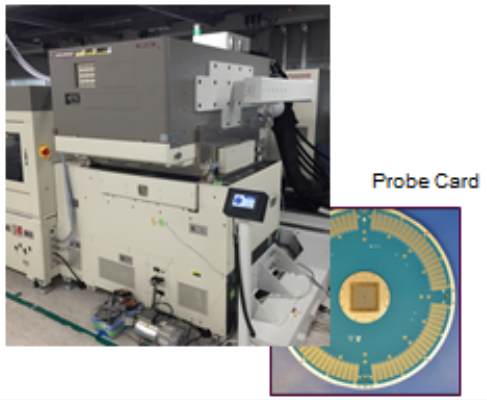
Direct micro-bump probing – Bare Die Handler

Die Handling & Micro Bump Contact are needed

HBM KGSD Test Solution

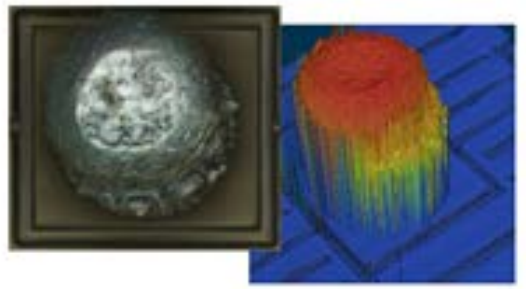
- HA1000L : Die Level Handler (Advantest)
- T5503HS : Memory Test System (Advantest)
- Probe Card : Probe Card for HBM (FFI)

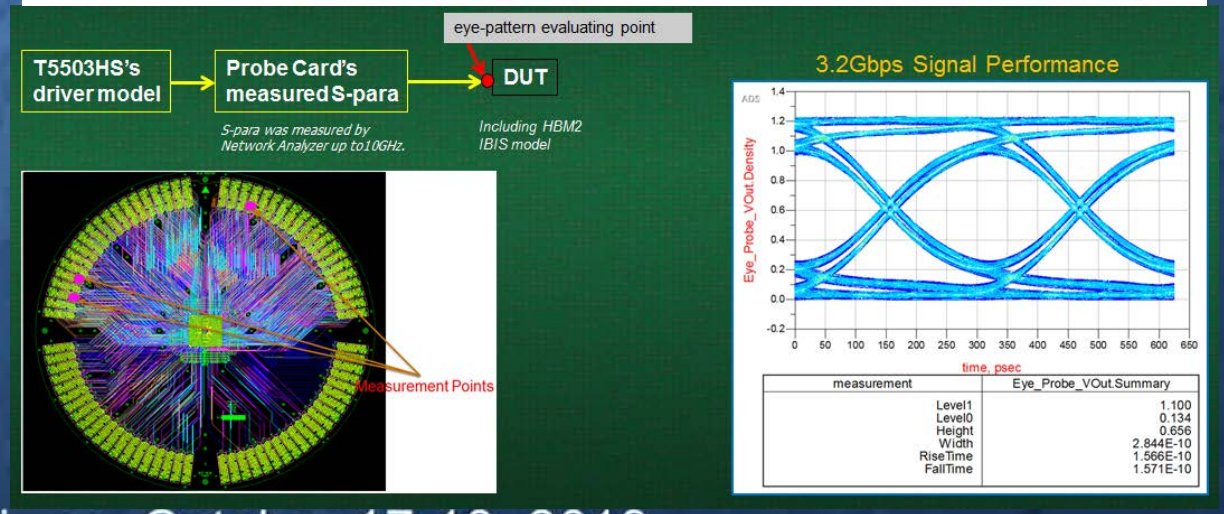




COMPASS 10

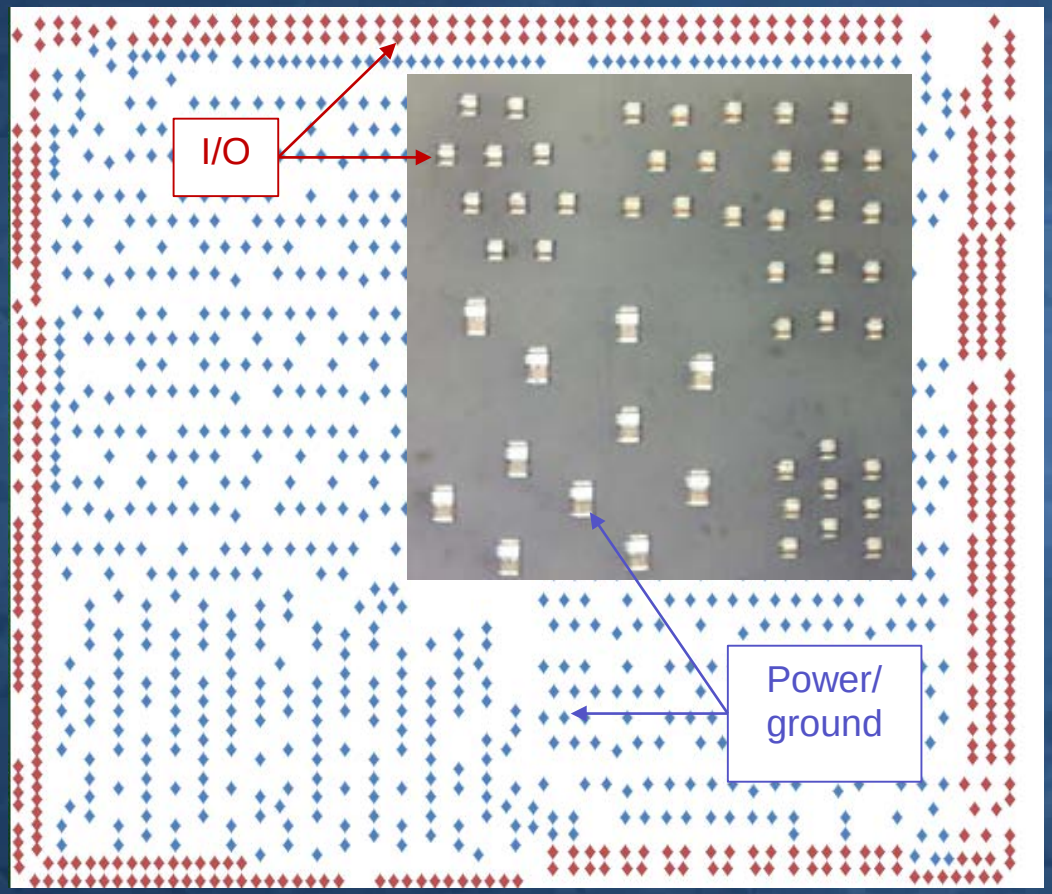
Condition	T.T:600sec 1 time	T.T:600sec 2 times
Scrub depth[um]	2.61	2.99
Scrub diameter[um]	14.81	15.04





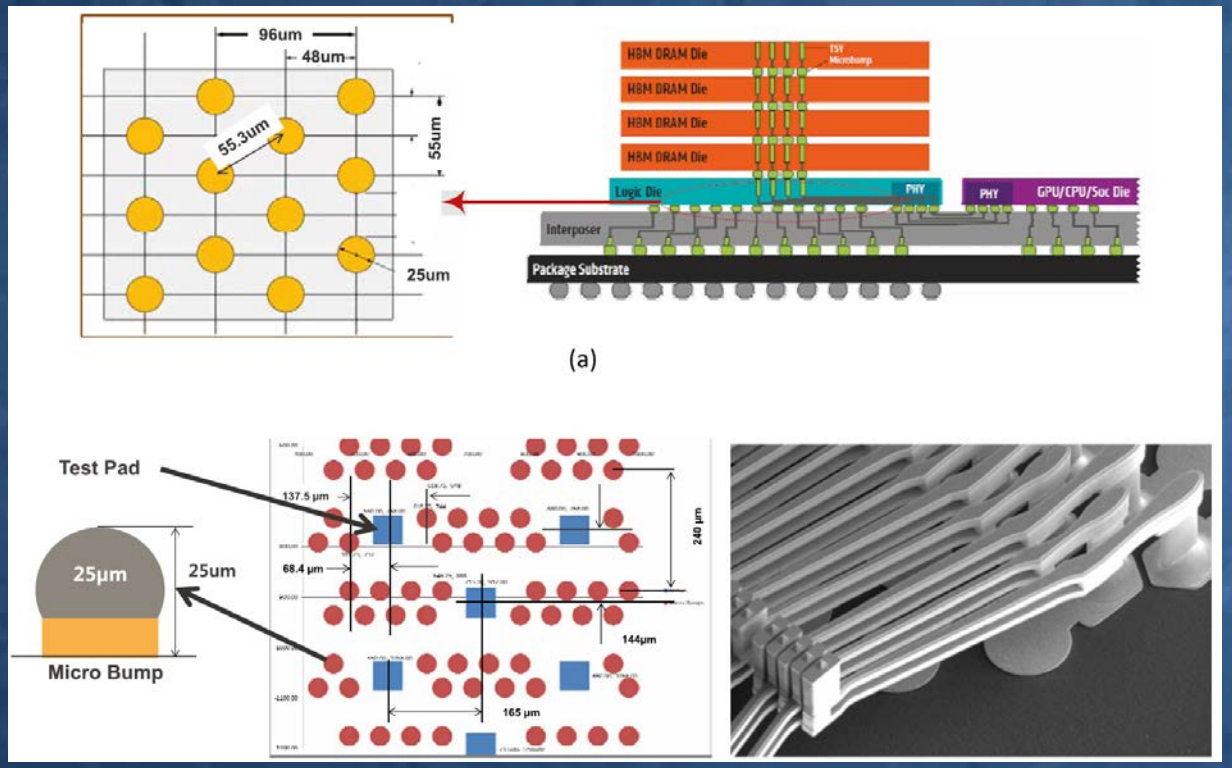
Source: Kiyokawa (Advantest) and Nhin (FormFactor), Compass 2019

Example – In-Die Microbump Optimization



- **Small I/O bumps – small/gentle probes**
  - But smaller I/O probes risk burnout and reduced life for higher-current power/ground connections
- **Higher-current power/ground bumps – larger/stiffer probes**
  - But power/gnd probes risk damaging I/O bumps
- **Rather than compromise, decouple require-ments with a Hybrid MEMS probe card**
  - Composite metal MEMS technology to match force, wear, etc. per probe
  - Much higher uptime (reduced probe burn events)
  - 40% improvement in power impedance
  - Many permutations possible

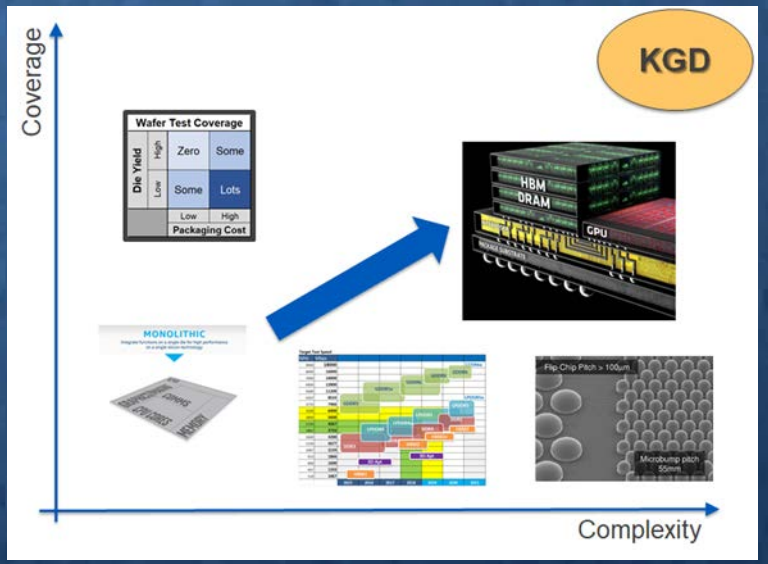
Example – HBM with Test Pads Instead of Microbumps



- **Redundant pads = possible alternative to directly probing microbumps**
- **Advantage:**
  - Doesn't damage microbumps
- **Challenges:**
  - May consume/increase die real estate
  - May constrain test coverage (fewer signal connections)
  - May impact high-speed signal performance (different routing)

Summary and Conclusions

- **Advanced packaging will fill the vacuum left by the end of Moore's Law**
  - Burden shifts from front end (lithography/inspection) to back/middle end (assembly/test)
- **Technical challenges**
  - Microbumps can be probed directly, with sufficiently advanced probe card technology
  - But it's not easy – trends include smaller/denser/non-flat targets, higher frequency signals
- **Economic challenge**
  - Packages are expensive (many steps, component dies)
  - Final test alone provides no info to correct/improve
  - KGD is ideal, but expensive
  - Balance test coverage cost vs. package yield loss cost
  - Test multiple insertion points to optimize test coverage
- **Optimized test program requires data**
- **Solutions available today**



SWTEST ASIA 2019

Methodology of VCSEL Probing and Testing

MPI CORPORATION

Hector Lin
Product Development Manager

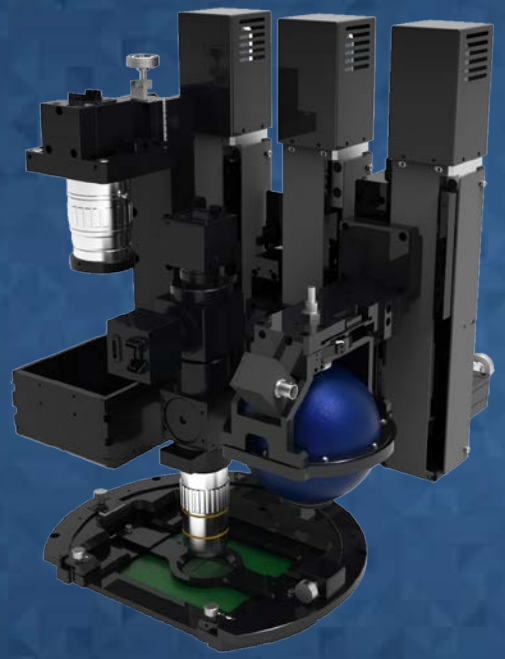
Hsinchu, Taiwan, October 17-18, 2019

Overview

- VCSEL Product and Measurement Requirements
- Probing System Status
- Measurement Performance
- Challenges of VCSEL Testing
- Summary

VCSEL Product with Measurement

- **Vertical type**



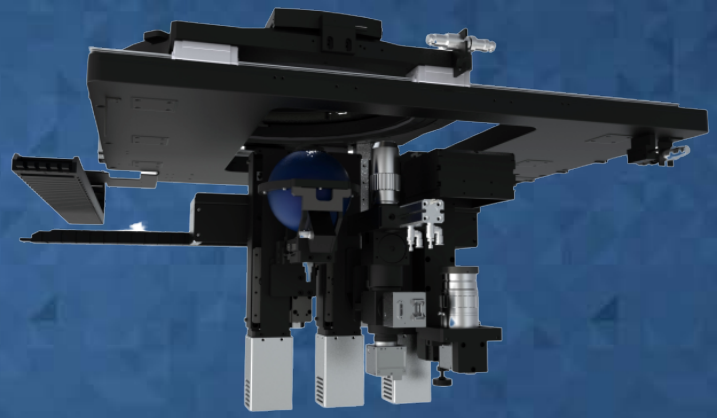
Measurement Unit on Top

1. LIV Measurement with Sphere
2. Far Field Measurement with optics
3. Near Field Measurement with optics

Design Factor

1. Measurement distance is limited by probe
2. Measurement circuit with chuck
3. Temperature controlling by thermal chuck

- **Flip Chip Type**



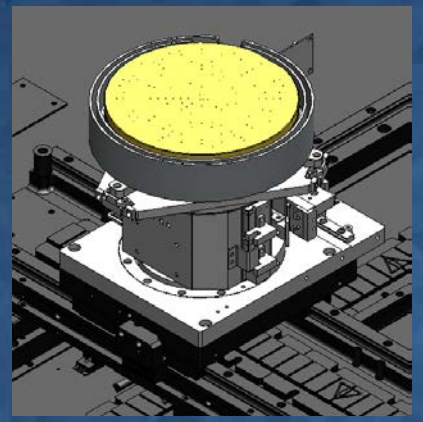
Measurement Unit on Bottom

1. LIV Measurement with Sphere
2. Far Field Measurement with optics
3. Near Field Measurement with optics

Design Factor

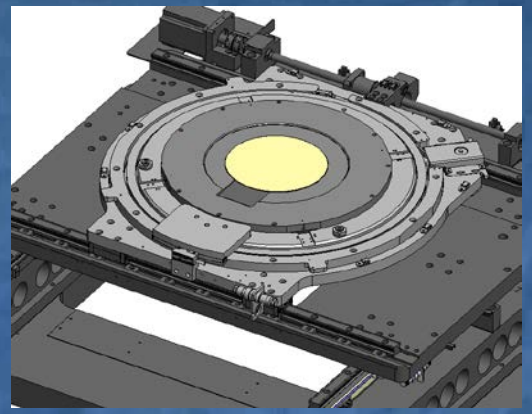
1. Measurement distance is limited by probe
2. Measurement circuit with chuck
3. Temperature controlling by thermal chuck

Probing System Status



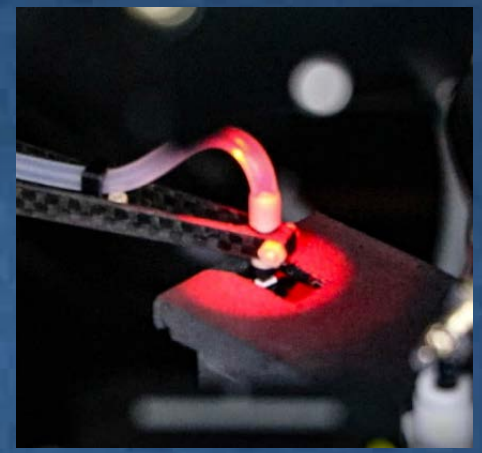
Top Probing Structure

Prober Structure
1. Wafer support with chuck
2. Support vertical wafer and board
3. Probing on top side



Bottom Probing Structure

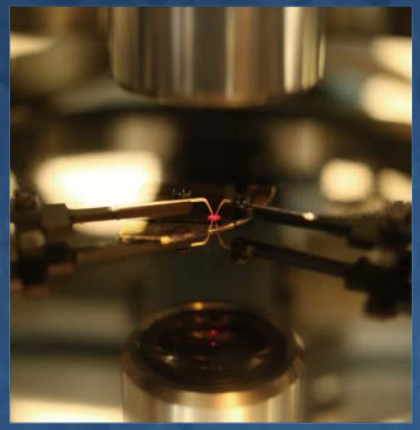
Prober Structure
1. Wafer support with special chuck
2. Support flip chip type wafer
3. Probing on top side



Single Device
Probing Structure

Prober Structure
1. Support device from die to package
2. Device holding with vacuum
3. Probing on top side / bottom size

Top Probing System Status



Measurement Structure

Prober Configuration

1. System as open for ambient to 200 degree
2. System as enclosed for -40 to 200 degree
3. System with positioners / probe cards
4. Chuck for thin wafer / carrier holding
5. Optical measurement : LIV / NF / FF

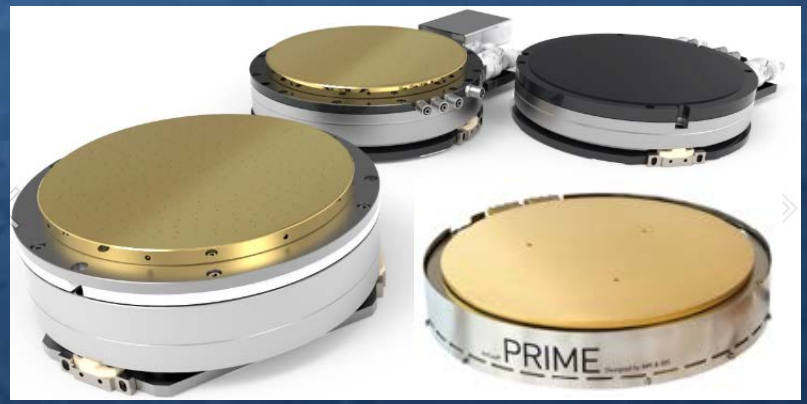
Application note

1. Prober type confirmation
2. Probe style based on device layout
3. Chuck with temperature and electrical character
4. Optical measurement
5. Automation methods

Light Shielded Environment

Probe Type

Automation



Chuck Selection

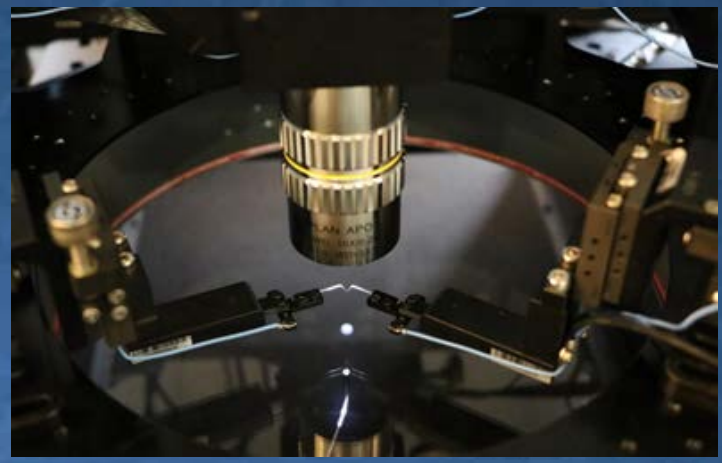
Bottom Probing System Developing

Prober Configuration

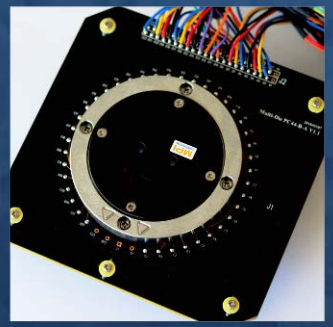
1. System as open for ambient testing
2. System with positioners / probe cards
3. Chuck for thin wafer / carrier holding

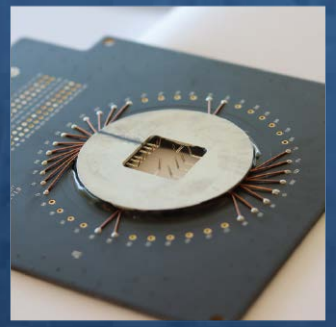
Application Note

1. Probe style based on device layout
2. Chuck selection
3. Optical measurement
4. Automation methods



Measurement Structures

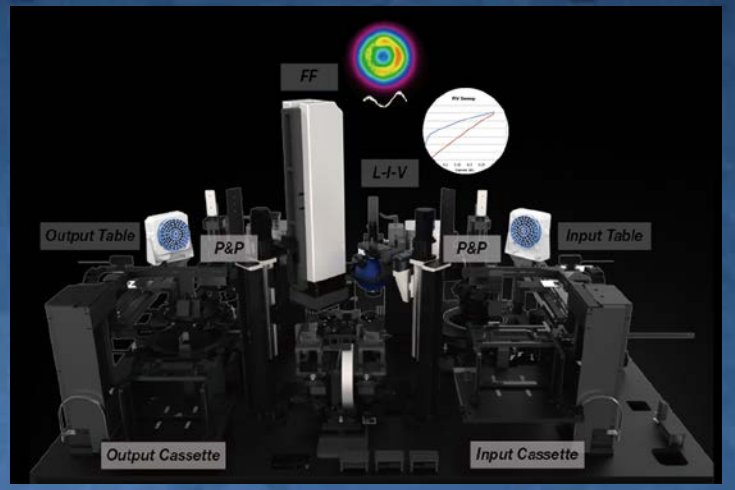




Probe Type

Single Device System Status

High Efficiency P&P Probing



Measurement Structure

Prober Configuration

1. Testing with turret chuck
2. Input frame area and output frame area
3. Chuck with temperature controlling
4. Max with dual testing structure

Application note

1. Device dimension and P&P method
2. Device pad layout and condition
3. Probe type and structure
4. Optical measurement : LIV / NF / FF
5. Automation and production flow

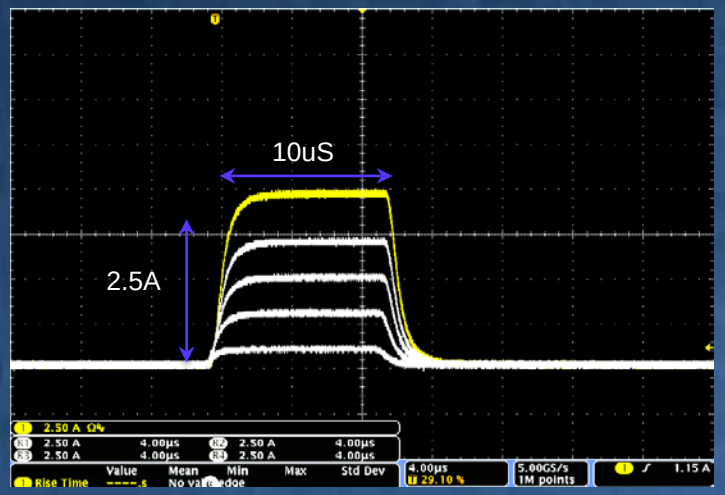
Bottom Emitting Device Testing

Edge Emitting Device Testing

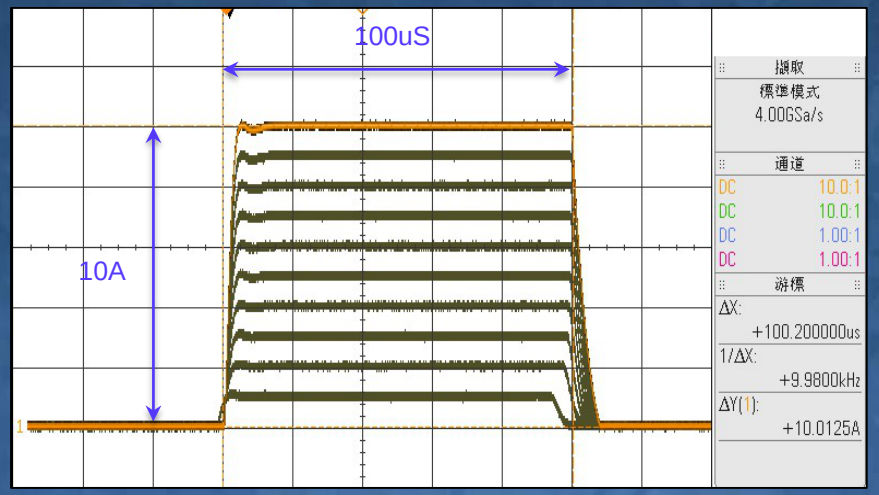
Measurement Performance

- **Electrical Testing Performance**
  - Response performance
  - Probe mark and applying current
- **Spectrum Measurement Performance**
  - Spectrum from spectrum meter and OSA
- **Beam Quality Measurement Performance**
  - NF Measurement Structure
  - FF Measurement Structure

Electrical Testing Performance



2.5A 10uS pulse shape



2.5A 100uS pulse shape

Application Factor
- Device Character
- Device Resistor
- Power and current range
- Device response time
- Leakage level

System Environment
- Probe type
- Cabling methods
- System shield method

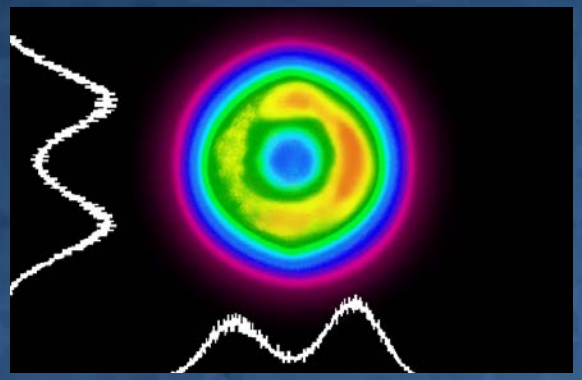
Multi – Instrument Structure
1. Current pulse:
   up to 10 A at 10 uS pulse width
2. Current and voltage measure with
   1MS/sec digitizers

Multi – Instrument Structure
1. High power source combination
   100us pulse shape
2. Current to be extend to higher level
3. Low current region accuracy
4. Flexible structure to extend other measurement

Max Current	Pulse Width			
	1us	10us	100ms	Over 300ms
5A	△	△	◎	◎
10A	△	△	◎	◎
20A	△	△	□	□
Over 20A	△	△	□	□

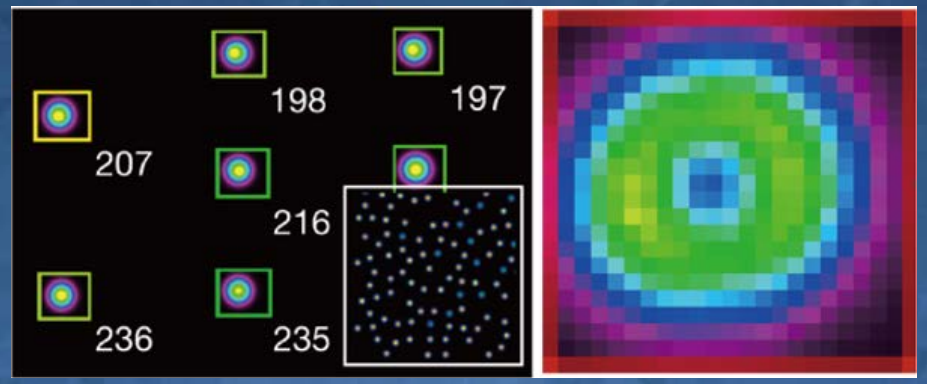
◎ Ready
□ Ready but application-dependent
△ Under development

Beam Quality Measurement Performance



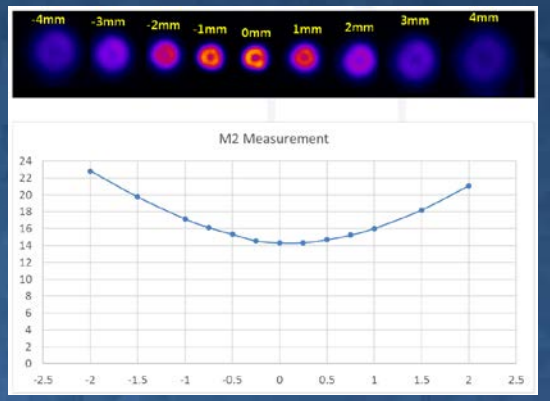
Far Field Measurement

Application Note
1. Current pulse:
   up to 10 A at 10 uS pulse width
2. Current and voltage measure with
   1MS/sec digitizers



Near Field Measurement

Application Note
1. High power source combination
   100us pulse shape
2. Current to be extend to higher level
3. Low current region accuracy
4. Flexible structure to extend other measurement



M2 Measurement

Application Note
1. Current pulse:
   up to 10 A at 10 uS pulse width
2. Current and voltage measure with
   1MS/sec digitizers

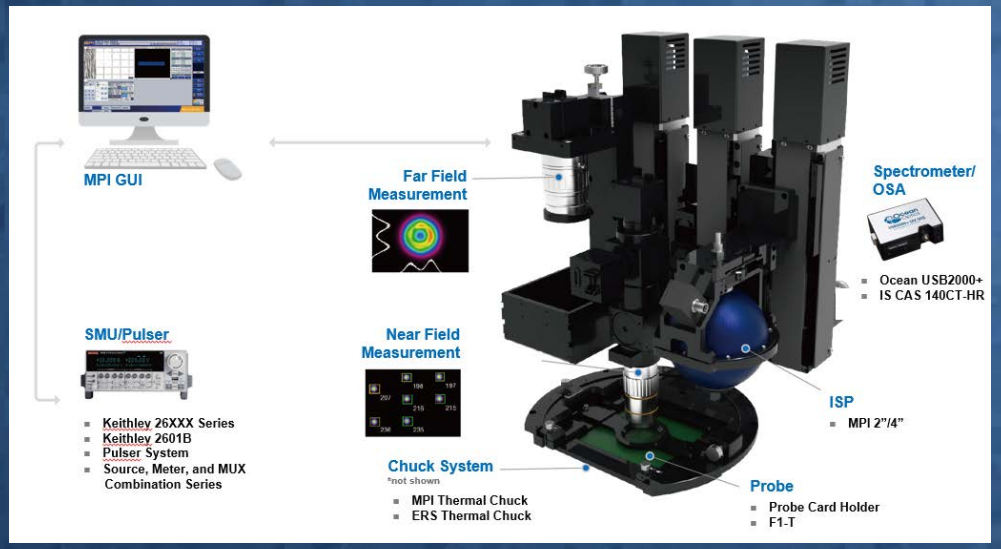
Challenge for VCSEL Prober

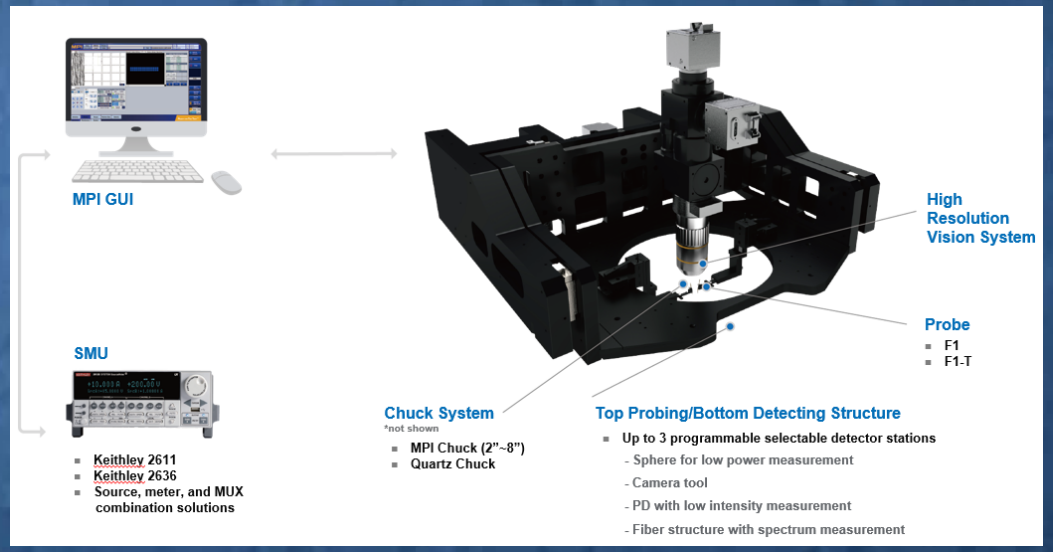
Top Probing System

1. Reduce the influence of circuit impendence
2. Temperature controlling (-60 degree to 200 degree)
3. Process for flexible VCSEL layout
4. System automation

Bottom Probing System

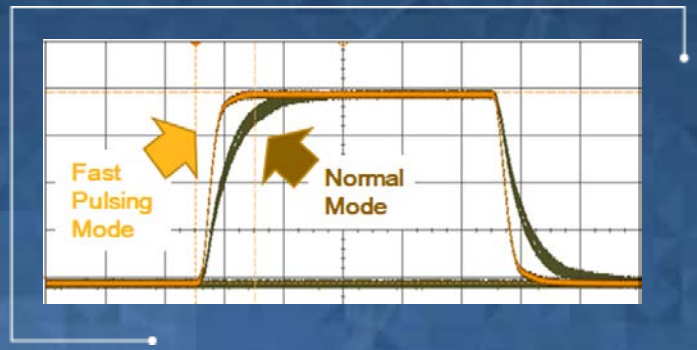
1. Reduce the influence of circuit impendence
2. Temperature controlling method
3. Contacting controlling
4. Process for flexible VCSEL layout
5. System automation



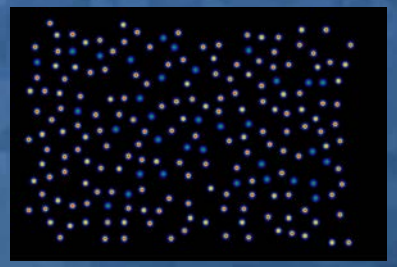


Challenge of VCSEL Testing

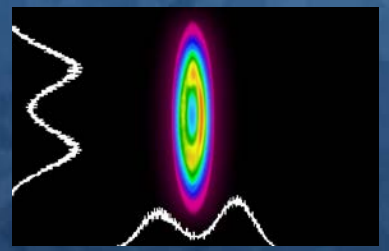
LIV Testing
1. Optimization of source capability
   - nS level to mS level
2. Optimization of digitizer for measurement
3. Optimization with probe / circuit
4. Spectrum resolution and dynamic range

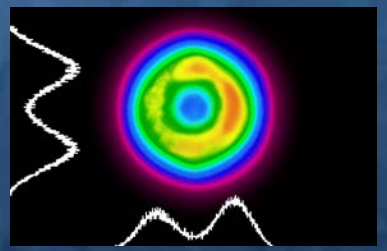


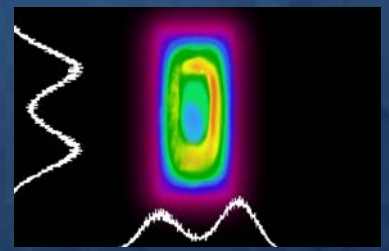
Near Field Measurement
1. Divergence angle range
2. Lager VCSEL sensor
3. Lager Power range
4. Smaller emitter size and pitch



Far Field Measurement
1. Definition of measurement position
2. Limitation of optics and diffuser
3. VCSEL module Far Field Testing







Summary

To Provide Optimized Optical / Electrical Testing Solution For Photonics Applications

mpi-corporation.com

SWTEST ASIA 2019

Probing Technology Challenge Now & Future

力成集團 PTI GROUP

Clark Liu
Henry Tseng
Jason Sung
PTI Taiwan

Hsinchu, Taiwan, October 17-18, 2019

It was the best of times,
it was the worst of times…

Charles Dickens

Overview


Background
Technology
Challenge
Conclusion
Acknowledgement

PTI Group Testing Service in Asia

力成集團 PTI GROUP

PTI

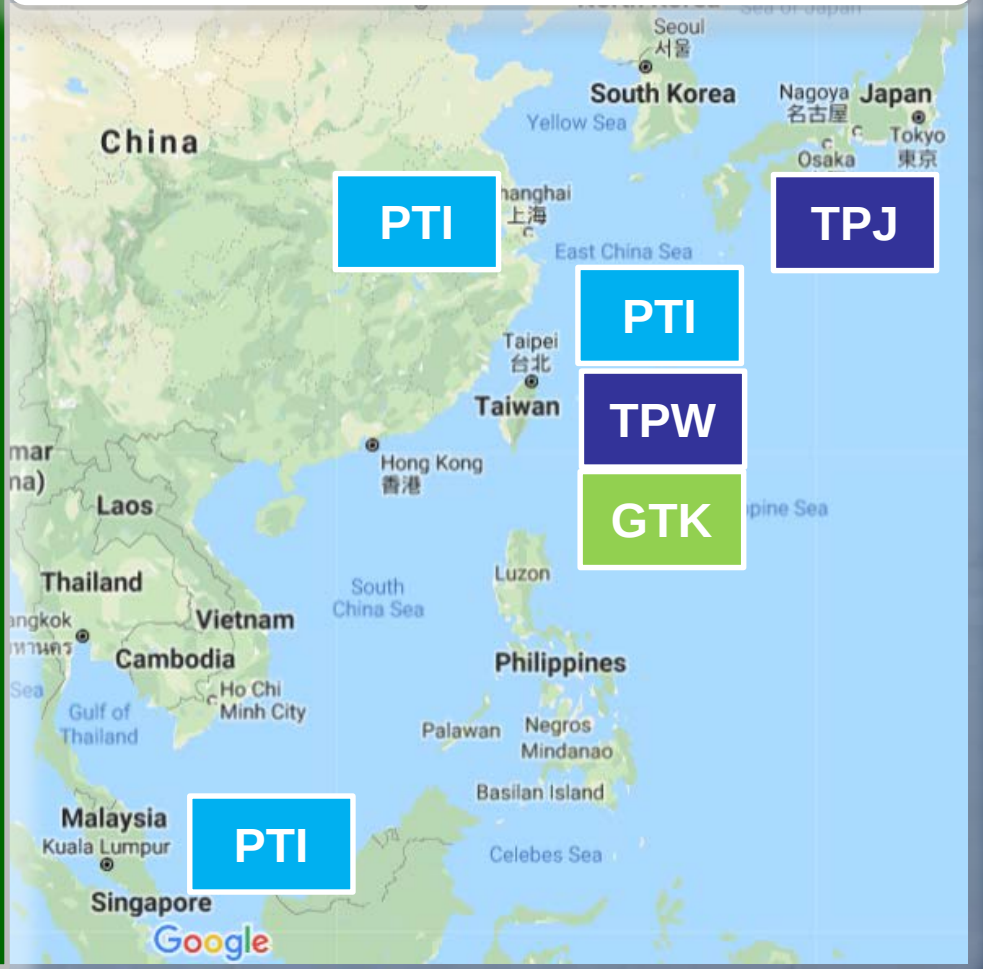
GTK

TPW
TPJ

PTI Group >1000 Probers Install Base

PTI	GTK	TPW / TPJ
CP : Memory +SOC FT : Memory +SOC Advance Package Test	CP/FT: SOC	CP: Memory +SOC FT: SOC

Site Location



Probing Technology Challenge

(1) Probe Technology

(2) Prober Technology

(3) Inspection Technology

(4) Cleaning Technology

(5) New Application

(1) Probe Technology Challenge

How to Support NPI ?

?

Process	Device	Pitch	Contact	ATE
• 7nm • 16nm • 28nm • 40nm	• DRAM • Flash • SOC	• 40um • 60um • 80um • 100um	• Al Pad • CPB • WLCSP	• 93K • Flex • T5503



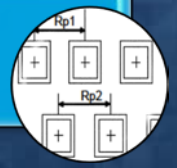


Enough Information ?

No! Probing Engineer keep challenge by internal / customer !!!

- Array
- LOC
- Stagger
- Corner

Probe Layout



- MEMS
- Cantilever
- Vertical
- Pogo

Probe Type

- Digital
- RF
- Analog
- CIS

Test Application

- Al Pad
- CPB
- WLCSP
- RDL

Probe Material

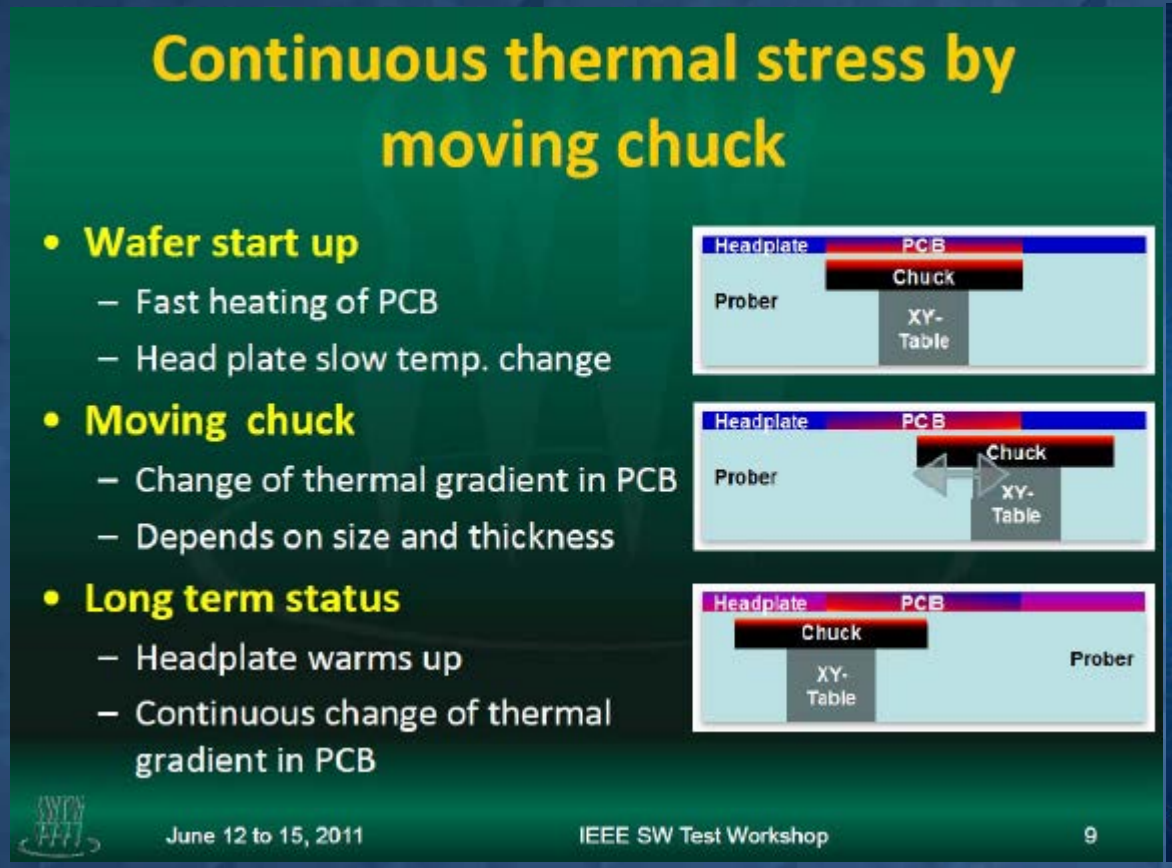
- Dual Temp
- CCC / MAC
- CR Issue
- Customized

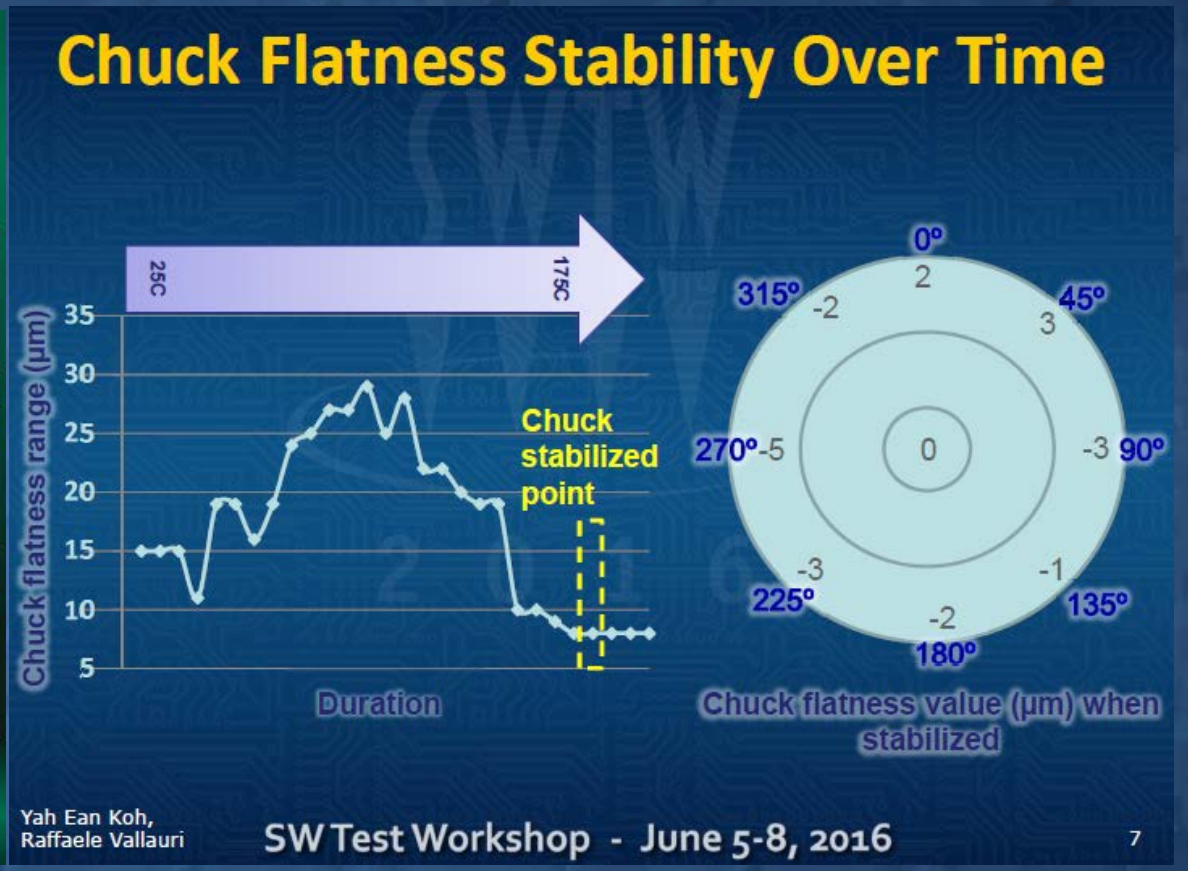
Test Request

Because New Probe Development Still Challenge:

- Precision / Repetitive
- Multi-Materials / Multi- Type Probes
- Maximum Allowable Current
- Wide Range Working Temperature
- Reasonable Wear Rate
- Maintainability
- New Process and Application Support
- Overall Cost Concern

(2) Prober Challenge _ Chuck Requirement



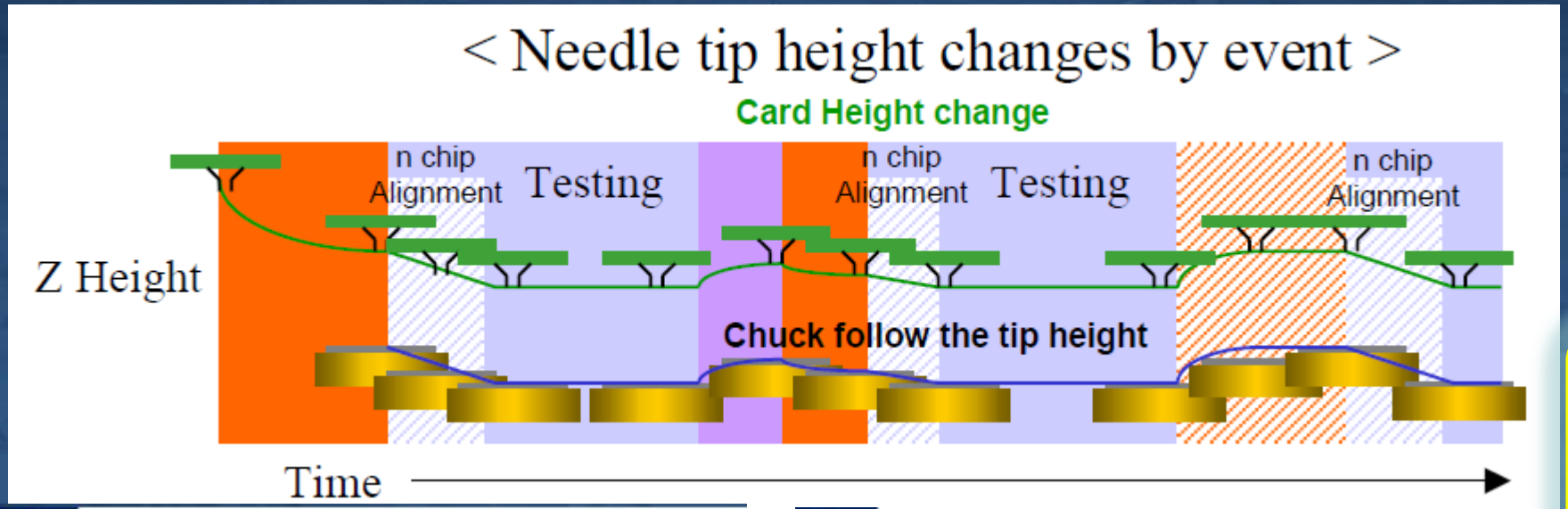


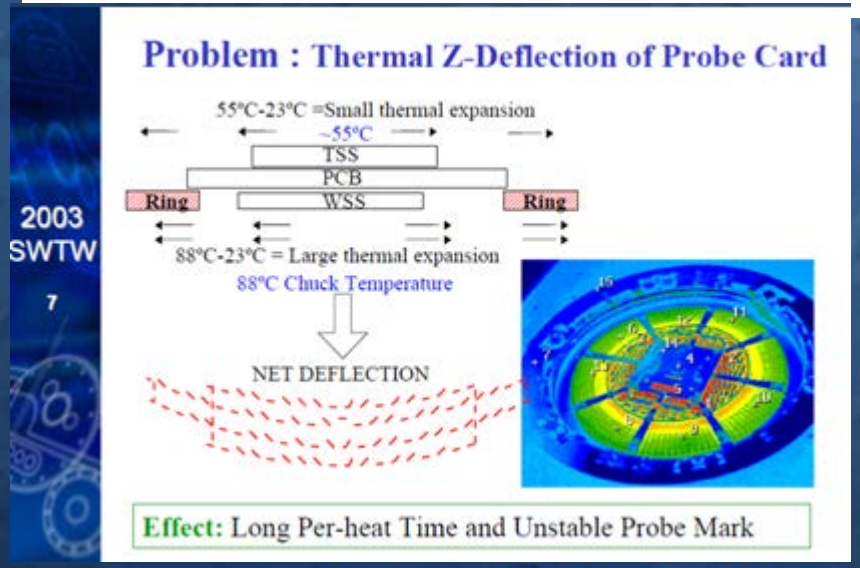
Ref.: S07_02_Bleyl_Martens_SWTW2011

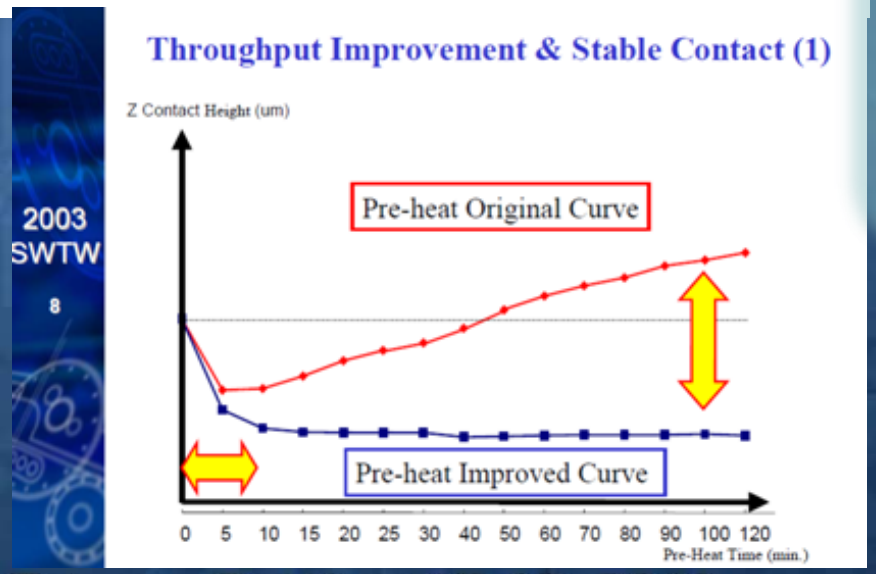
Ref.: GF_W.L.S_SWTW2016

Chuck Heat Dissipation / Precision Management

Chuck Dynamic Change as Soaking Impact

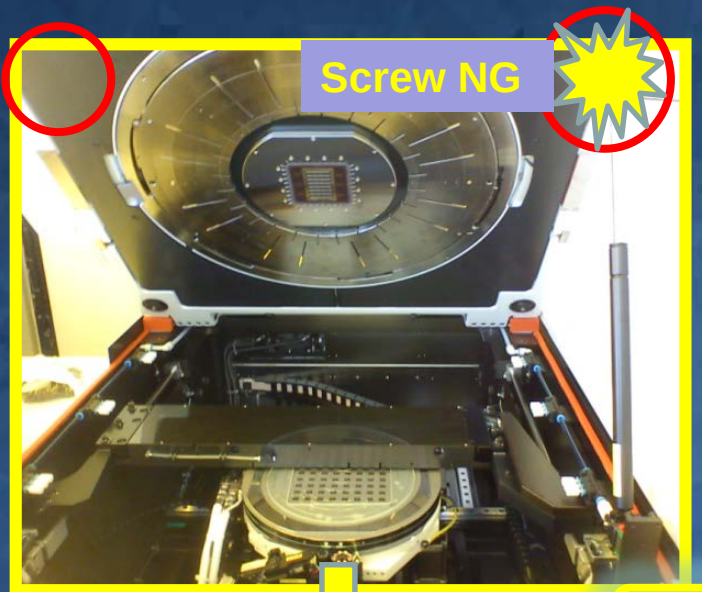


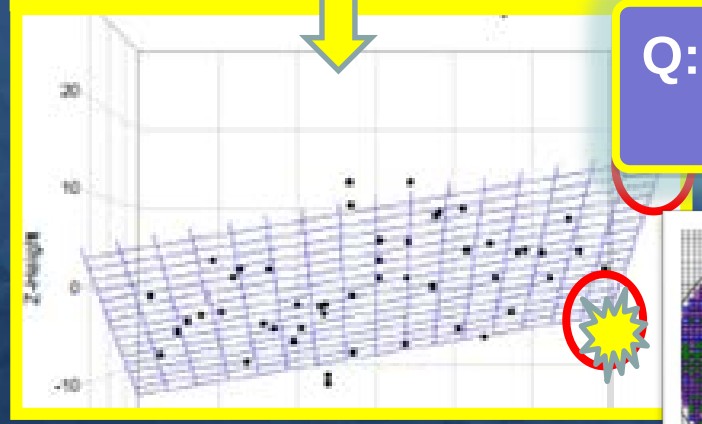




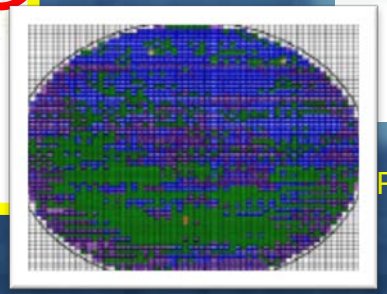
Q: More Data and Information get from Prober?

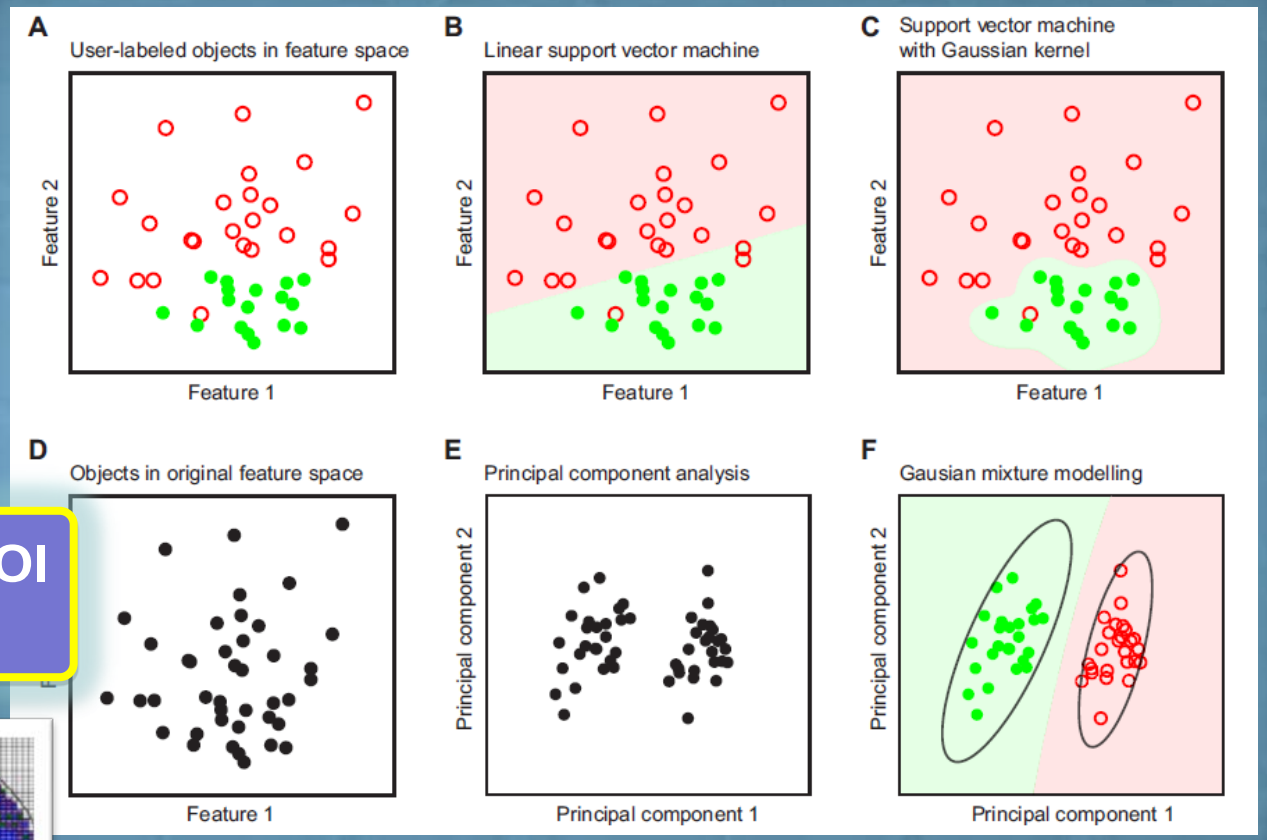
Machine Learning in Probe Mark Analysis





Q: Prober / AOI / PMI?





Ref:2013_Machine learning in cell – teaching computers to recognize phenotypes

Deep Learning

2003 SWTW 16

Summary (2)

Future Challenge:

1) Device / Pad / Pitch Shrink

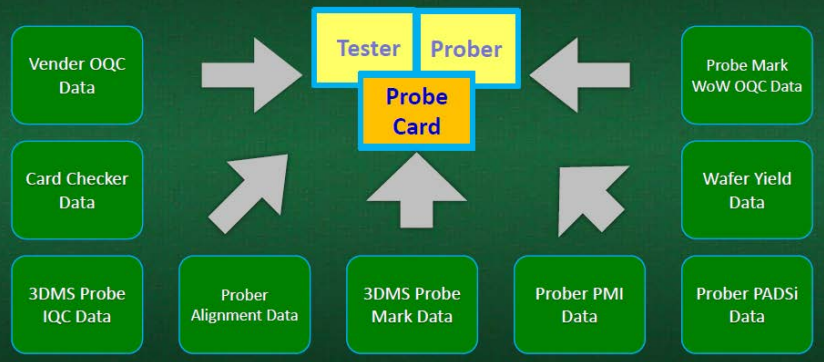
2) More Accuracy Contact

3) New Material Development

4) Cleaning Technology

5) High Speed or High Parallelism Testing

Future Work: Many Data Streams for Big Data



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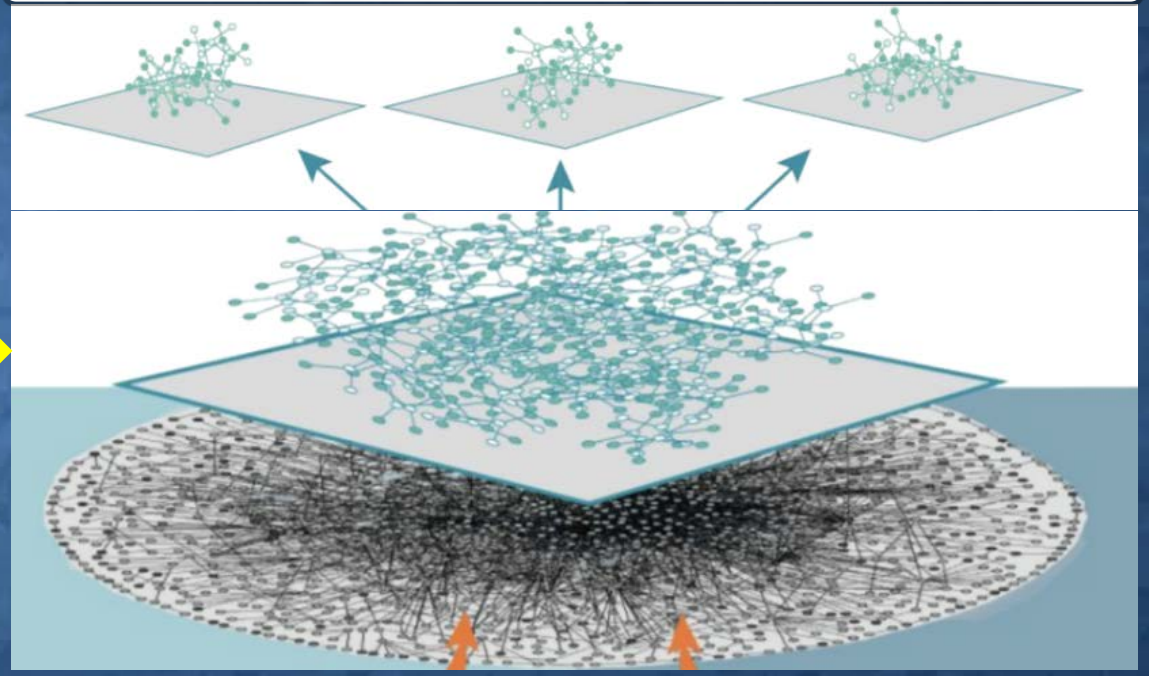
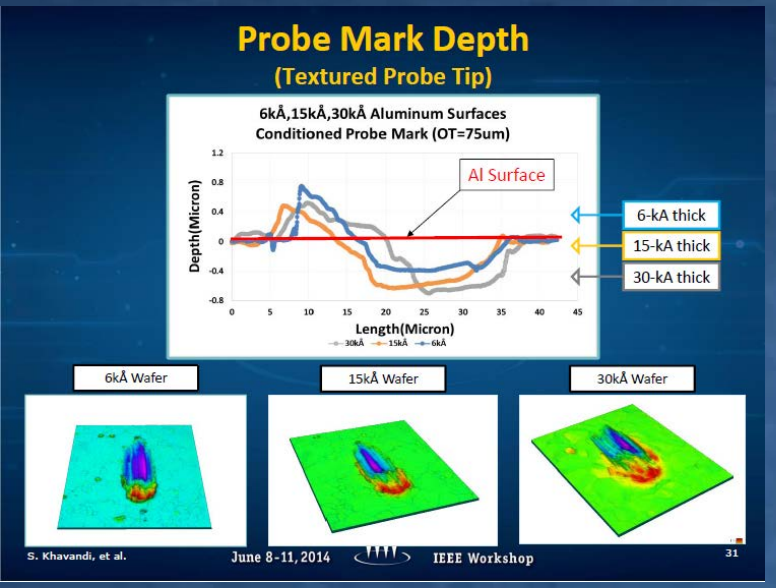
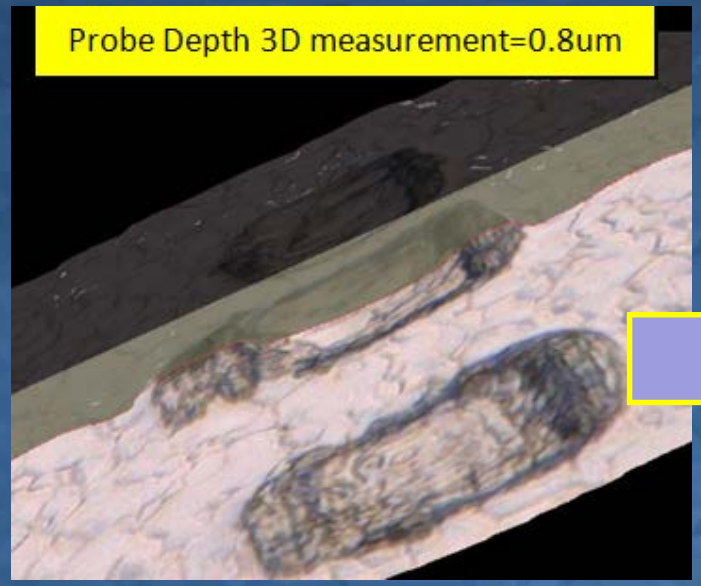
Test Data / Wafer Mapping

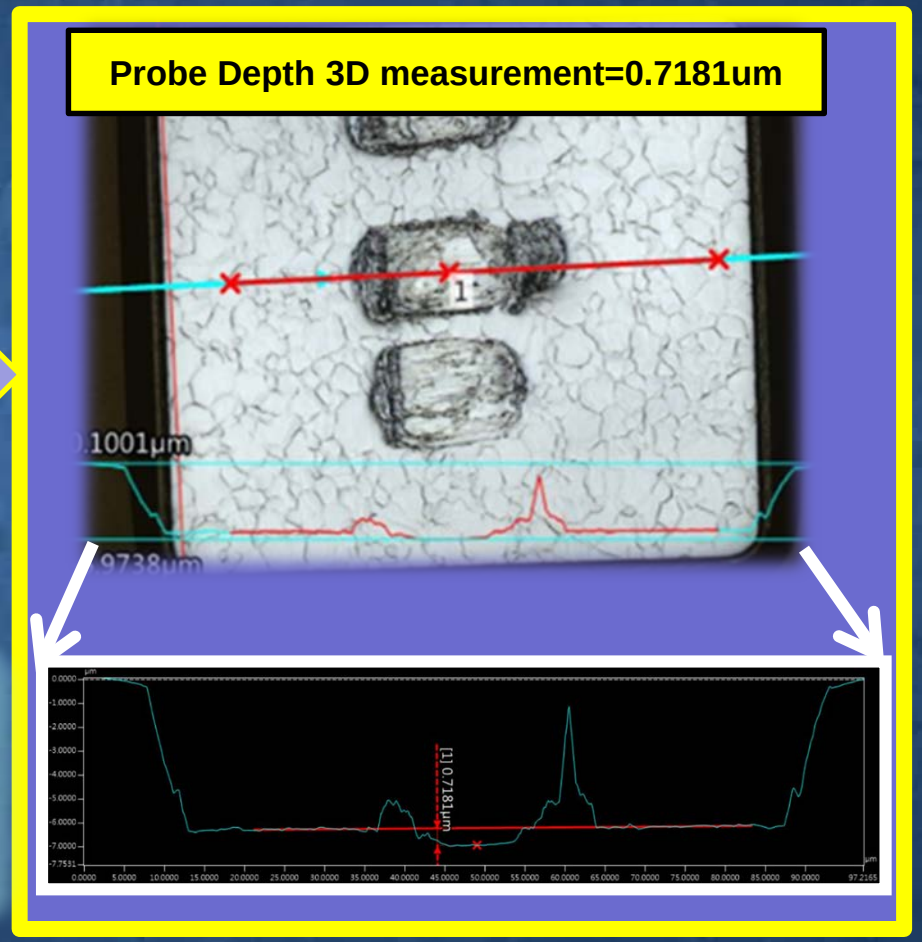


Ref:2018_Deep Learning for the Masses (… and The Semantic Layer)

(3) Inspection Technology Challenge





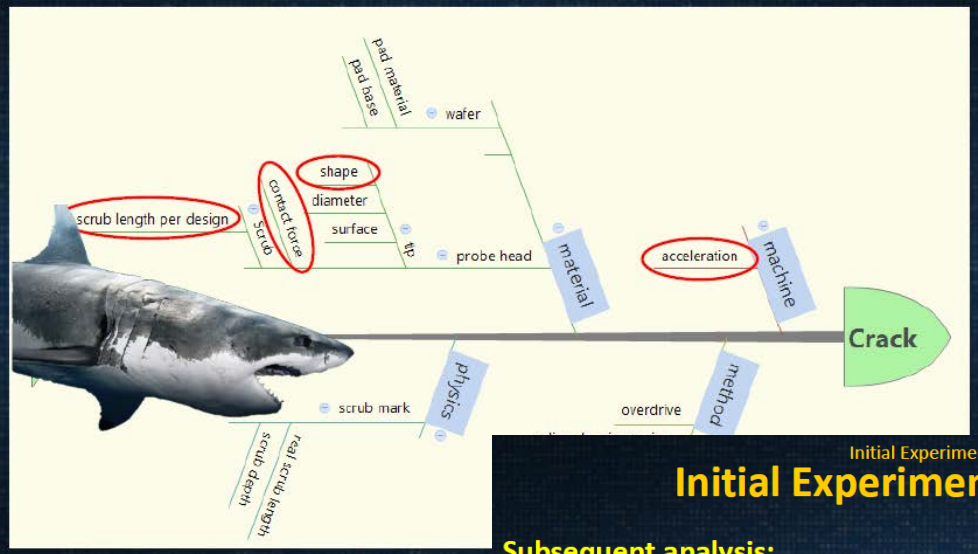


- Exist Resolution is 0.1um
- New Technology is 0.001um

Key: Pad DFM and Probing Parameters Control

Main experiment – digging for the root causes

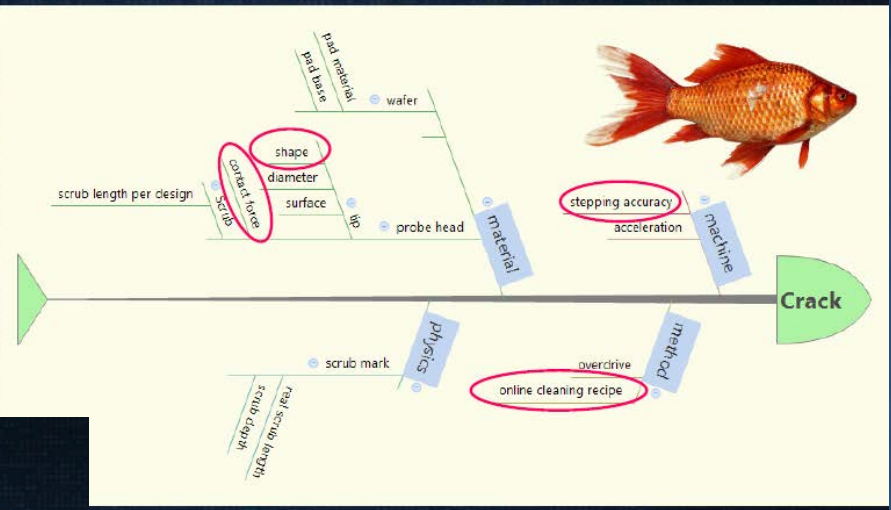
What are the Main Factors to Cause Pad Cracks?



- **Most important factors**
  - tip condition: shape, contamination
  - contact force
  - step accuracy
- **Finally, all factors on this diagram are still in the game.**

Summary

Top Factors to Pad Cracks



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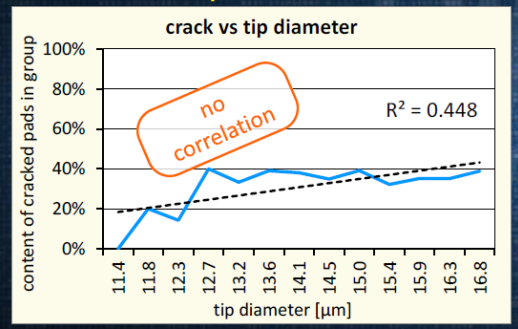
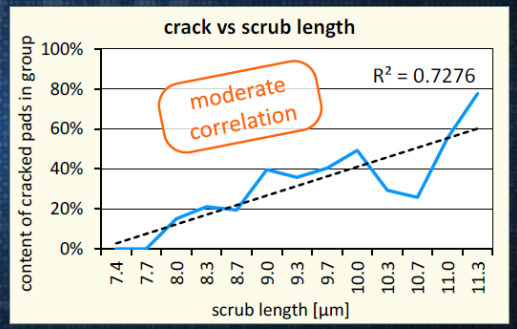
Initial Experiment – first qualification run

Initial Experiment on the Probe Floor

Subsequent analysis:
Probe card analyzer data have been correlated to the crack data



No correlation for tip diameters from 11 to 17 µm



Moderate correlation for scrub length from 7 to 11 µm

Twitchell, Boehm

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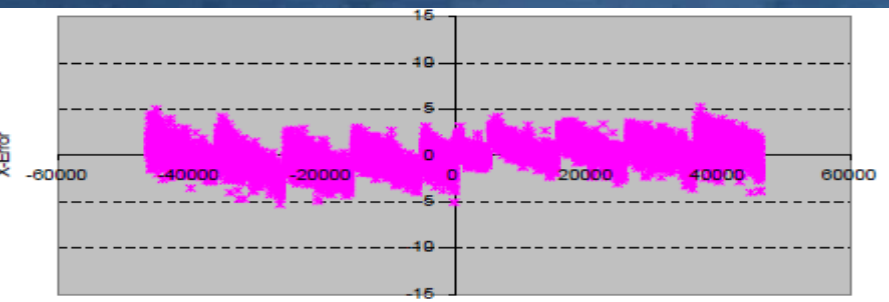
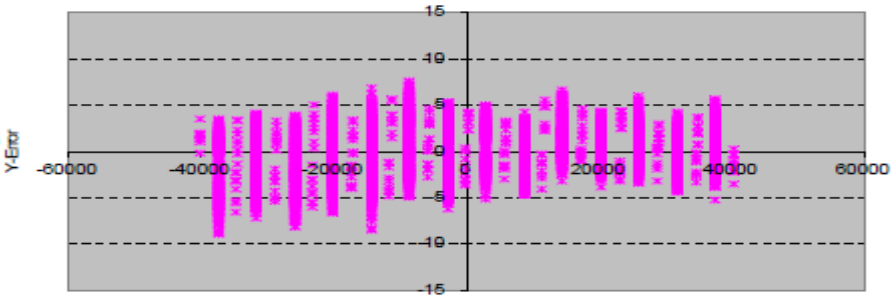
7

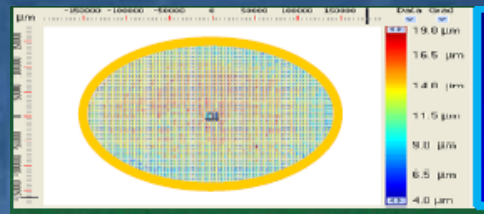
Inspection Equipment Function Integration

X-Error (um)
<+/-5um

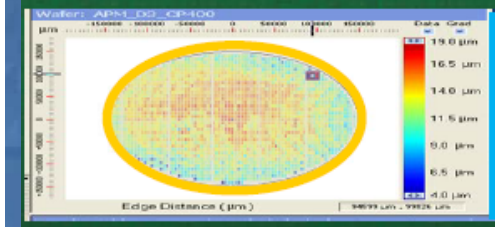


Y-Error (um)
<+/-8um

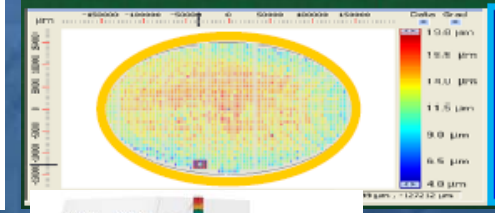




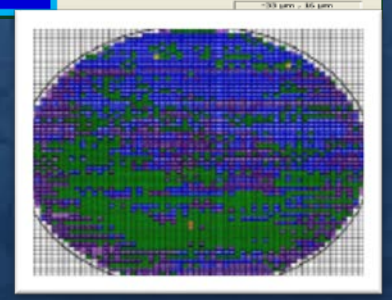
Probe Mark A/A <25%
Production P/M Keep Out
>5um



Production P/M Keep Out
<5um
(Vender only ensure Off
Line Check @RT >5um)



Probe Mark A/A <25%
Production P/M Keep Out
>5um

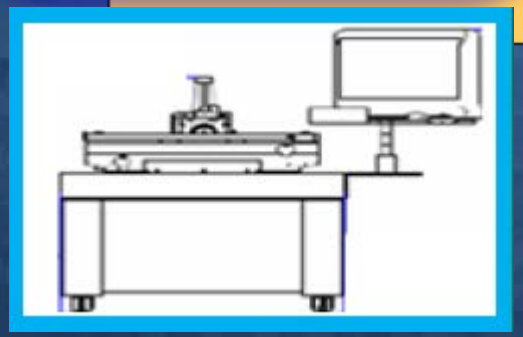


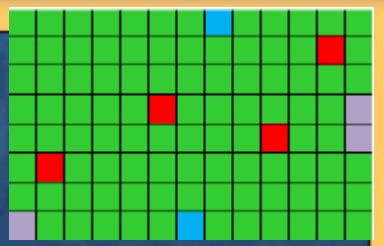
Inspection Tool Development Requirement

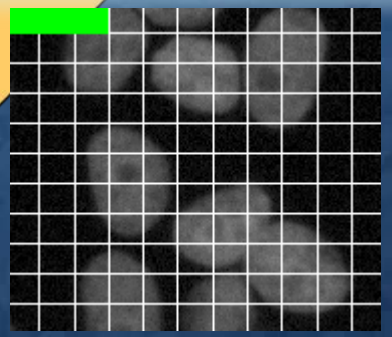
Off Line Measurement

On Line Measurement

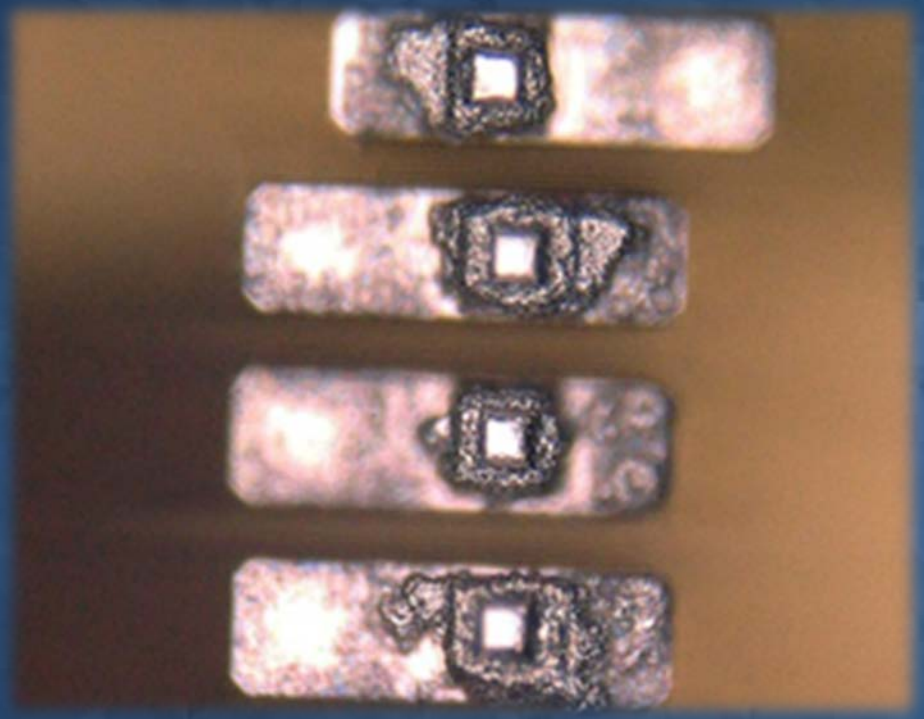
AI & Machine Learning

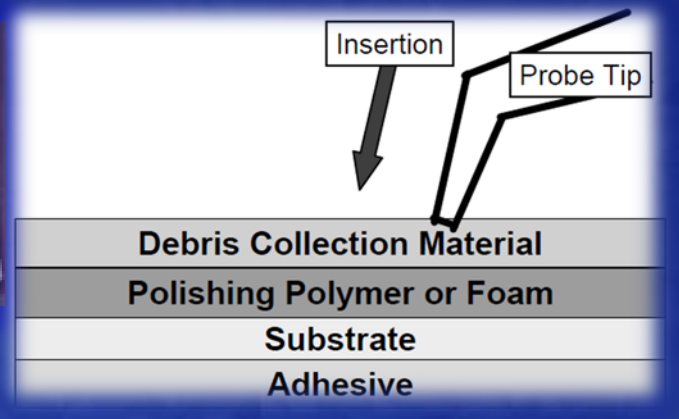


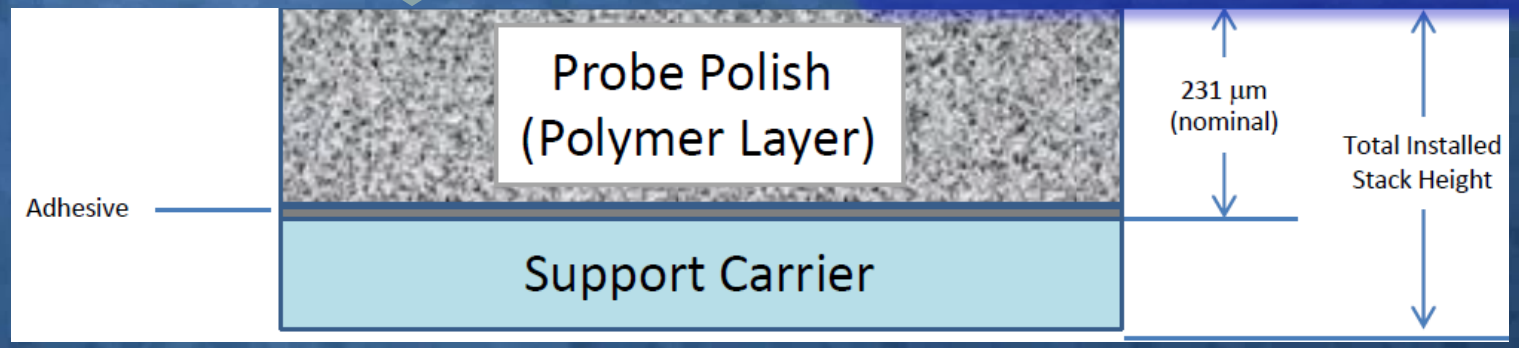




(4) Cleaning Technology Challenge

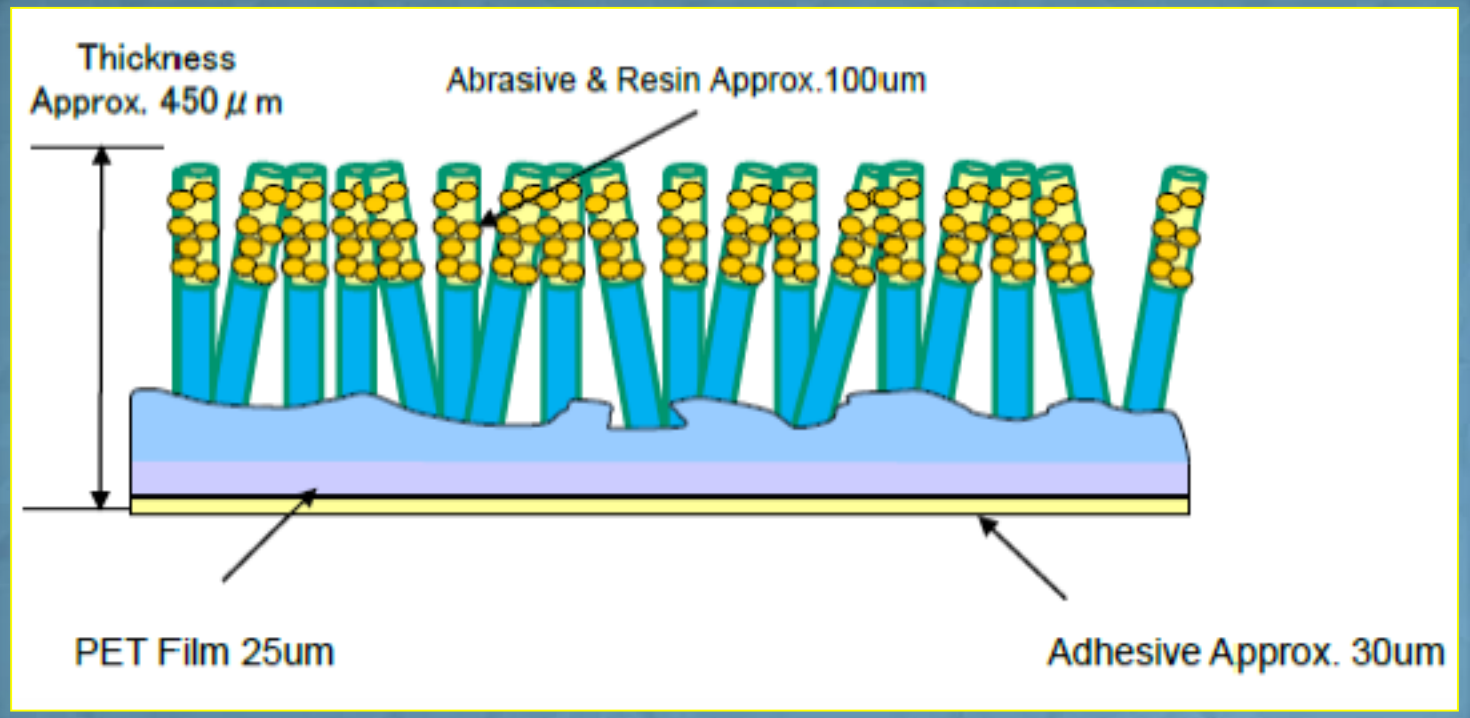


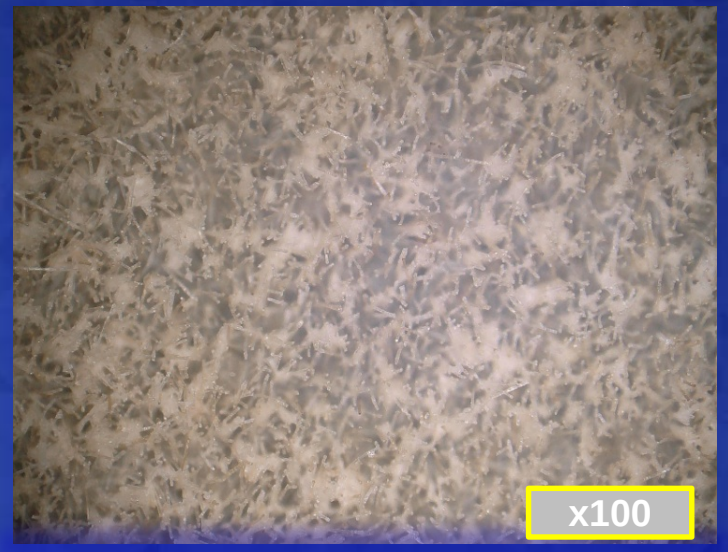




- **Exist Cleaning Material only remove probe tip residue**
- **Worst case need chemical cleaning (Cost / Down-time / EP)**

New Cleaning Material for Auto Clean

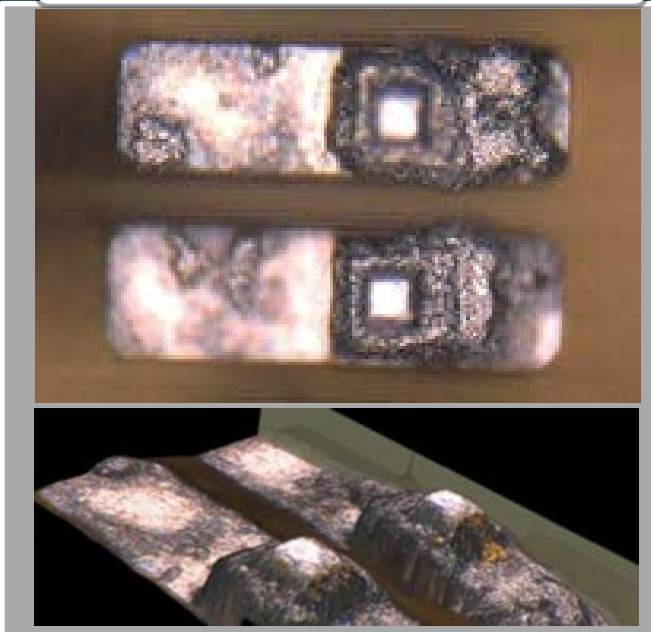




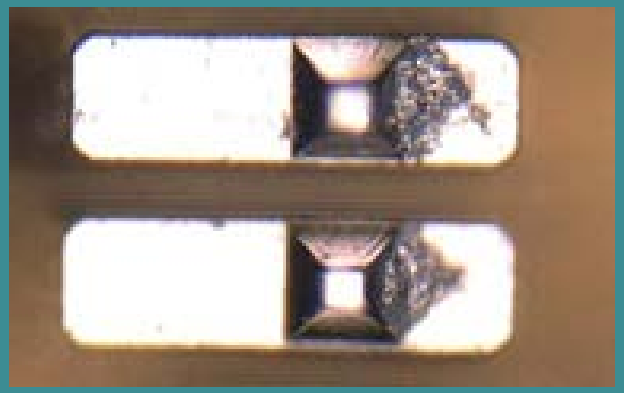
- Exist Technology 0.1um
- New Technology 0.001um

Auto Cleaning in Prober Experiment Result

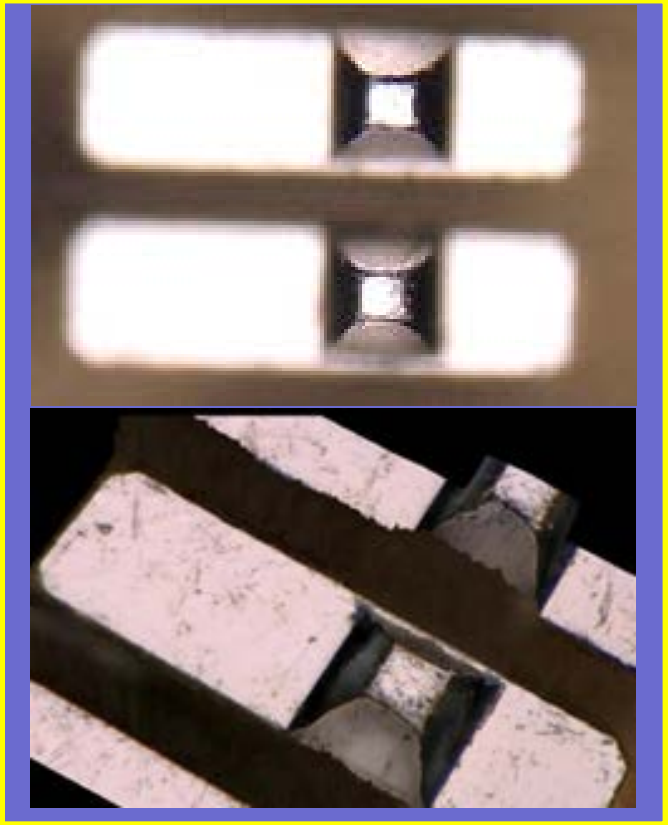
Before Clean



After 1000 TDs



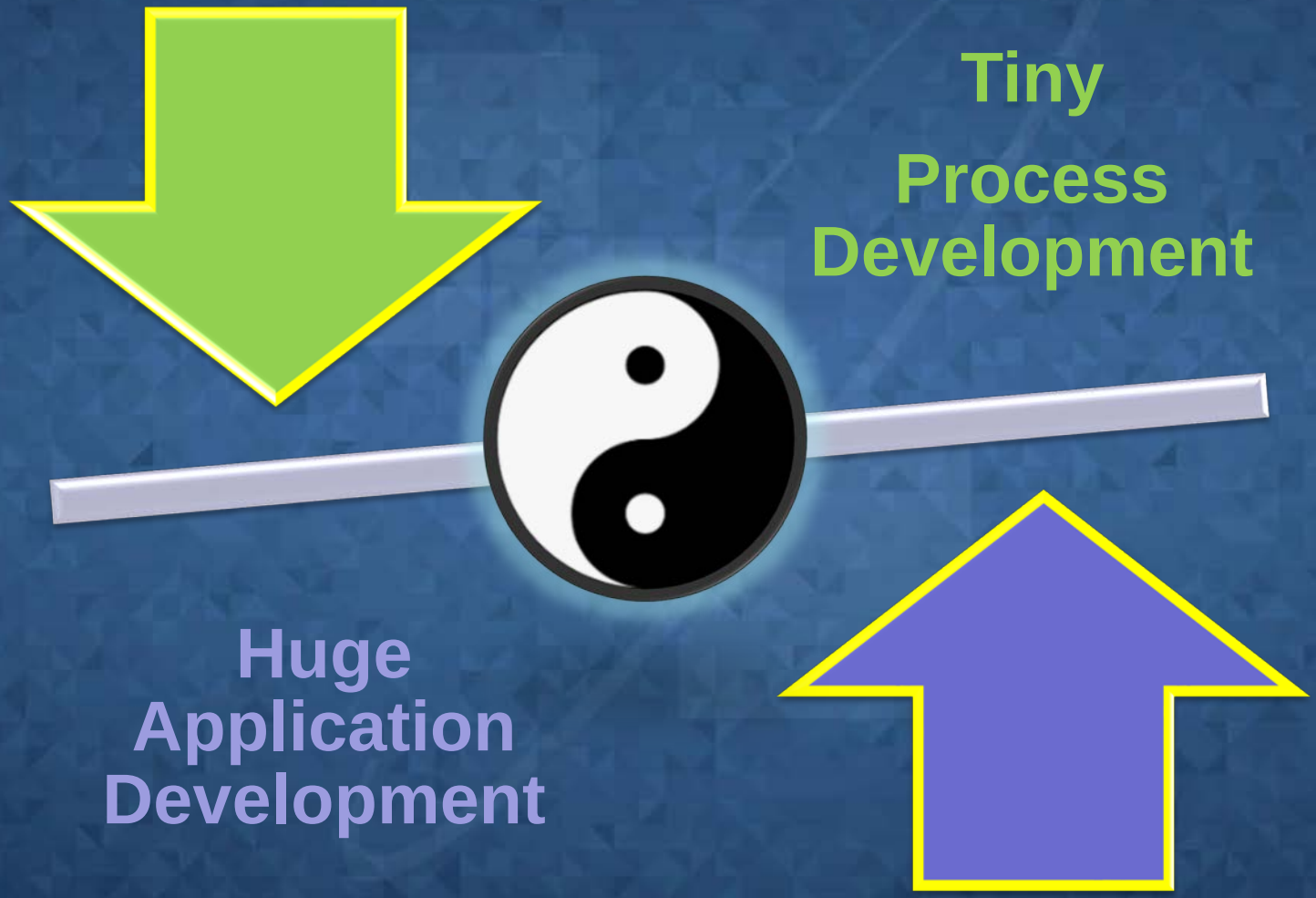
After 2500 TDs



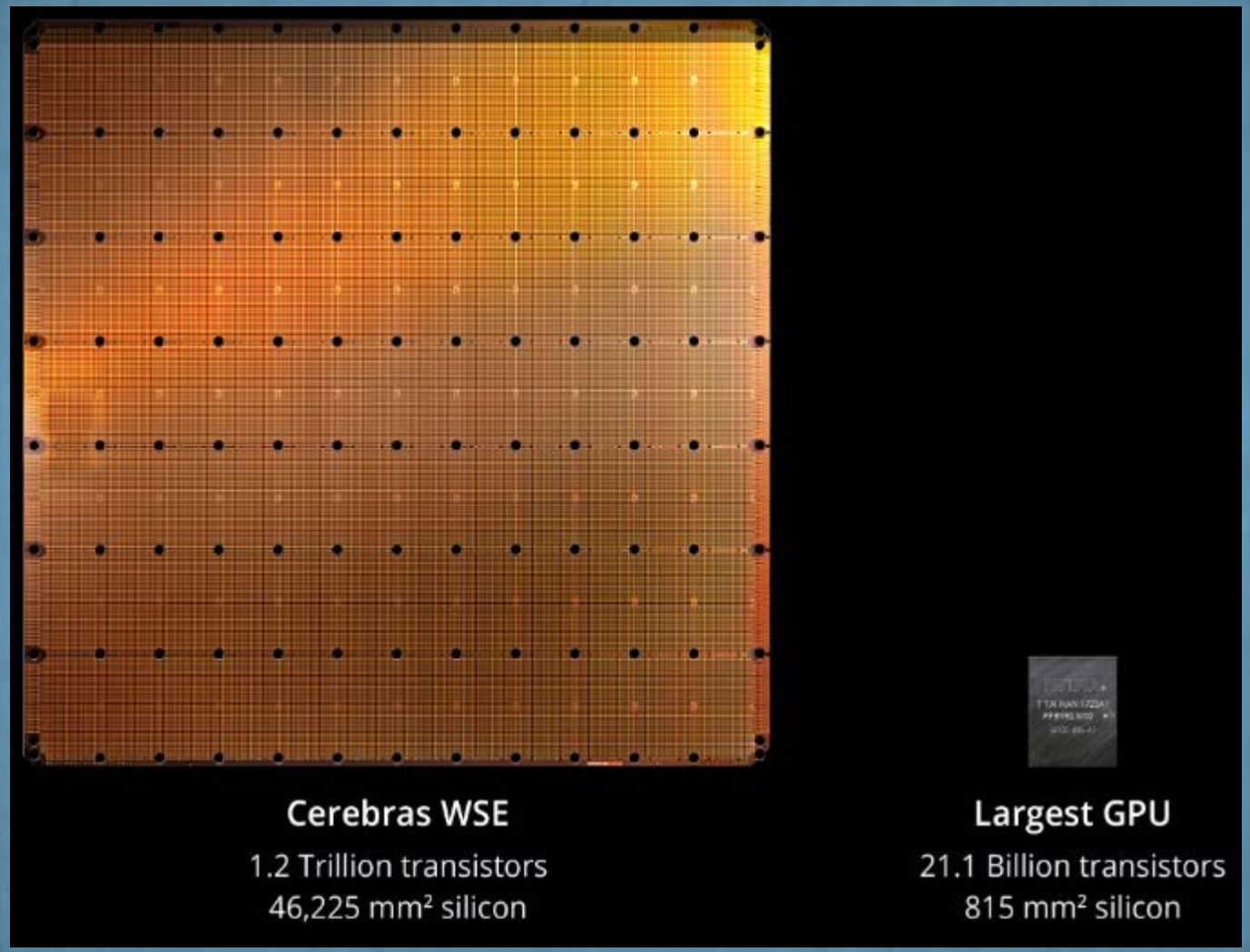
- **Must Keep in Room Temp Cleaning and suggest keep MP OD.**

(5) New Application Challenge

Semiconductor Inflection Point



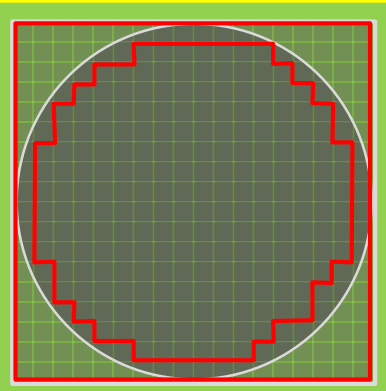
Super Larger Chip



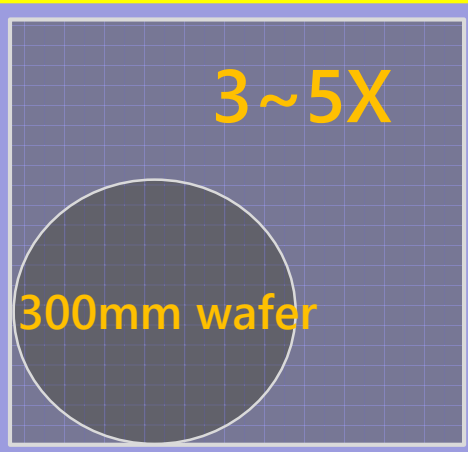
Wafer Scale Engine:
tsmc 300mm Wafer
8.5” x8.5” Diameter
84 Chips Connected
18GB SRAM

https://wccftech.com/meet-cerebras-wse-the-worlds-largest-chip-at-more-than-56-times-the-size-of-an-nvidia-v100/

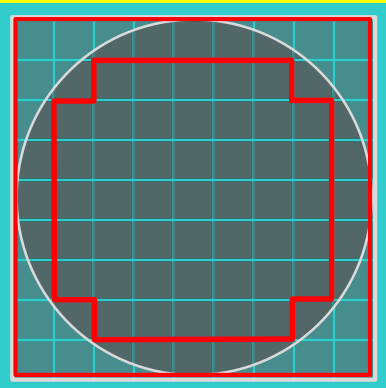
PTI FOPLP in Production



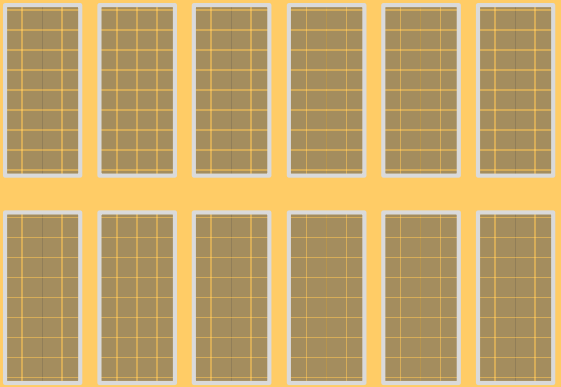
➢ Small package allows higher area efficiency



➢ Larger panel provides better efficiency



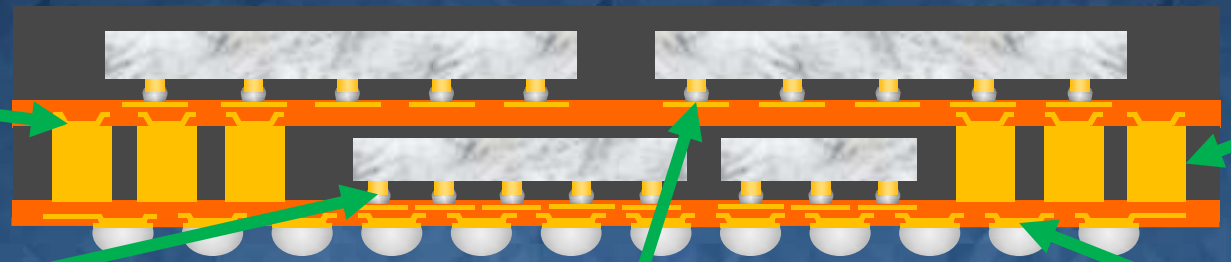
➢ Larger package size enjoys even higher area efficiency



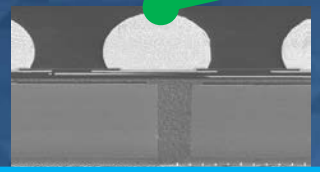
➢ Can break down into smaller “substrate” for testing processing

Advantages of PLFOP

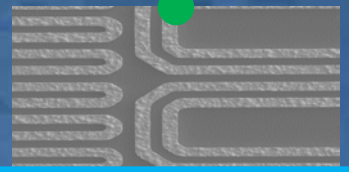
- Thin RDL & PI
- Low Z-height
- Mobile AP



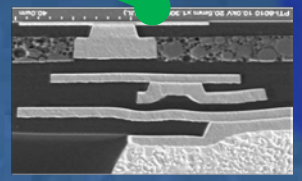
- Fine pitch pillar
- High I/Os
- High BW PoP

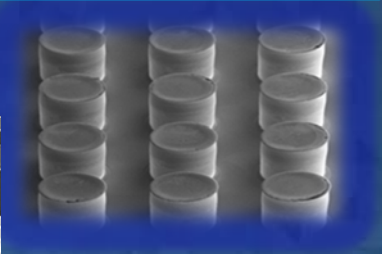


- Side-by-side
- Short transmission & High I/O interconnection
- Logic + Memory



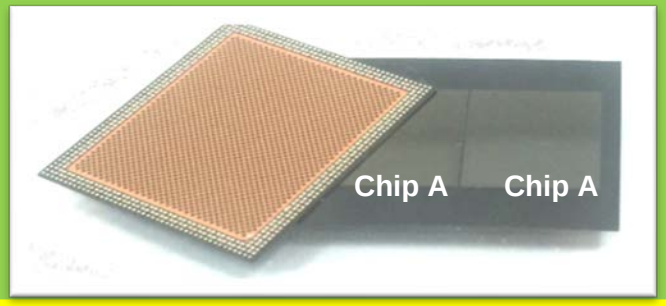
- <5/5um L/S
- Low insertion loss , Coplanar waveguide
- >3 GHz CPU , GPU



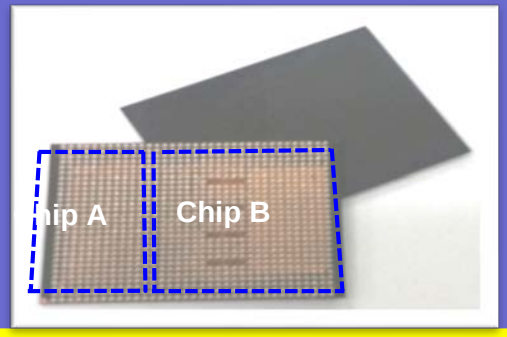


- Short path
- Low J
- PMIC , Power

Homogeneous



Heterogeneous

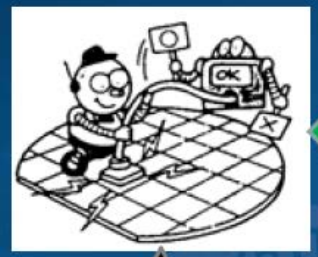


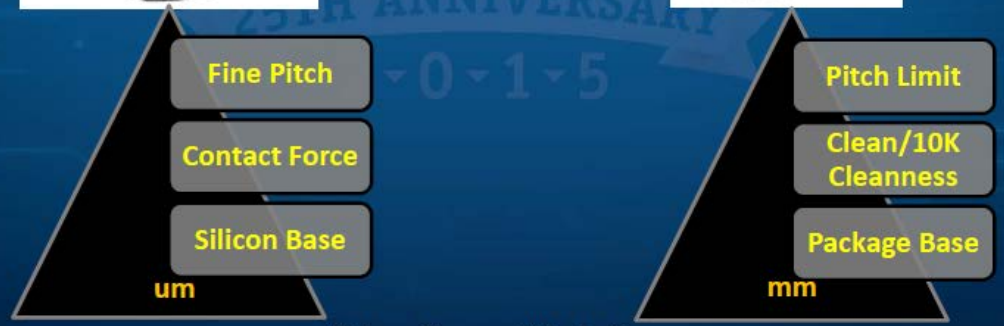
Pillars in Fan Out

Testing Technology Integration (WT+FT+SLT)

More WLP Test or More Finial Test?

- WLP Test
- Finial Test

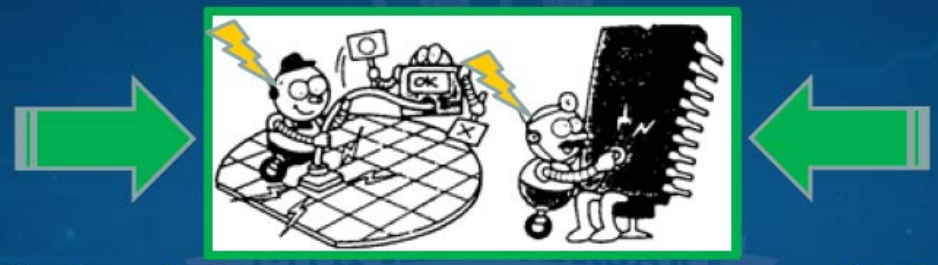




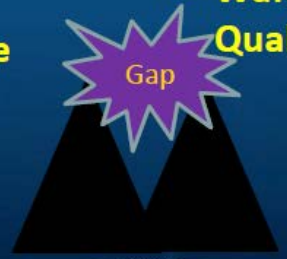
Pictures Source : Mitsubishi

Wafer Test or Finial Test Vender @ WLP Testing?

- Wafer Test Vender
- Finial Test Vender

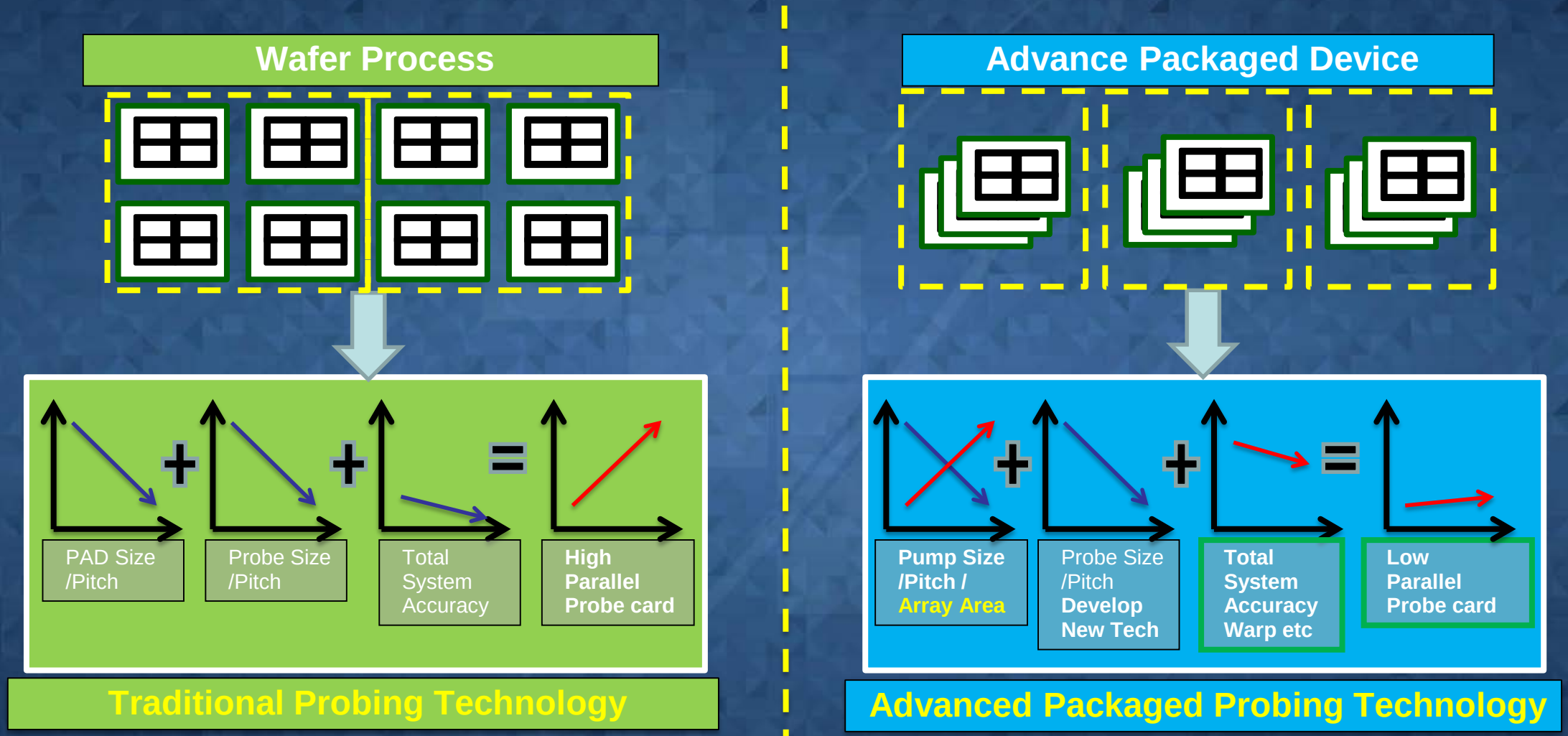


- Cycle Time Challenge
- Cost Challenge
- New Process Challenge
- Cooperation Model Challenge
- Wafer Level Requirement and Quality



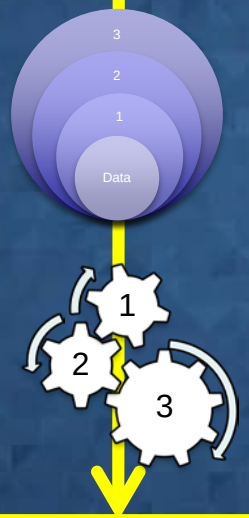
FOPLP Testing could make flexibility Solution in Probing / Finial / SLT Test.

Probing Technology Challenge



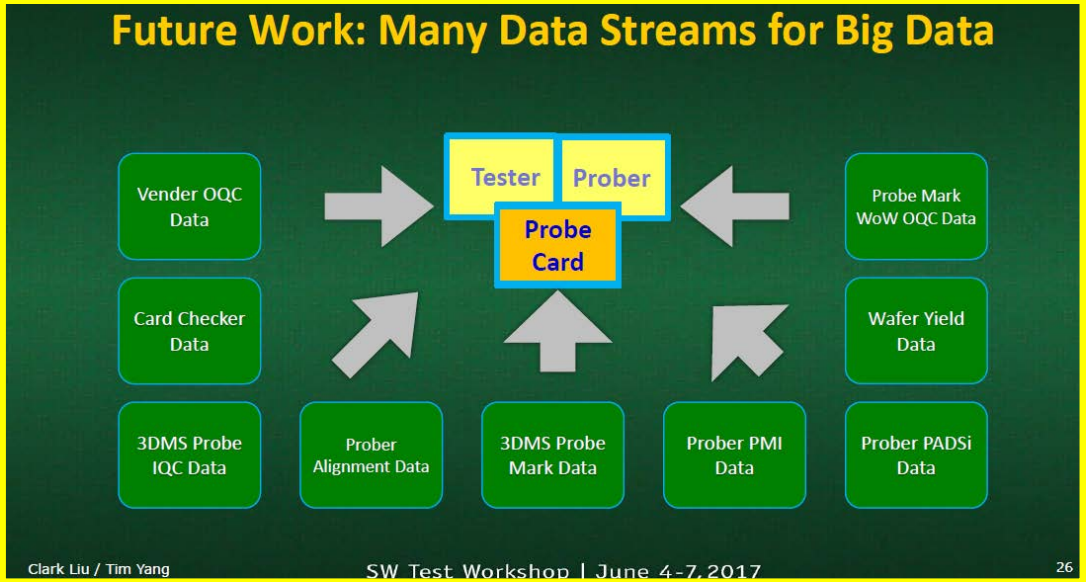
Conclusion

Data Engineering Knowledge



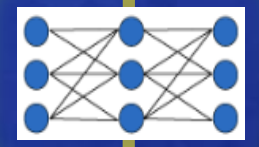
Automation Knowledge

Domain Expert Knowledge



AI Knowledge

Data Analytics Knowledge



Machine Learning Knowledge

Acknowledgments

We would like to thank PTI Group colleagues support for this presentation.

(1) PTI Eric Huang / James Hsieh

(2) TPJ Koike Hiroyuki / TPW Scott Huang

Also thanks suppliers fully support in this project.

(1) FFI Daniel Liang

(2) ITS Danny Chu

Thank you!

Q & A

WAFER DEFECT DIAGNOSIS WITH TEST BIG DATA DRIVEN TECHNIQUES

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KEN , CHAU-CHEUNG CHENG
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CHENG-YEN TSAI
SYING-JYAN WANG
PETER YI-YU LIAO
LEON CHOU
CHEN-SHIUN LEE

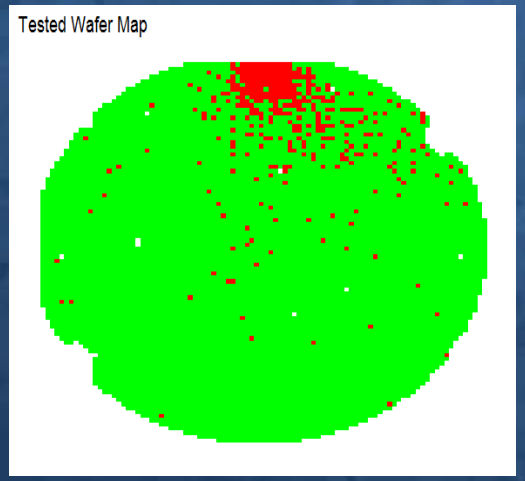
Hsinchu, Taiwan, October 17-18, 2019

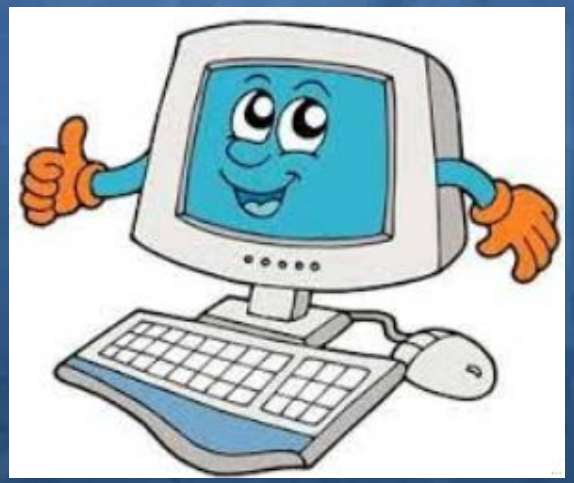
SWTest Asia Podium Presentation Flow

- Introduction / Background
- Methods
- Experiment Results
- Summary
- Benefit / Goal
- Future Work

Introduction / Background (1)

- **There are lots of research about implement Big Data/Machine learning for classify wafer defects:**
  - Classify the defects case before engineer to handle.
  - Time Saving ->Reduce Cost -> Automation …….

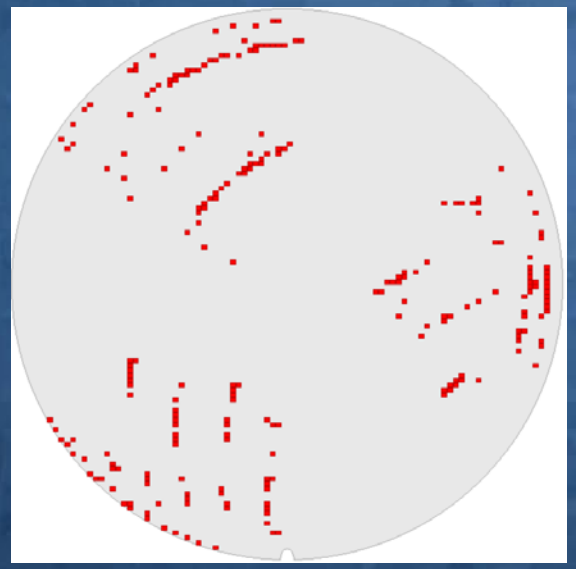




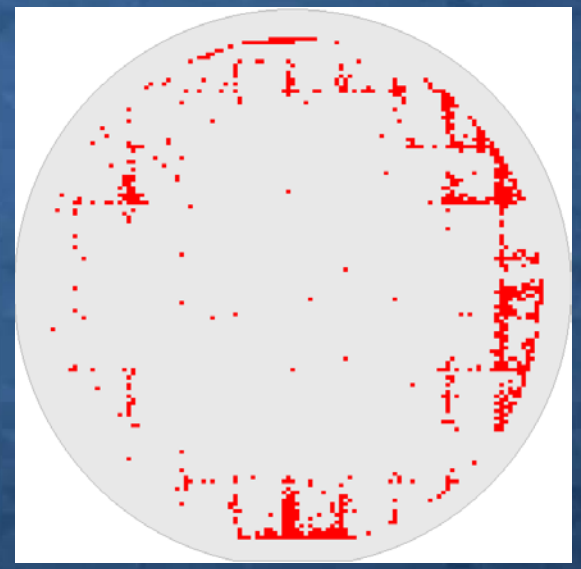
This is Cluster/Local Pattern.

Introduction / Background (2)

- **Wafer pattern is a important information for defect analysis.**
- **Correlation between fail patterns and root cause.**



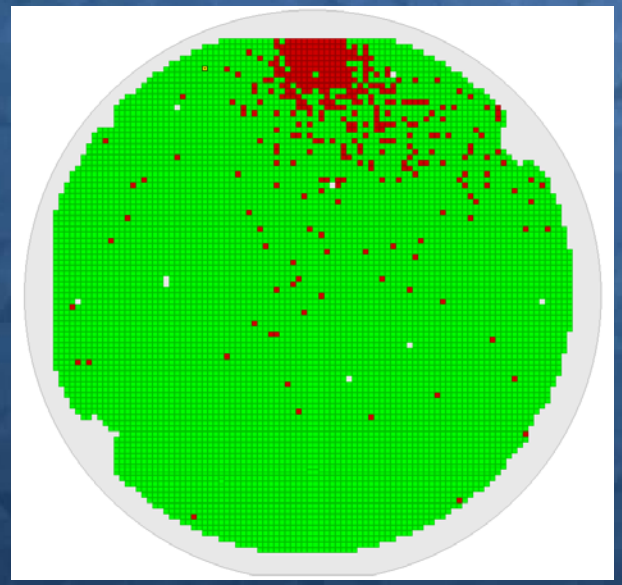
Testing Issue Related Fail



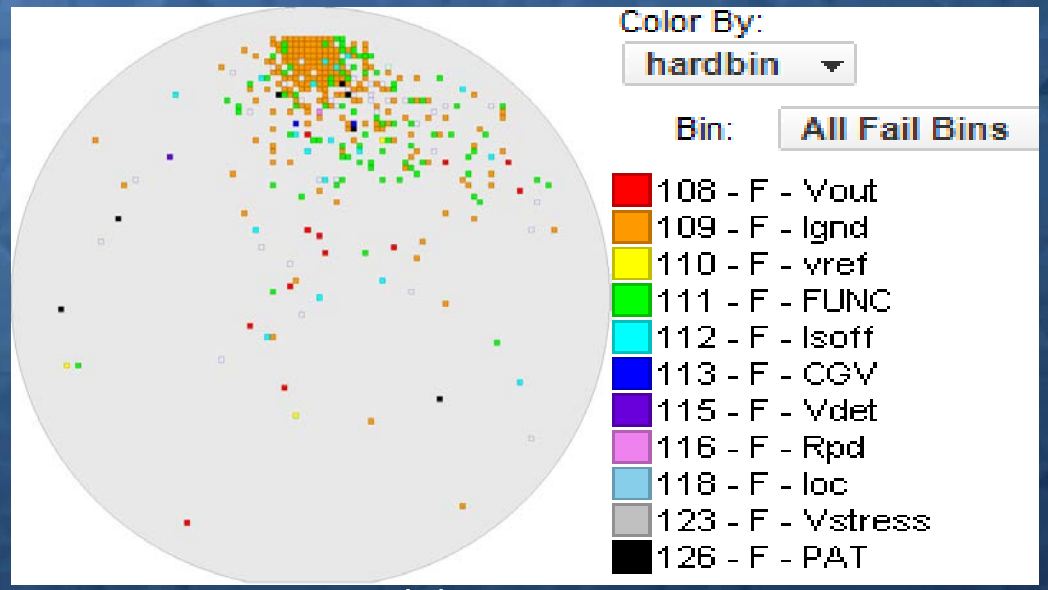
Fab Issue Related Defect

Introduction / Background (3)

- **Most wafer classification focus on Image / geometry (Fail Pass map).**
- **In wafer testing process , engineer need to analyzing electrical testing output as well.**
- **Need to classify / clustering wafer by HardBin for further analysis.**



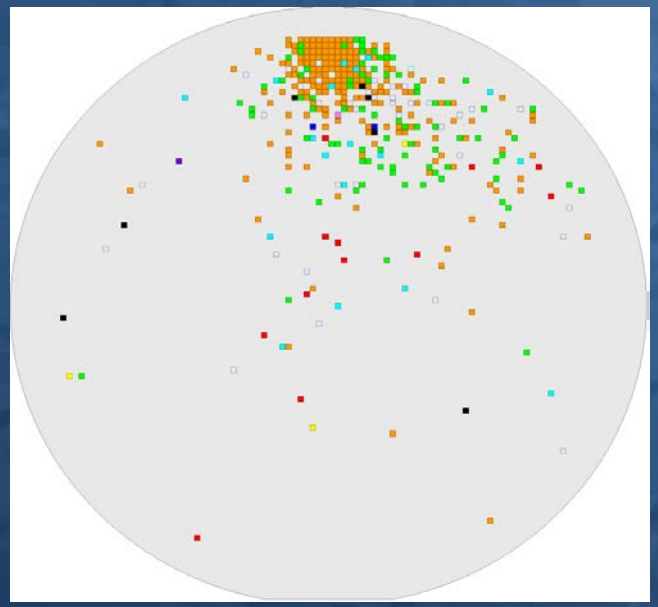
Fail Pass map



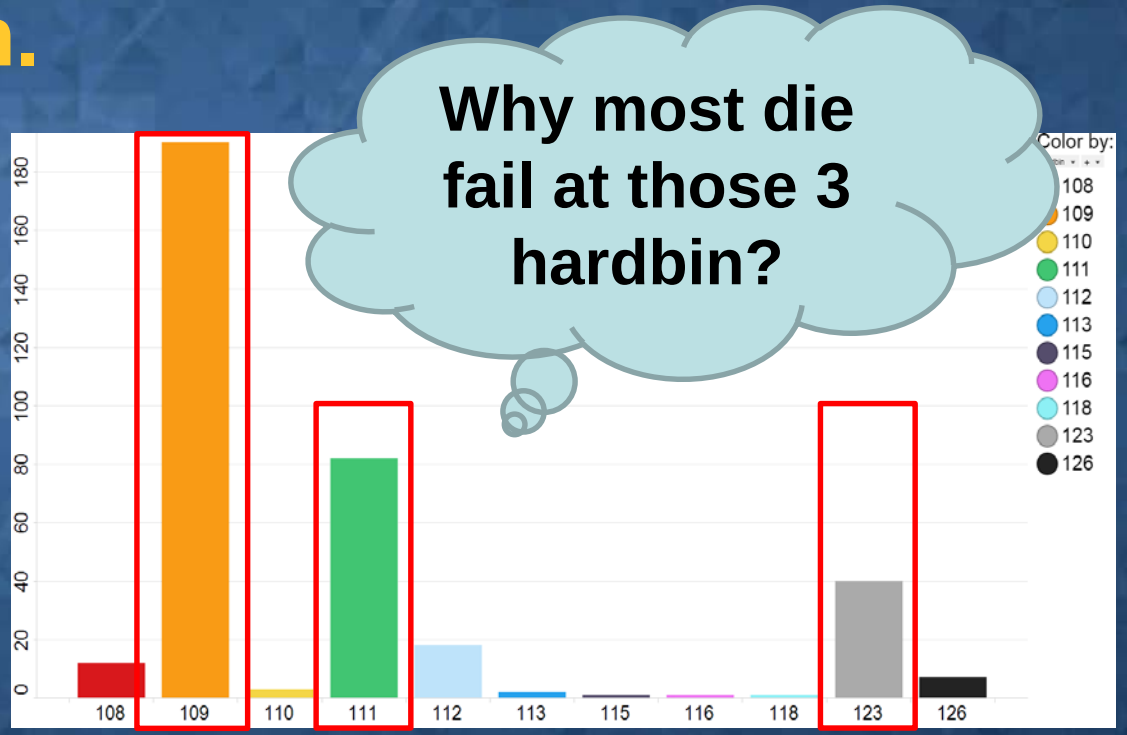
HardBin Map

Methods (1)

- **Hardbin = fail at which reason.**
- **Observe the hardbin distribution on wafer.**
- **Find the most fail hardbin.**



Wafer Hardbin Map



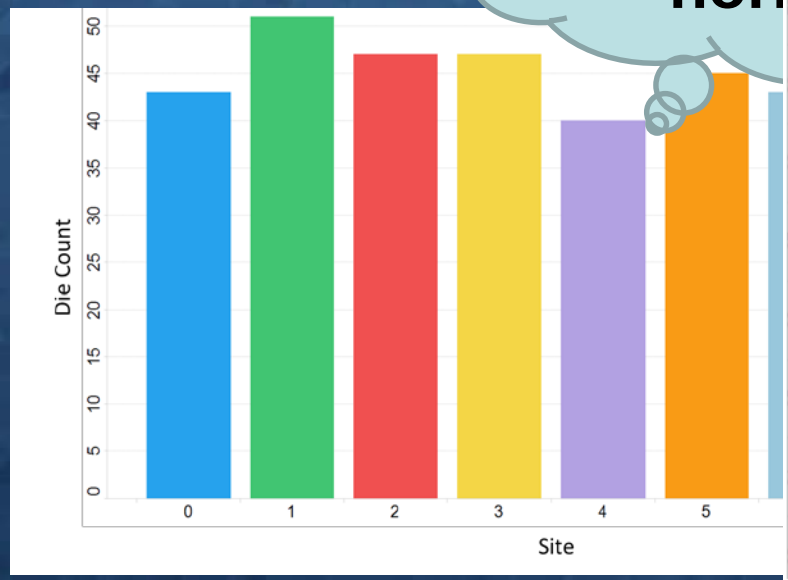
Hardbin distrbution

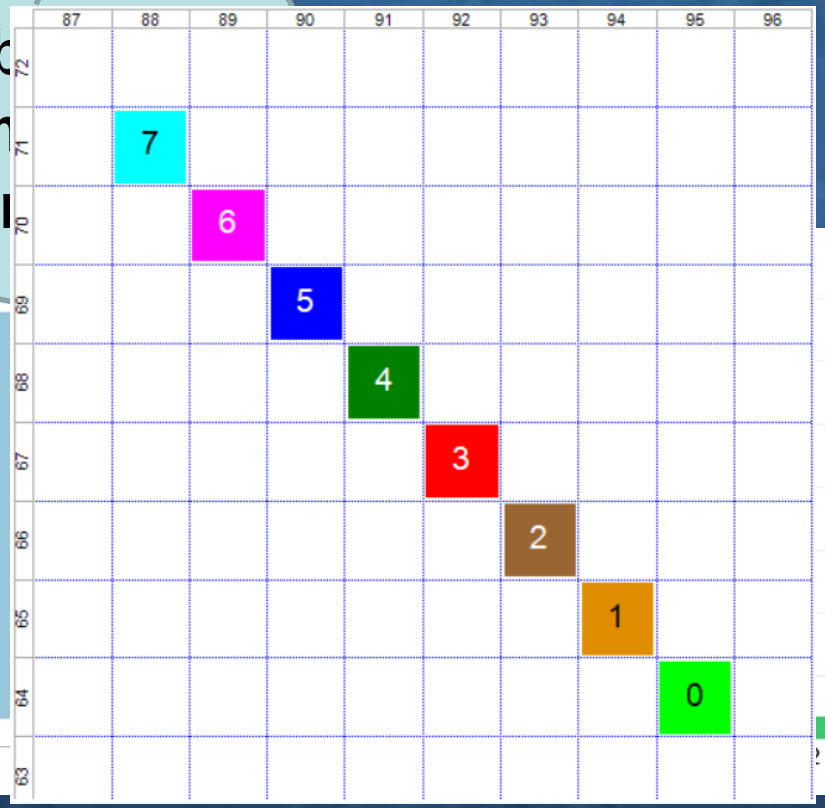
Methods (2)

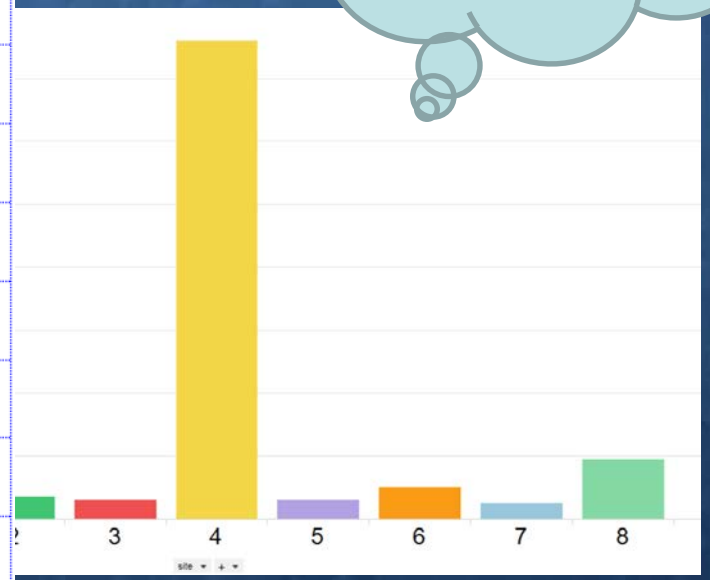
- **Observe the probe card Site distribution on wafer.**
- **Check if fail die concentrate on specific site(s)**

Distrib
seem
nor

Why most die fail at 2 site?



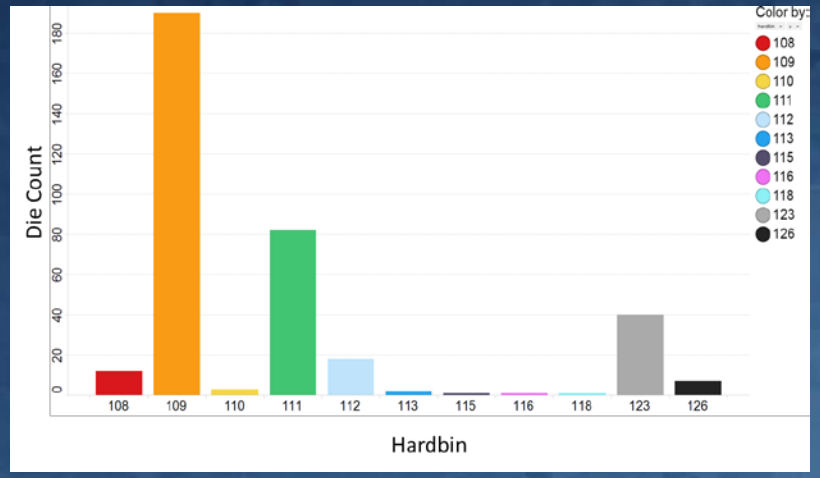




Normal Site Distribution

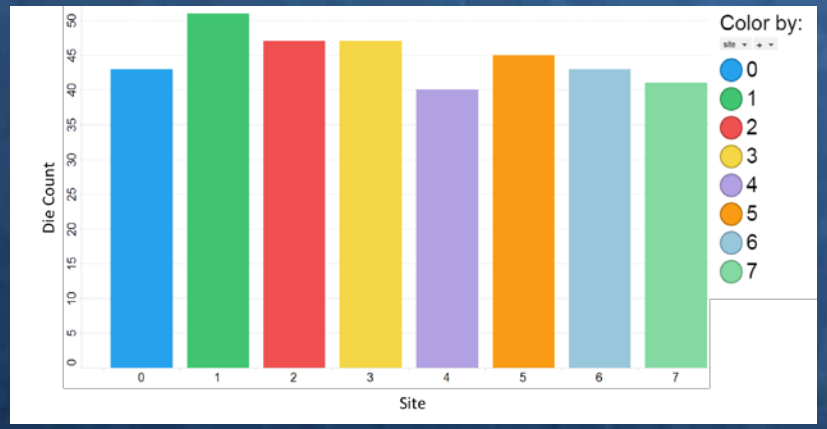
Abnormal Site Distribution

Methods (3)



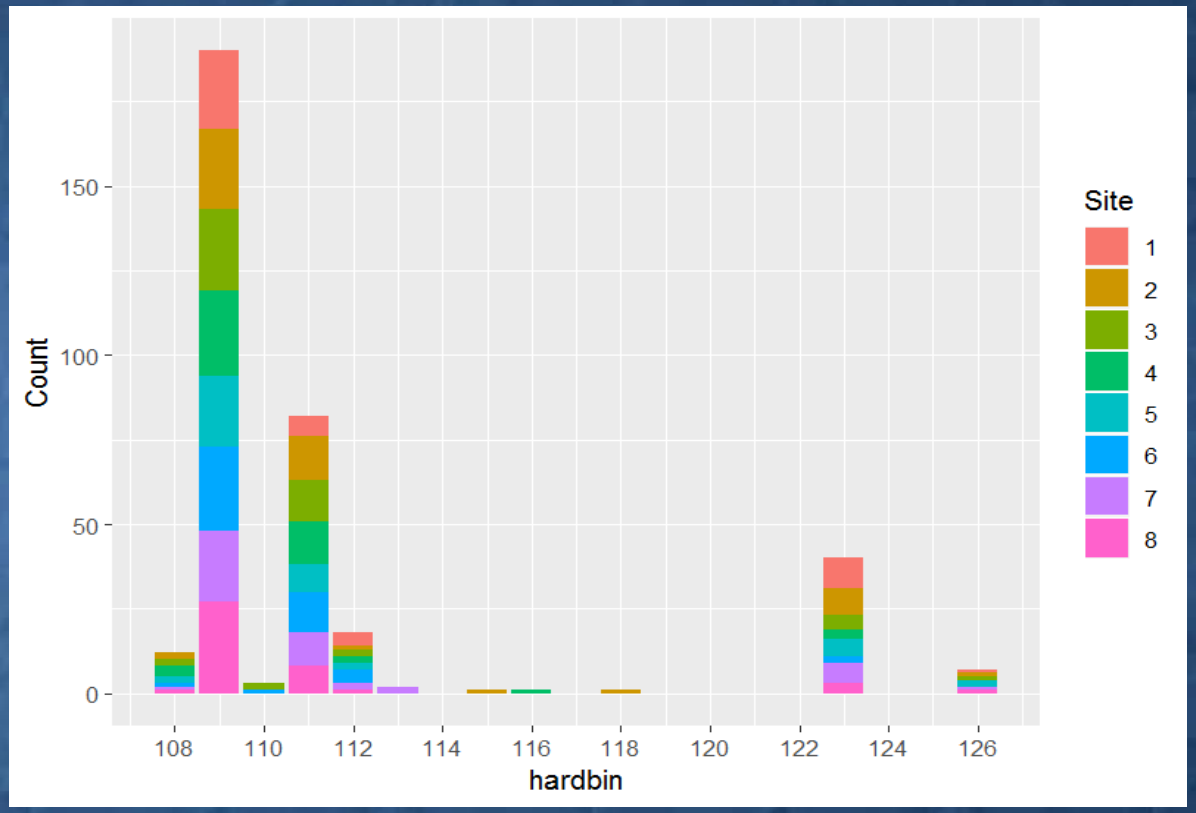
Hardbin distrbution

+



Site Distribution

=

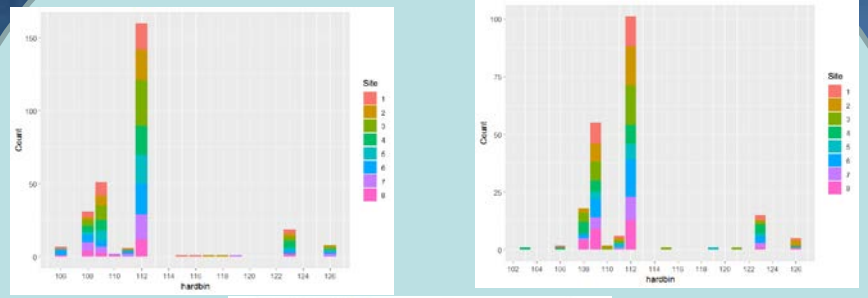


TestDNA Histogram

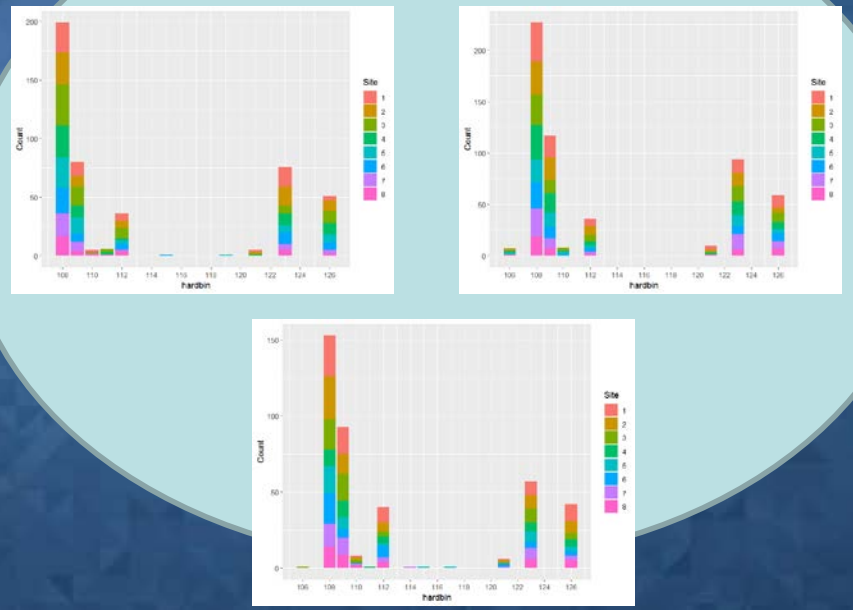
Methods (4)

- **Grouping Wafer by TestDNA with similarity:**

Type A



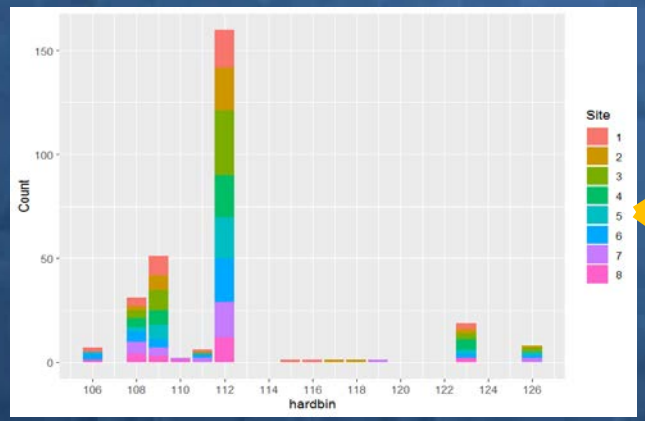
Type B



. . . .

Methods (5)

- **Features extraction and quantification:**



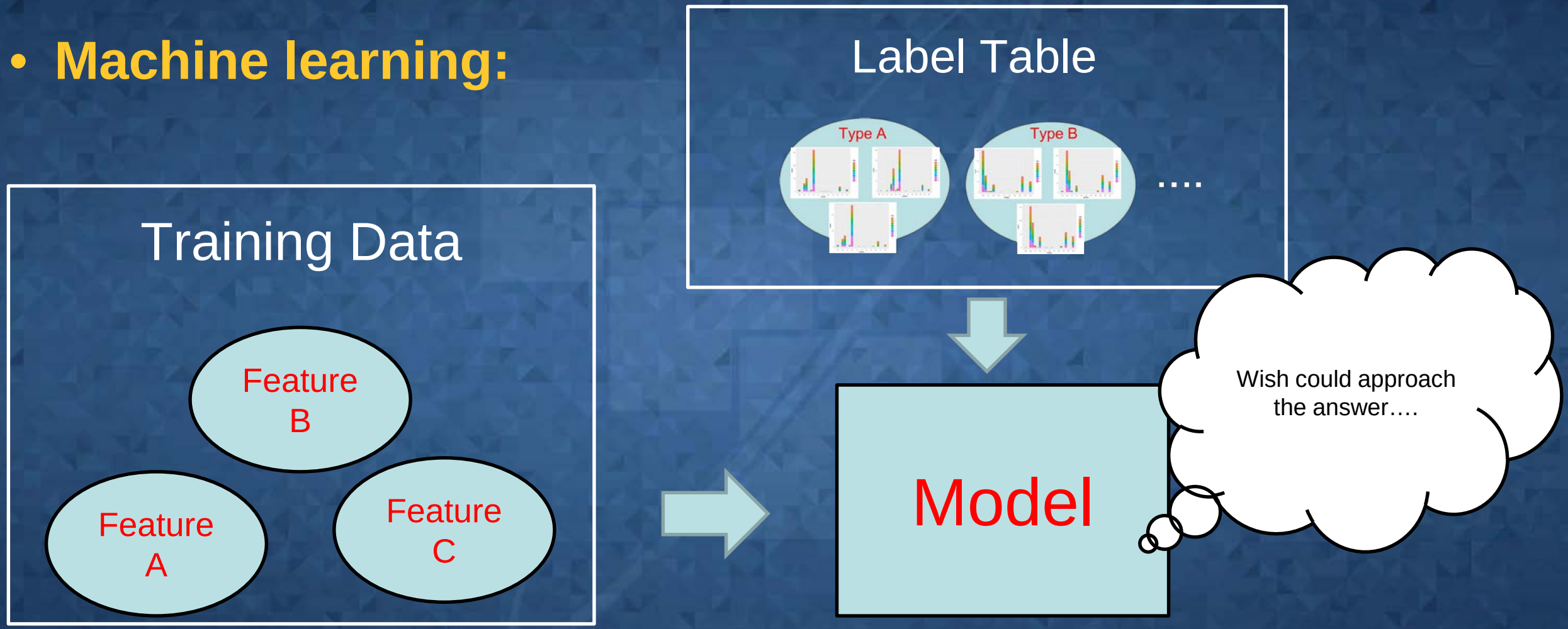
Feature A

Feature B

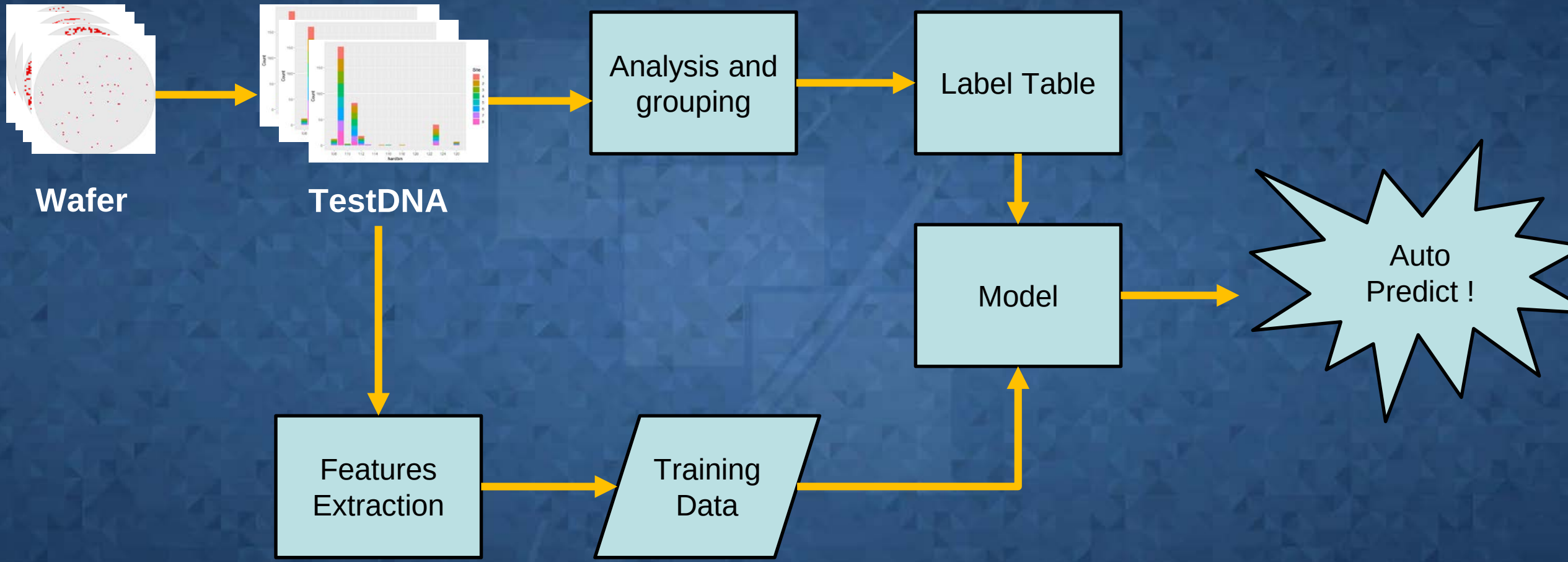
Feature C

Methods (6)

- **Machine learning:**



Methods (7) - Flow



Experiment Setup

- **314 wafers sperate to 10 class (9 defect class and 1 random class)**
- **Train : Test = 60% : 40% = 188 wafers : 126 wafers**
- **All wafers come from same product.(Same Fab process and tested by same process)**

Experiment Results

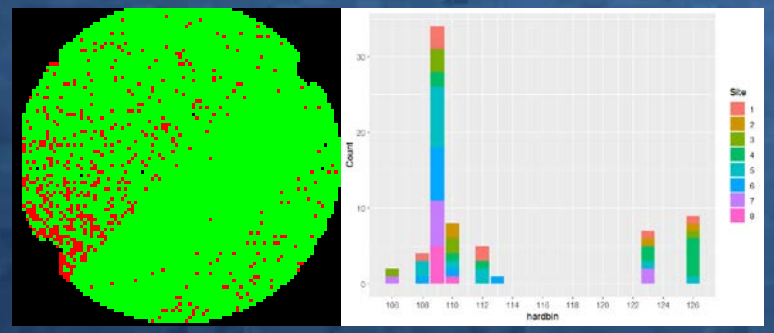
		Annotation									
		A	B	C	D	E	F	G	H	I	None
Prediction	A	**8 (88.9%)**	0	0	0	0	0	0	0	0	1 (11.1%)
	B	0	**6 (100%)**	0	0	0	0	0	0	0	0
	C	0	0	**7 (87.5%)**	0	0	0	0	1 12.5%	0	0
	D	0	0	1 (2.8%)	**34 (94.4%)**	0	0	0	0	0	1 (2.8%)
	E	0	0	0	0	**7 (100%)**	0	0	0	0	0
	F	0	0	0	0	0	**1 (100%)**	0	0	0	0
	G	0	1 (6.25%)	0	0	0	0	**14 (87.5%)**	0	0	1 (6.25%)
	H	0	0	1 (16.7%)	1 (16.7%)	0	0	0	**4 (66.6%)**	0	0
	I	0	0	0	0	0	0	0	0	**2 (100%)**	0
	None	0	0	0	0	0	1 (2.9%)	0	1 (2.9%)	0	**33 (94.2%)**

- **Average accuracy is ~92%**

Condition

1. **Need labeling the TestDNA Type by human since it's a *Supervised Learning*.**

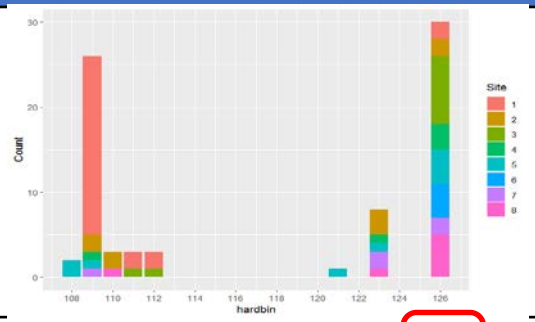
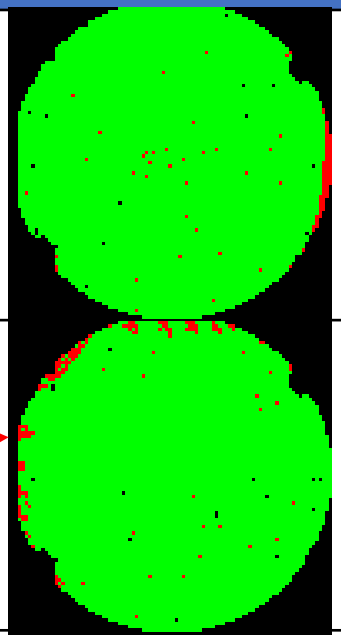
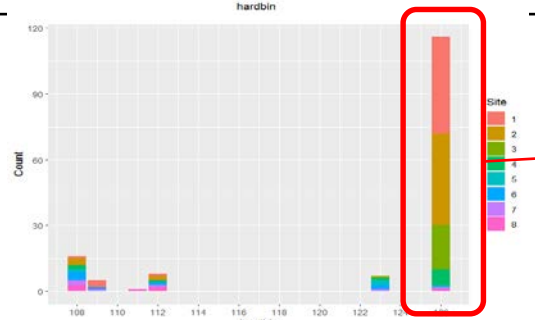
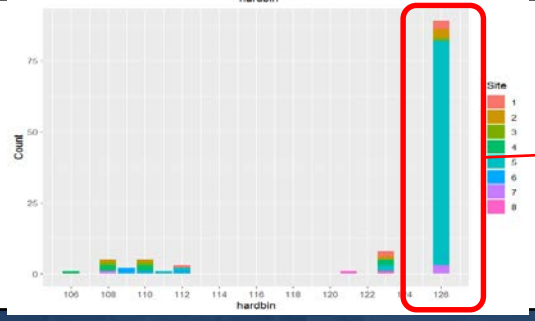
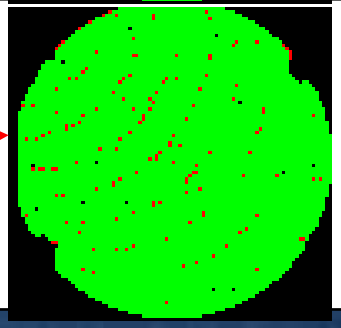
2. **Can not classify the wafer which have no similar wafers.**



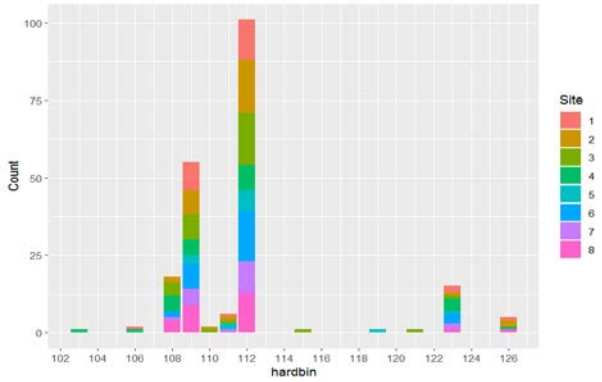
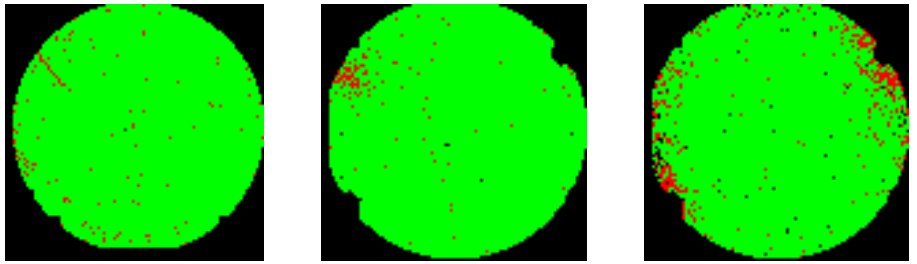
Wafer Map and TestDNA

If only one wafer TestDNA look like this in whole dataset.
How can we classify this?

Summary (1)

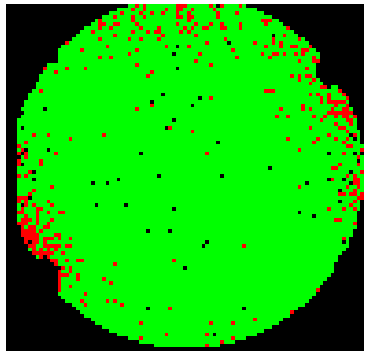
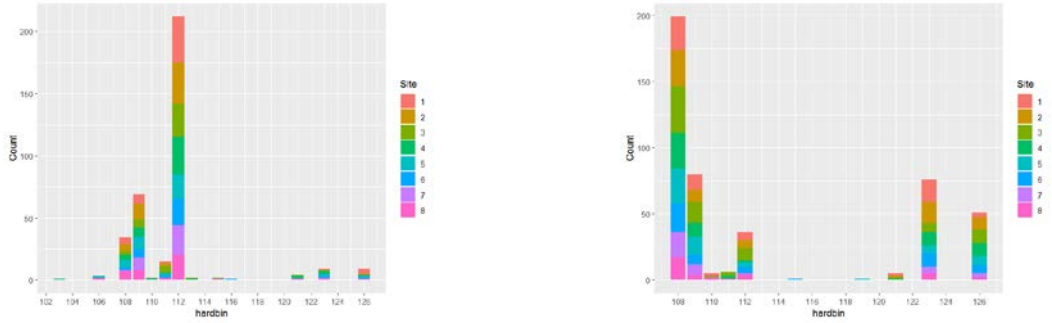
TestDNA Type	TestDNA Defect Mode Histogram	Wafer Map Patterns
Type 1		
Type 2		
Type 3		

Summary (2)

TestDNA Type	TestDNA Defect Mode Histogram	Wafer Map Patterns
Type 4		

- The Correlation between TestDNA and Patterns could be ***1 to multiple .***

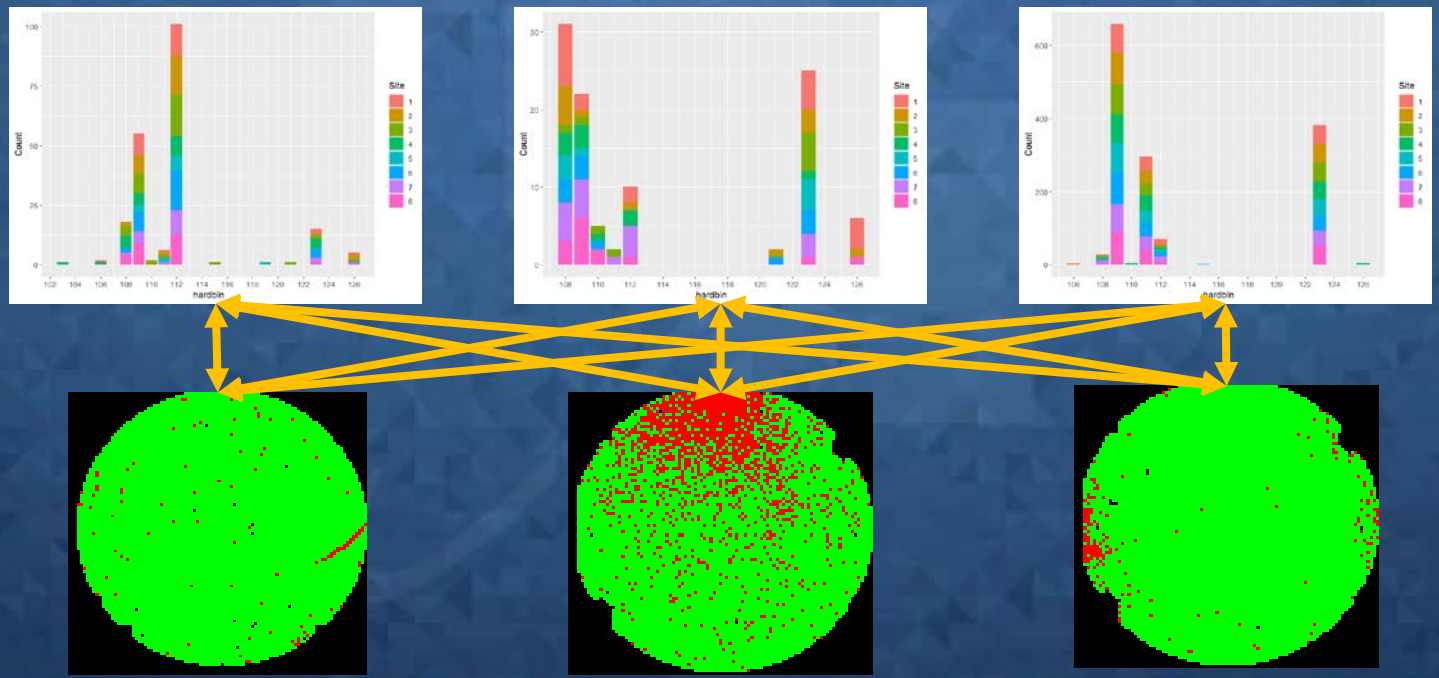
Summary (3)

Pattern Type	Wafer Map Patterns	TestDNA Defect Mode Histogram
Tennis		

- **Same Wafer Pattern could be find in different TestDNA Type.**

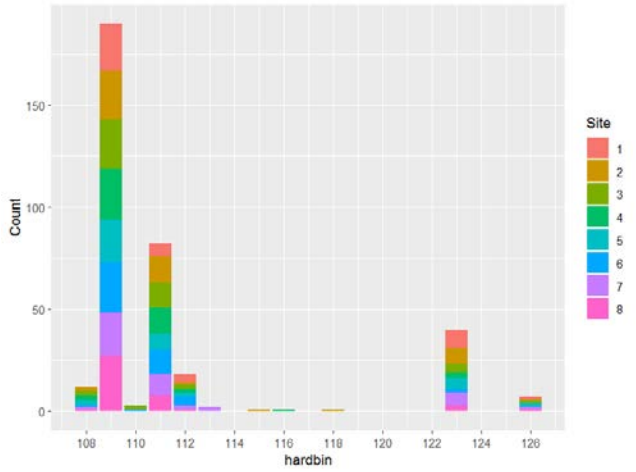
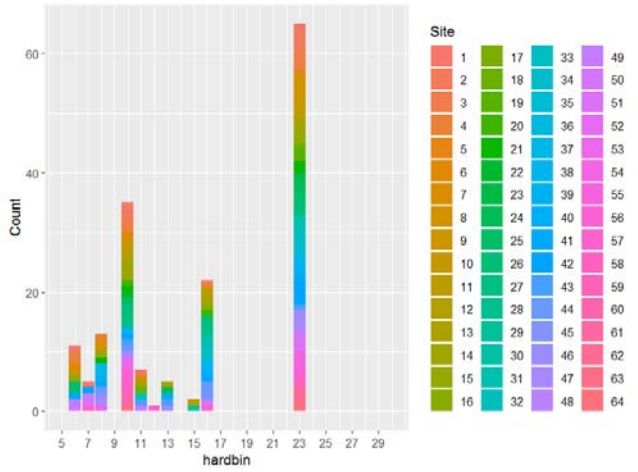
Summary (4)

- **The Correlation between TestDNA and Patterns could be *1 to 1 or 1 to multiple or even multiple to multiple.***
- **Input more features and dimension into machine for analysis.**

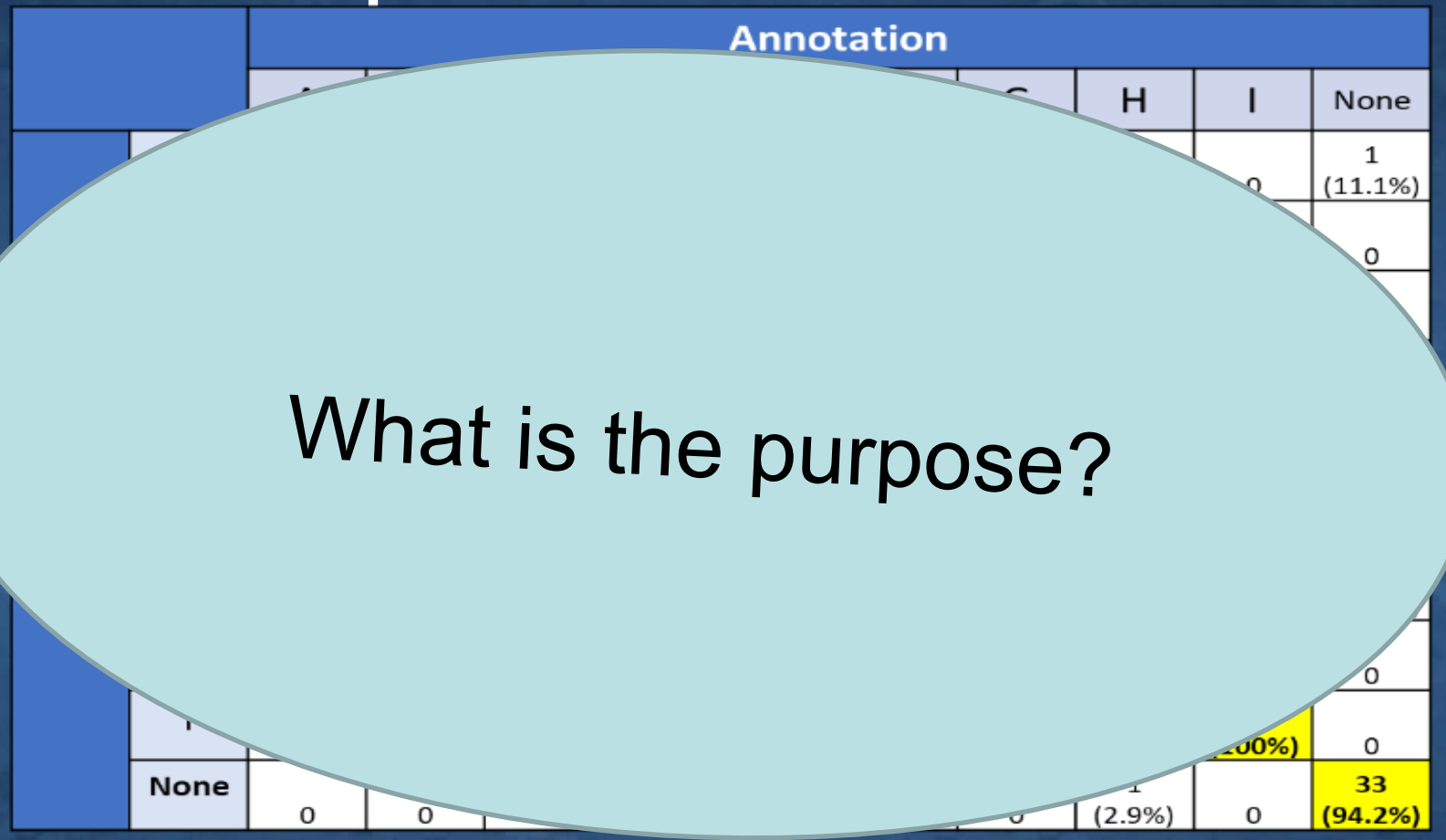


Summary (5)

- **Different** ***Product's*** **Wafer have** ***Different Characteristic (Different Hardbin and site setting …)***

Product	A	B
TestDNA Histogram		
Number of site	8	64
Hardbin Range	108 to 188	5 to 29

Experiment Results

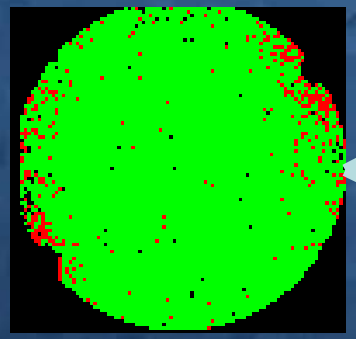


- **Average accuracy is ~92%**

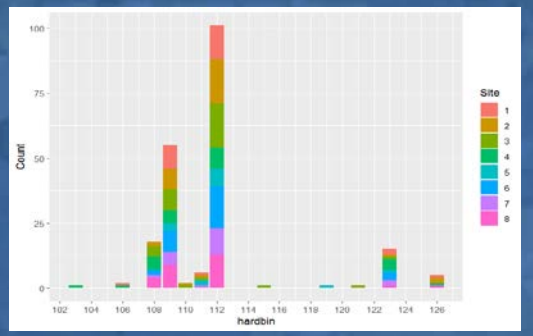
Benefit

1. **Classify the Wafer Patterns and TestDNA (Defect characteristic)**

Edge-Local / Edge-Cluster

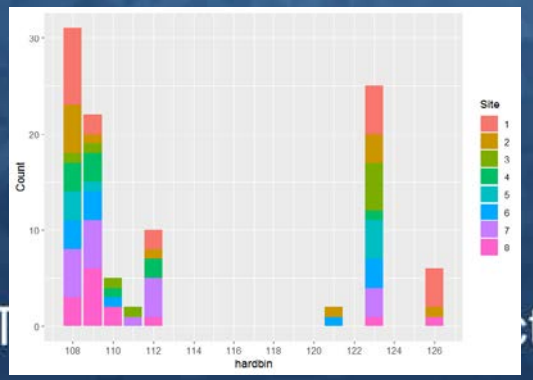


Type A

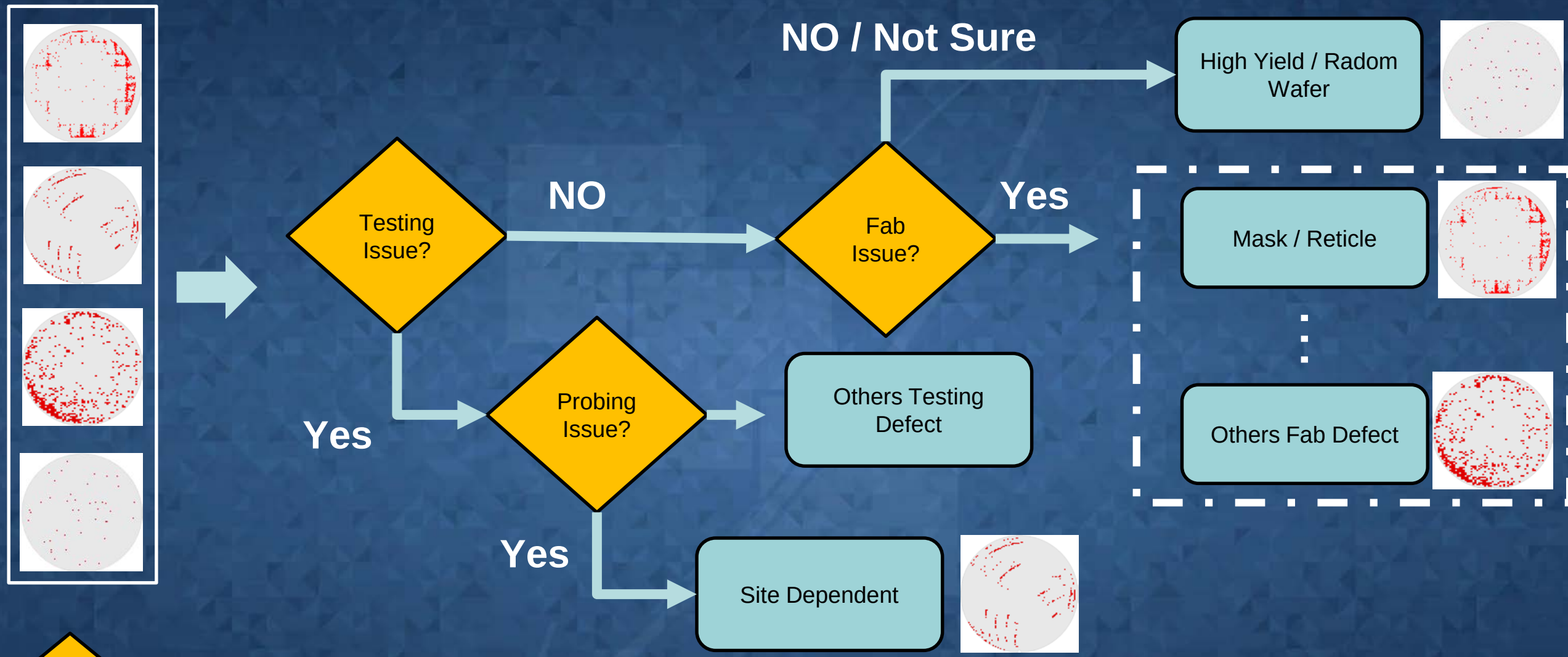


Defect Root Cause A

Type B

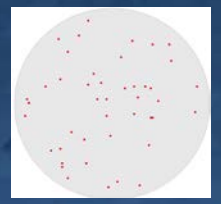


Defect Root Cause B


Wafer Input
Testing Issue?
NO
Fab Issue?
NO / Not Sure
High Yield / Radom Wafer
Yes
Mask / Reticle
Others Fab Defect
Probing Issue?
Yes
Others Testing Defect
Yes
Site Dependent
Analysis
Result

NO / Not Sure

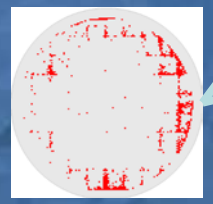
High Yield / Radom Wafer



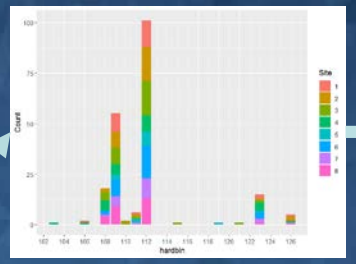
Fab Issue?

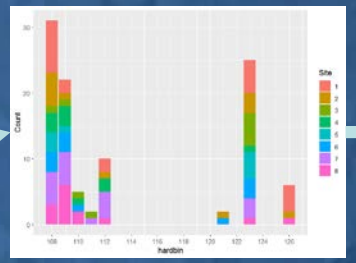
Yes

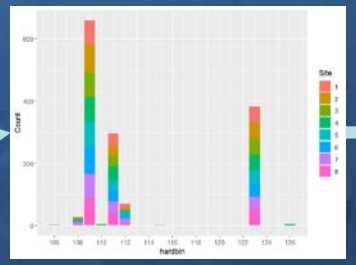
Mask / Reticle



Others Fab Defect







Root Cause A

Root Cause B

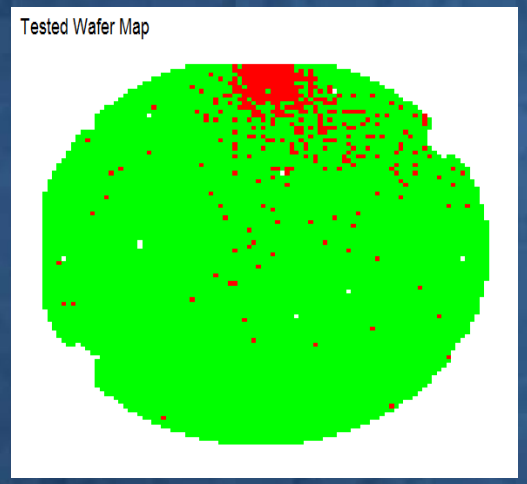
Root Cause C

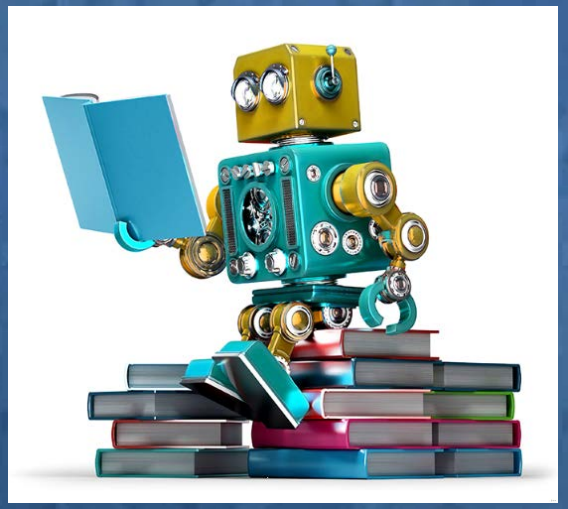
Analysis

Result

Goals

- **Root Cause Analysis -> Correspond Action**

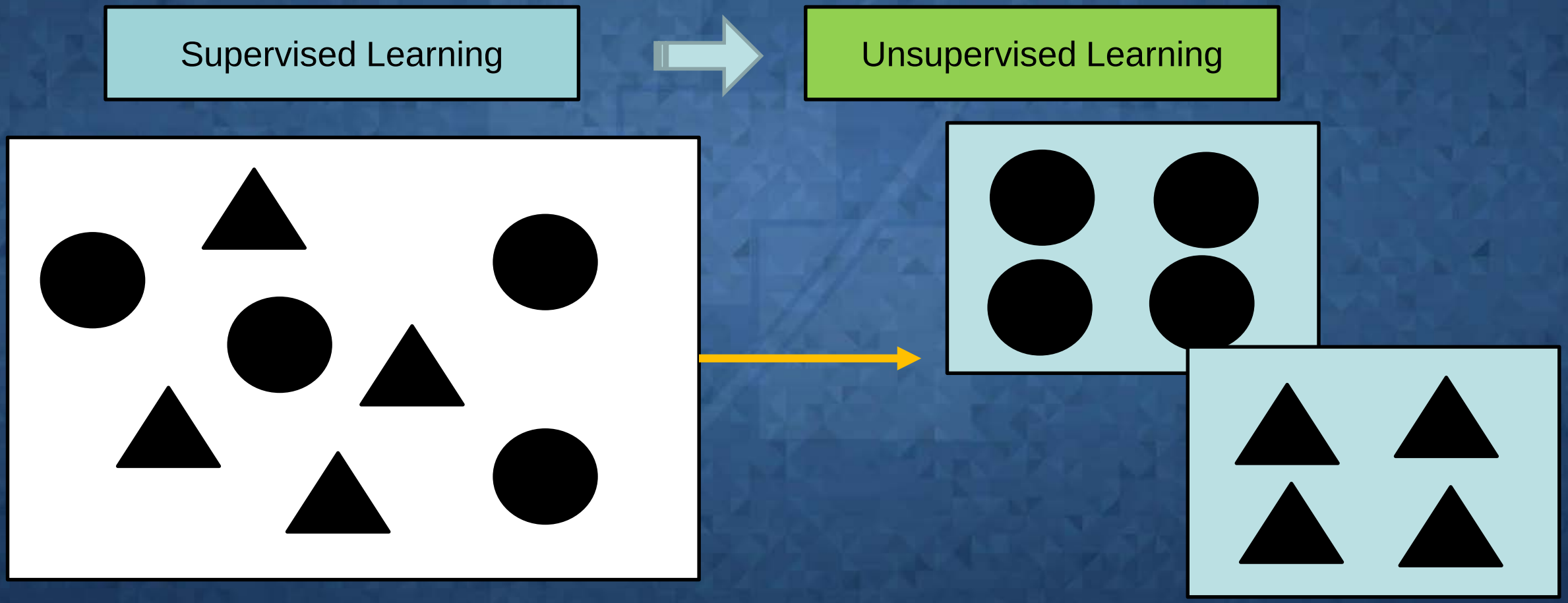




1. This is Cluster Pattern.
2. Hardbin distribution is ….
3. Therefore the Root Cause maybe A/B/C
4. ***Therefore , We should ….***

Future Work

- **Overcome the Condition :**



Thank You!

SWTEST ASIA 2019

Probe Card Electrical Quality Enhancement using Big Data Analytics

MPI CORPORATION

Kenny Huang, Steven Wu
Fred Chou, Alex Wei

1 2 3

Ying-Jen Chen[1], Yu-Mei Ling[2],
Yi-Yu Chen[2], Chen-Fu Chien[2,3]

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AiMS 人工智慧製造系統研究中心
AIMS, Taiwan, R.O.C.
Artificial Intelligence for Intelligent Manufacturing Systems Research Center

Hsinchu, Taiwan, October 17-18, 2019

Overview

- Background
- Objectives
- Methods
- Conclusion

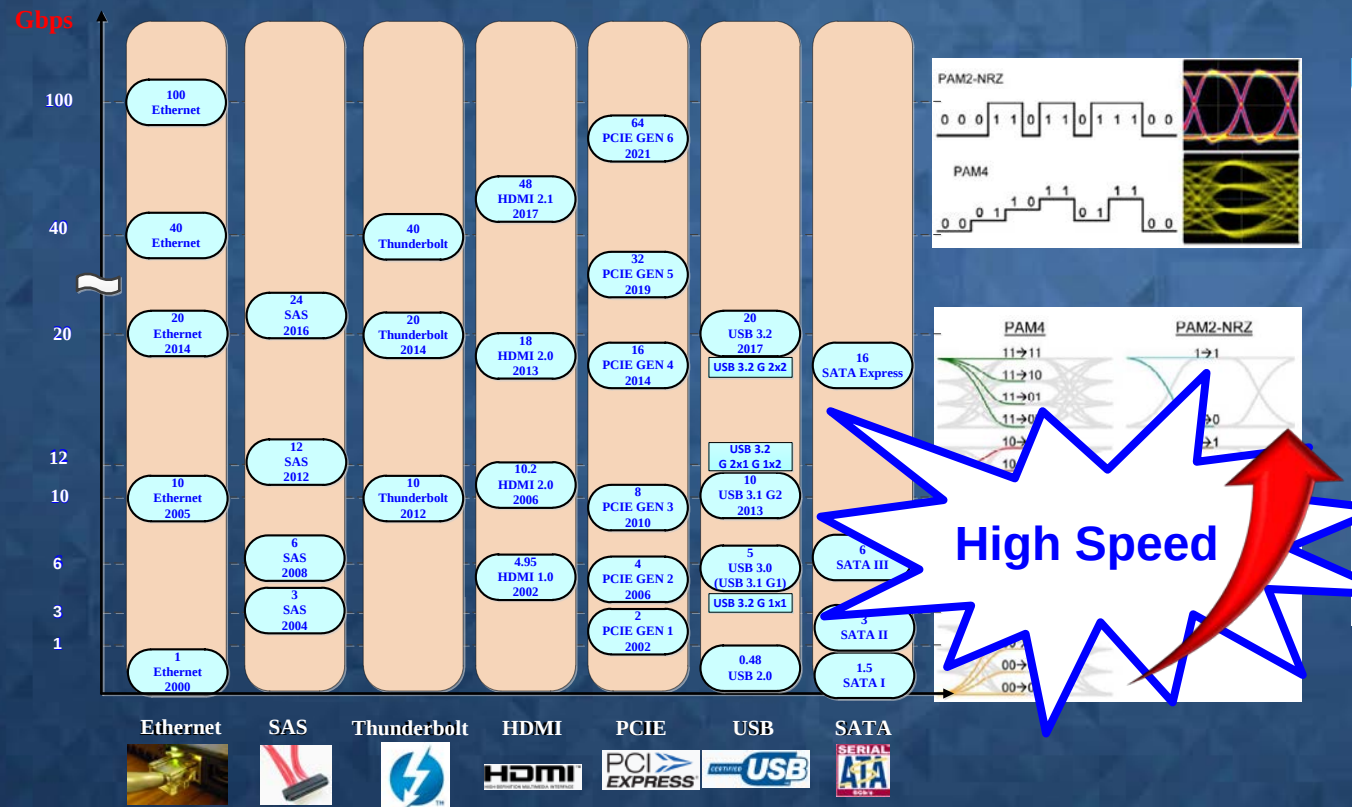
Background

- With the rapid development in smart technology, 5G transmission is a necessary trend in smart life. From smartphones, Virtual Reality, autonomous cars, to home appliances, the technology is reshaping our lifestyle. With all the signs, smart city is the trend and direction now and will be more in the future.

Source: https://www.ubermetrics-technologies.com

Increasing Electrical Requirements for IC

- In response to the 5G technology, the requirements for high-speed transmission of electronic products are getting higher while power loss is expected to be lower.

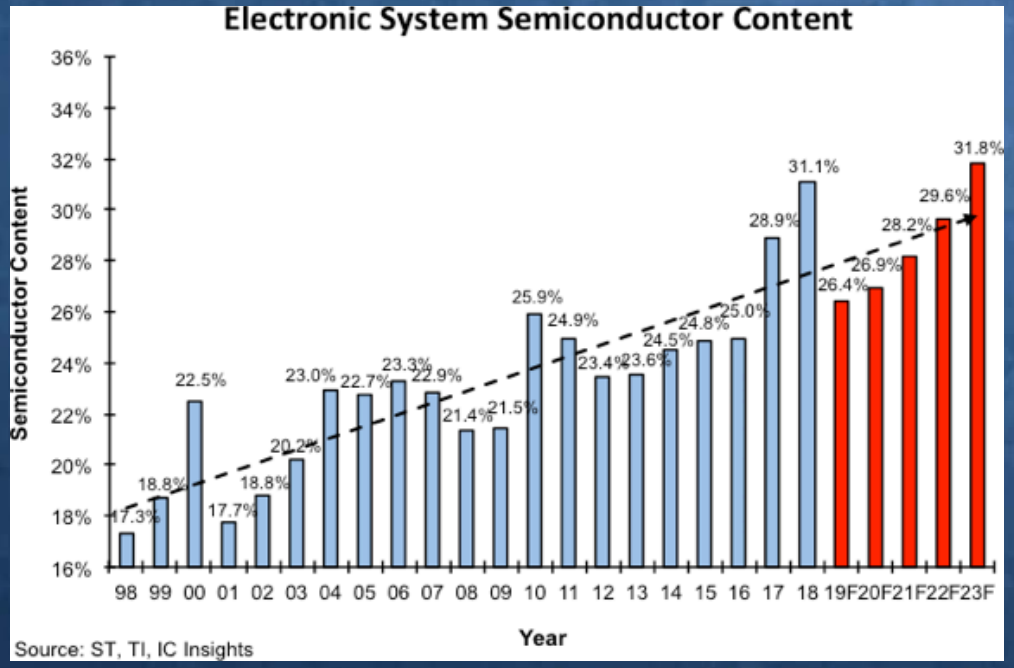


Year	Feature (nm)		Power (W)		Vdd (V)		Current (A)		Chip Freq (GHz)		Target Z (mΩ)	
1997	250		70		2.5		28		0.75		4.5	
1999	180		90		1.8		50		1.25		1.8	
2001	150		110		1.5		73		1.5		1.0	
2003	130		130		1.5		87		2.1		0.9	
2006	100	70	160	180	1.2	1.1	133	164	3.5	3.9	0.45	0.34
2009	70	50	170	200	0.9	1.0	1[illegible]	200	6.0	7.6	0.23	0.25
2012	50	36	175	[illegible]	0.6	[illegible]	[illegible]	[illegible]	[illegible]0.0	14.9	0.10	0.20
2015		25	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	29.1		0.16
2018		18	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	56.8		0.12
2020		14	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]8.8			0.12

Rdc(mΩ)
Power loss

Probe Card Quality Requirements

- The frequency of replacing and seeking for high configuration electronic devices has been declining nowadays, when people are looking for a better bargain.
- Reflecting to the industrial supply chain, the demand to test chips with same specification is increasing; hence, the demand for probe cards is changing from small-volume large-variety to large-volume small-variety. Therefore, it's vital to ensure the consistent quality of each probe card.



$B	2018	2019	2019/2018
Global electronic systems market	1,615	1,680	4%
Worldwide semiconductor market	504.3	443.8	-12%

Source : ICinsights
http://www.icinsights.com/news/bulletins/Semi-Content-In-Electronic-Systems-Forecast-To-Drop-To-264-In-2019/

Overview

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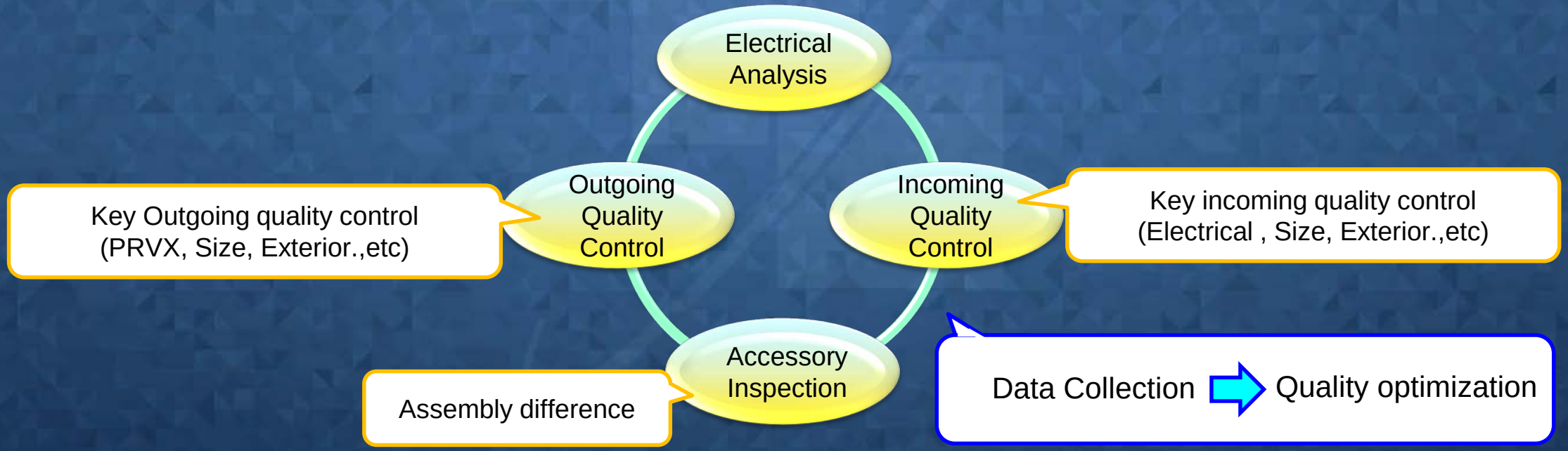
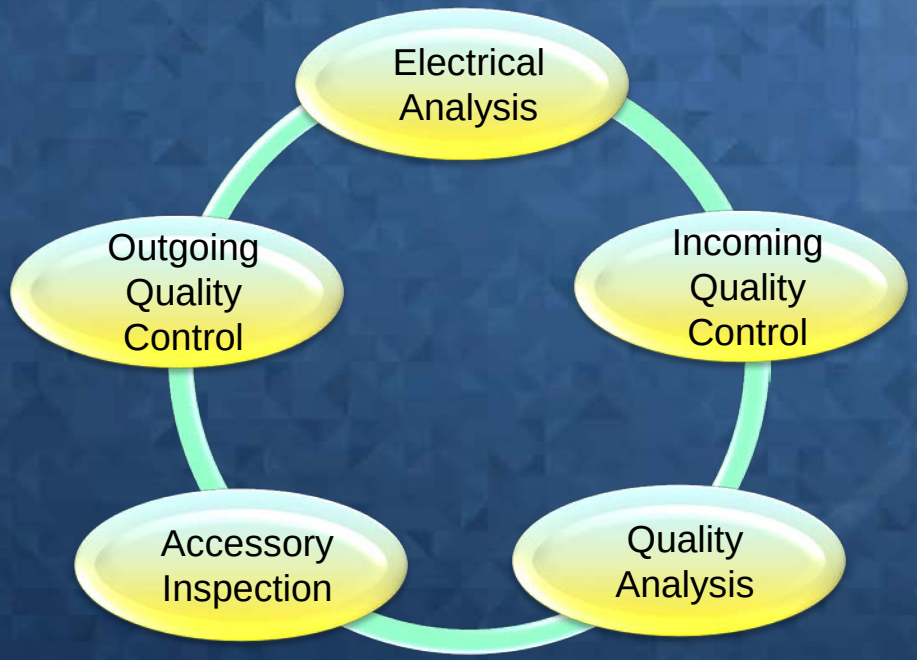
The Ordeal of Probe Card Inspection

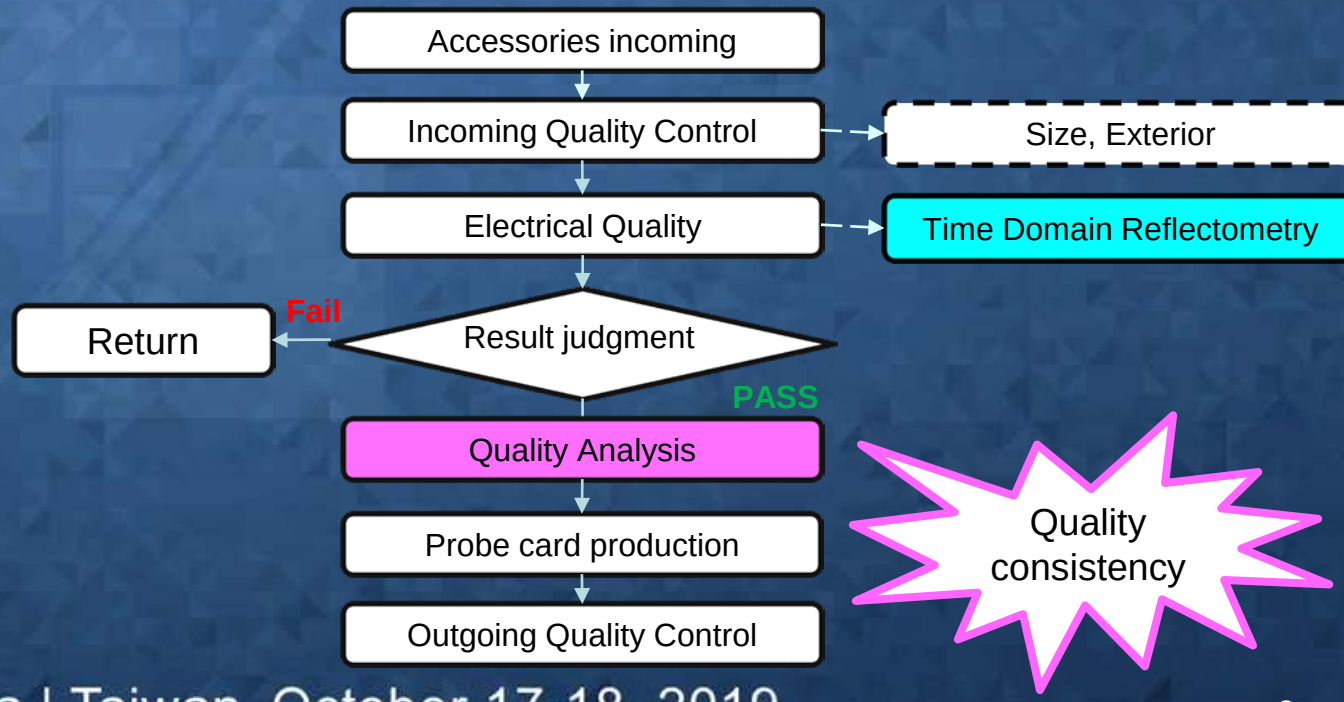
- With the rapid innovation of electronic devices, it corresponds to the timeliness of chip testing. In order to meet customer's needs, a rigorous and fast inspection focus on electricity, appearance, and mechanism, will be performed on probe cards from the order is placed to the shipment.
- However, to expedite the inspection could not satisfy the requirement of testing in a large amount of the same specification of chip.



The Quality Inspection Solution of Probe Card

- To integrate the complete data of a probe card, from the quality inspection data, material data, assembly data and electrical characteristic data, all of these information are quite huge and complex. It is difficult to find out the improvement of the key project.
- Therefore, we take priority from the "electrical characteristic data" of the key materials of the probe card.





Overview

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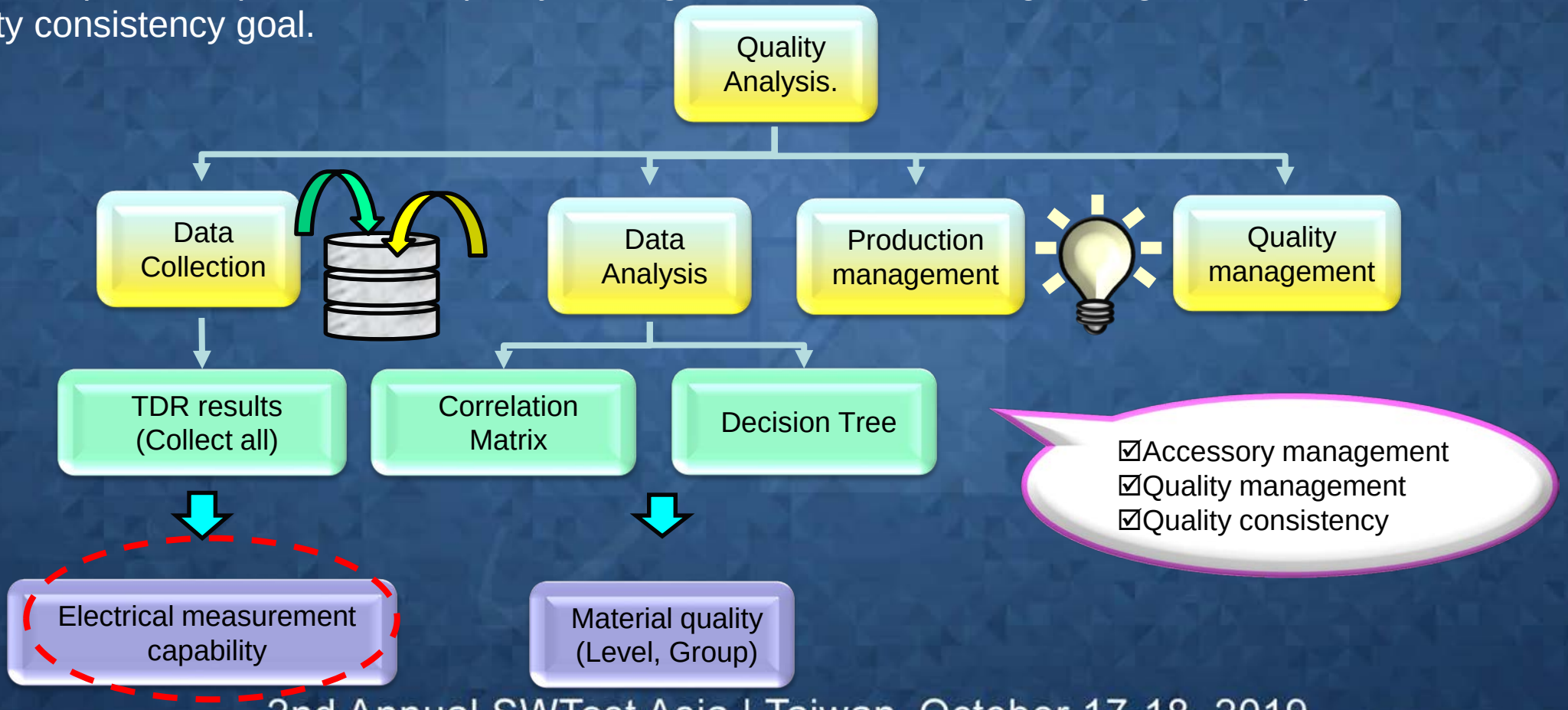
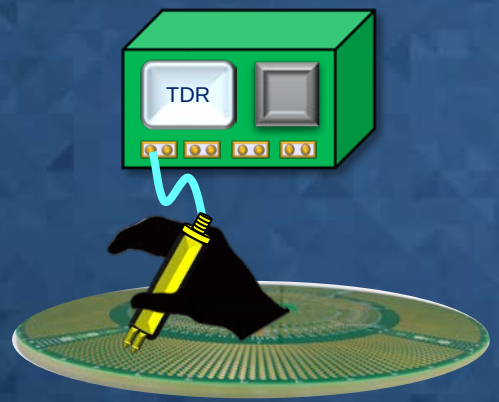
Optimize the Quality of the Probe Card

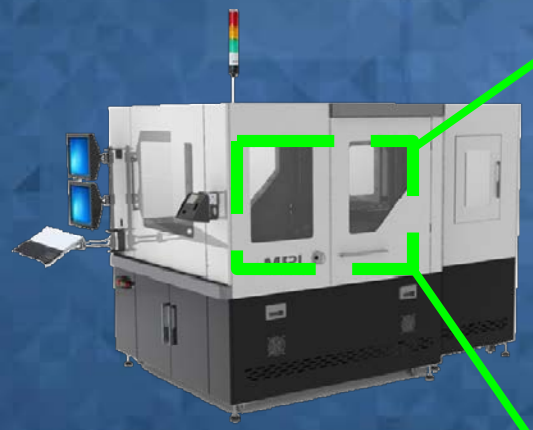
- Collecting the complete electrical characteristic data, and find out the consistency between the materials through the data analysis technology
- Then complete the process and quality management and monitoring throughout the process to achieve the quality consistency goal.

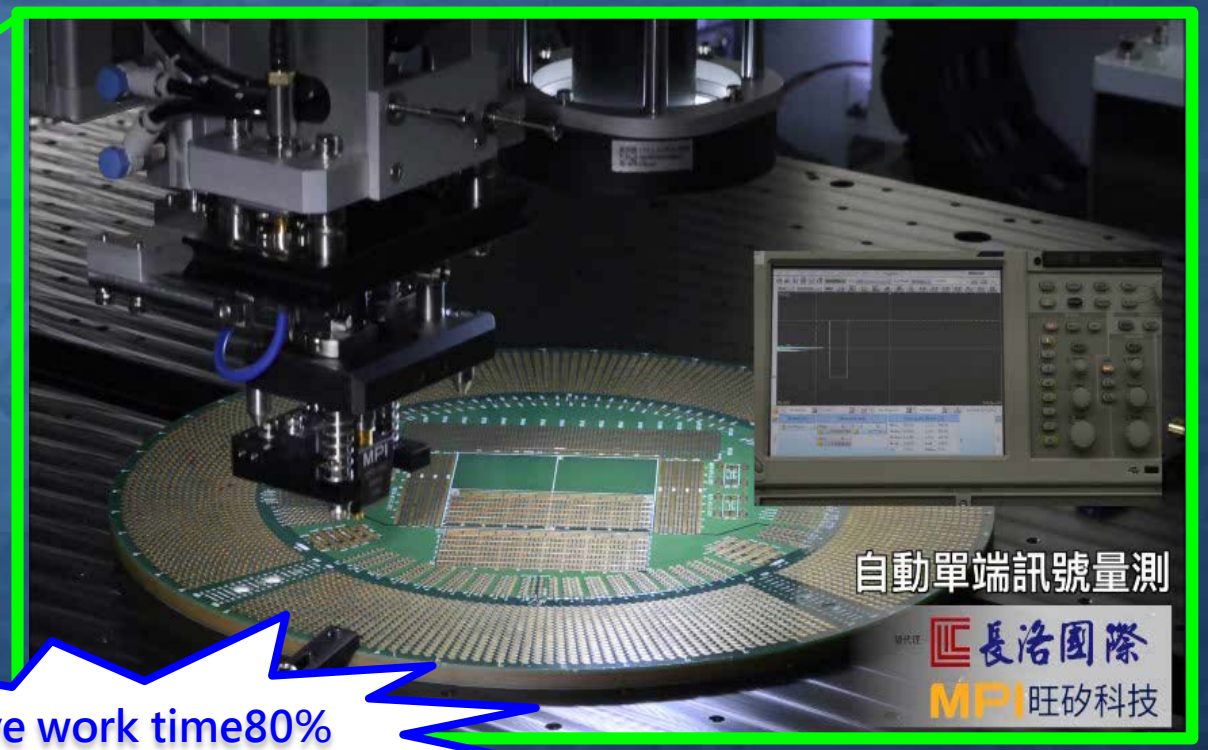


Measuring Capability of TDR Inspection

- Used to check TDR electrical characteristic by manual and randomly and also there does not enough inspection data to complete the analysis. Also, it will take plenty time if doing full inspection.
- We proposes to conduct a comprehensive inspection of TDR electrical characteristic data through semi-automatic TDR testing equipment.







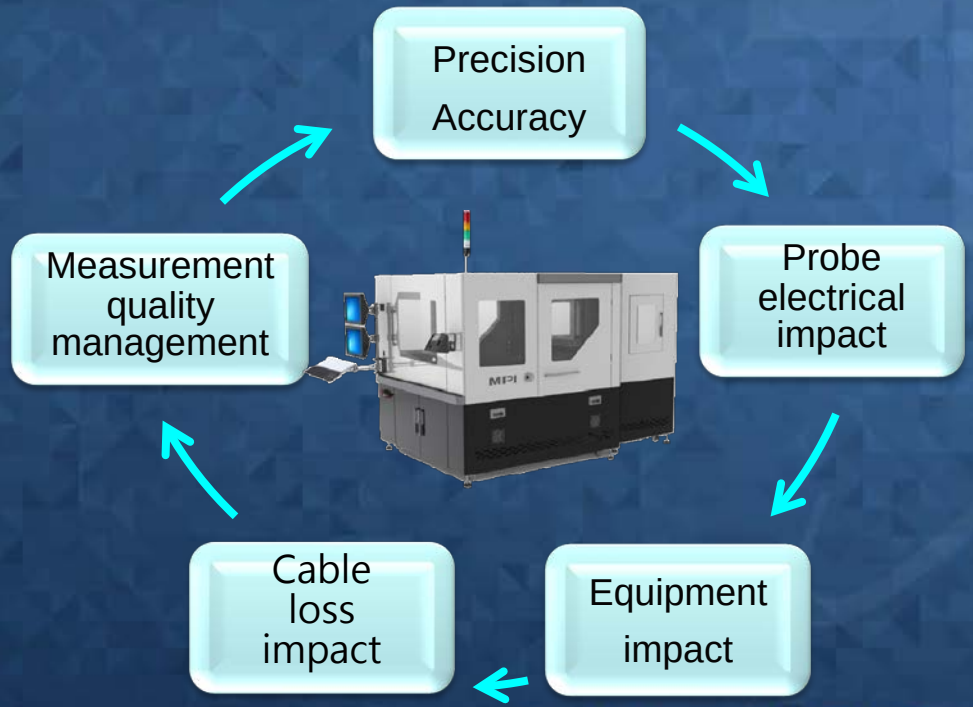
Random inspection
- Long working time
- Lack of data
- Inconsistent quality

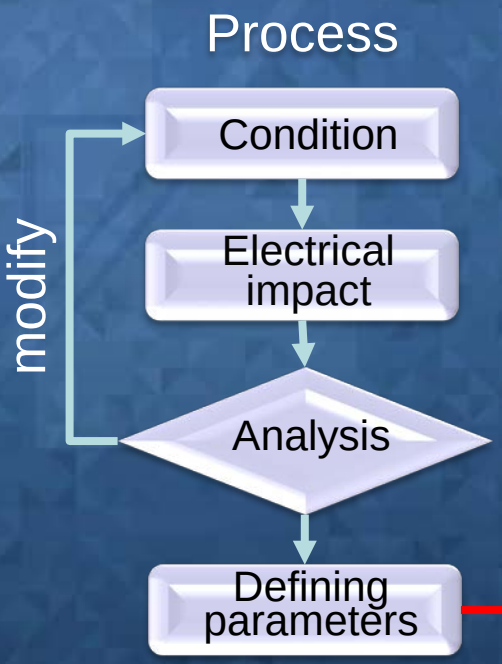
All inspection
- Reduce working time
- Complete data
- Consistent quality

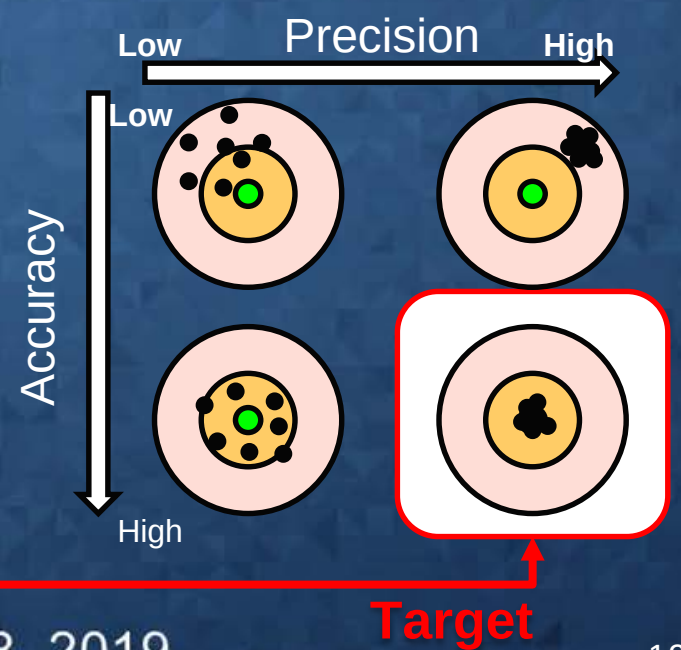
Save work time80%

Measurement System Analysis(MSA)

- The accuracy and precision of measurement are the most concerned specifications for an electrical testing equipment.
- We verify TDR semi-automatic equipment by MSA standard procedure. Using the assumptions of various electrical characteristic variation items, collecting experimental data to find out the influence range, and immediately adjust parameters of the equipment and repeat verification to achieve the range of TDR measurement accuracy and precision of electrical capability target.

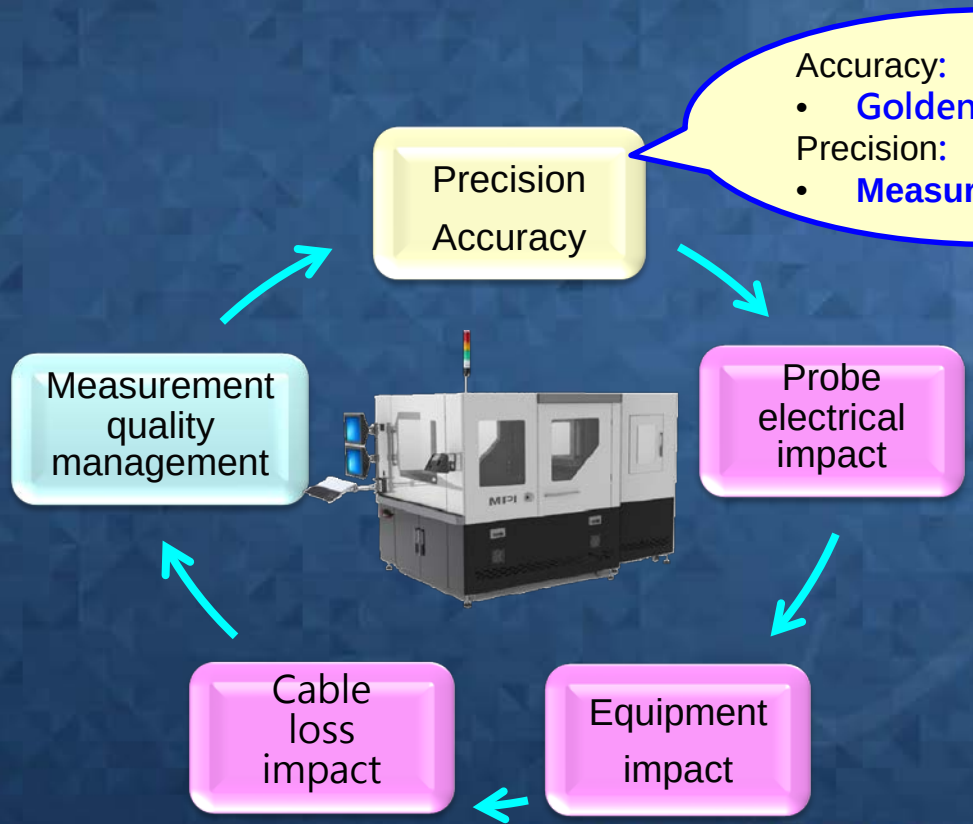


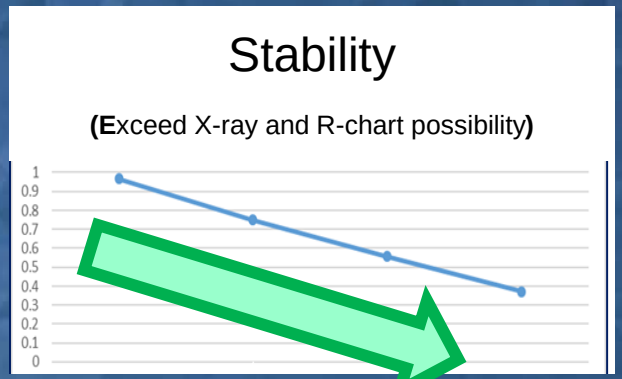


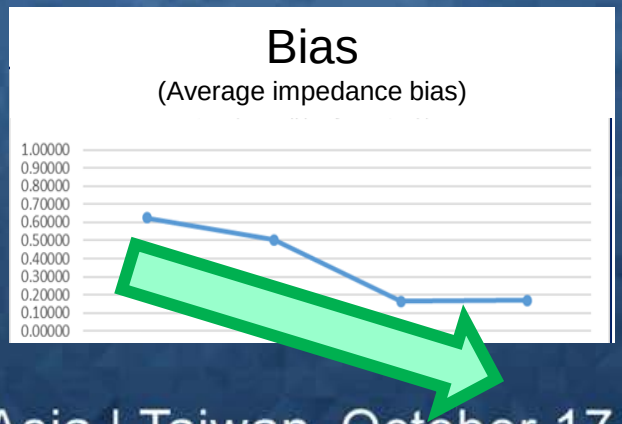


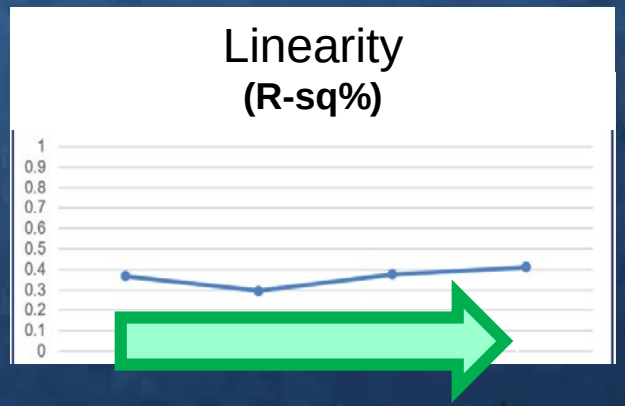
Measurement System Analysis(MSA)

- The adjustment of each variation item by the experimental data in different stage, and finally the TDR testing equipment measurement capability has been verified to meet the measurement error range of the TDR detection instrument.



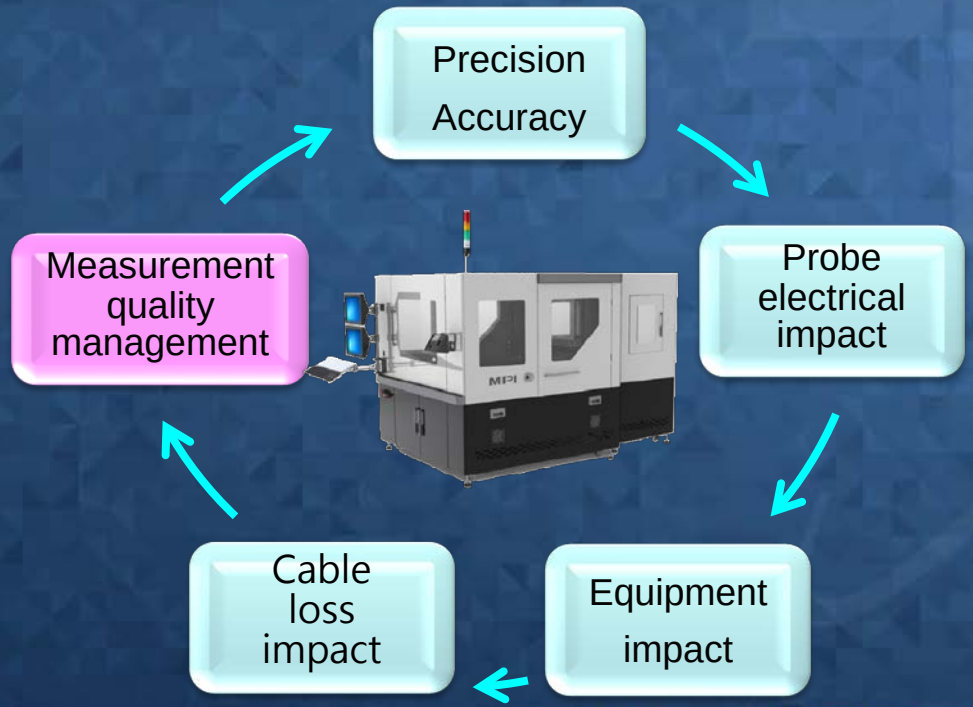


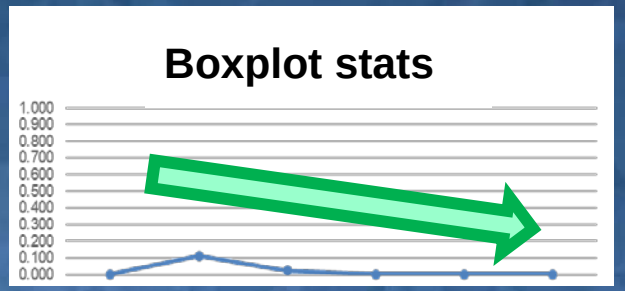


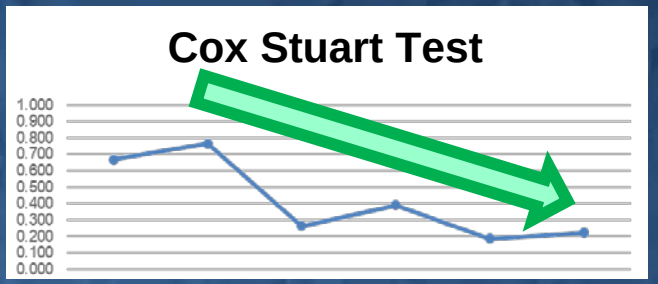


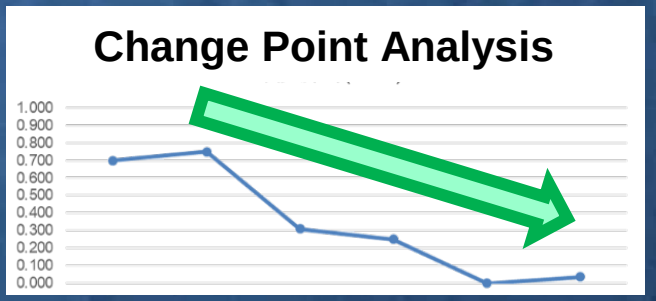
Measurement Quality Monitoring

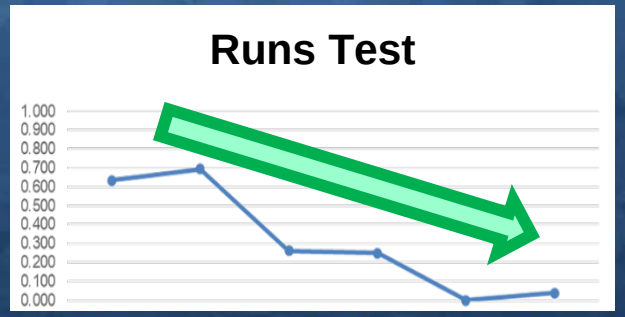
- In the last stage, standard statistical methods are used to monitor the error ratio of each experimental data to perform quality monitoring of semi-automatic testing equipment to ensure measurement quality.

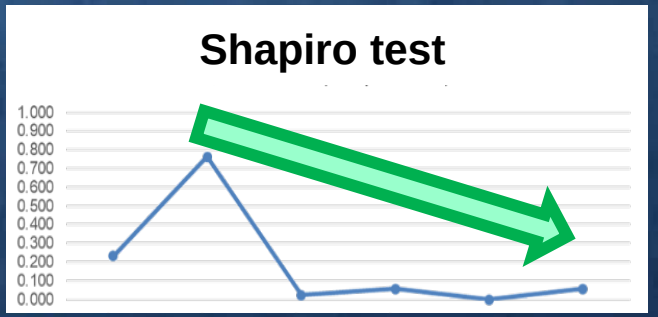






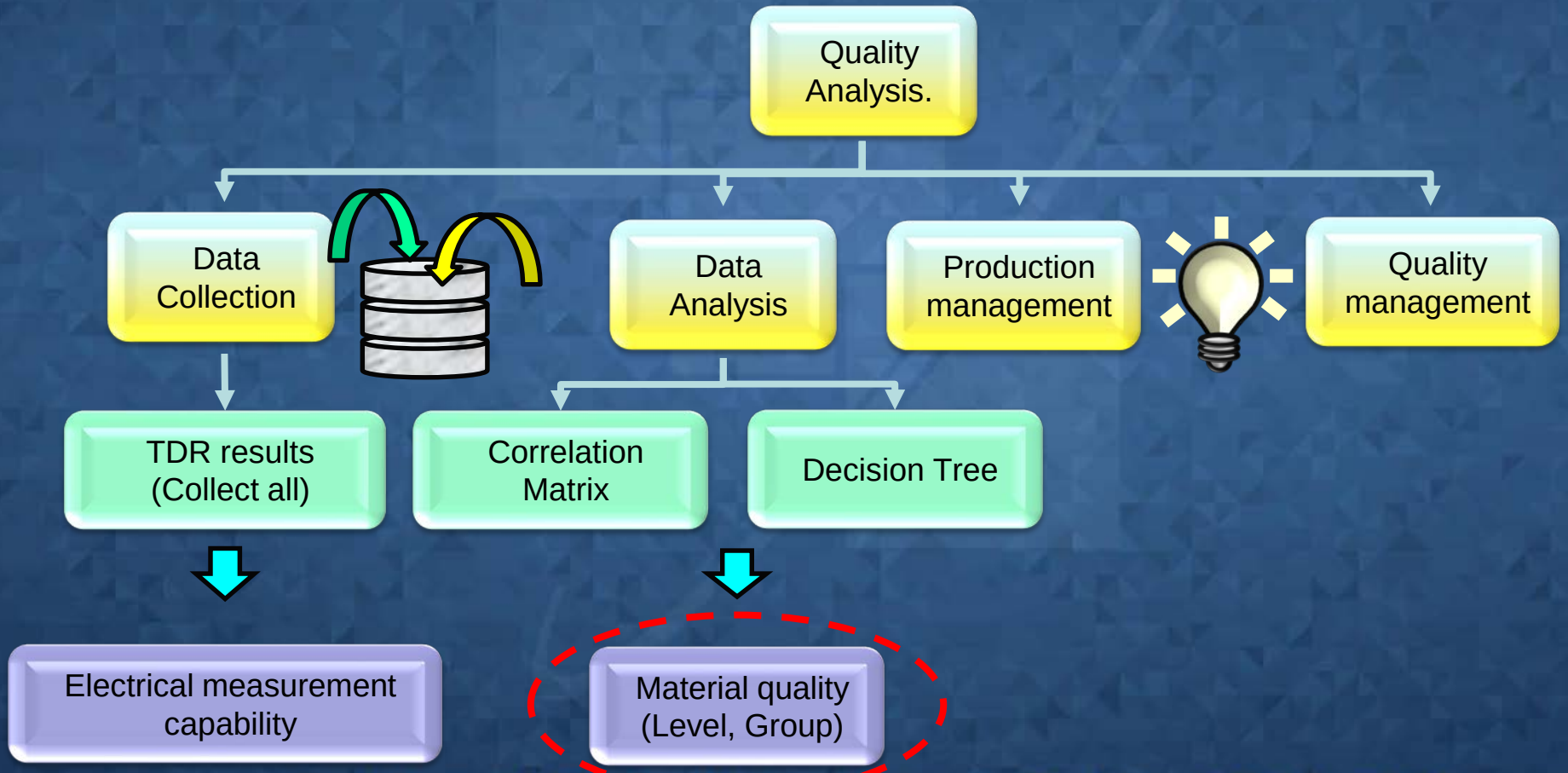






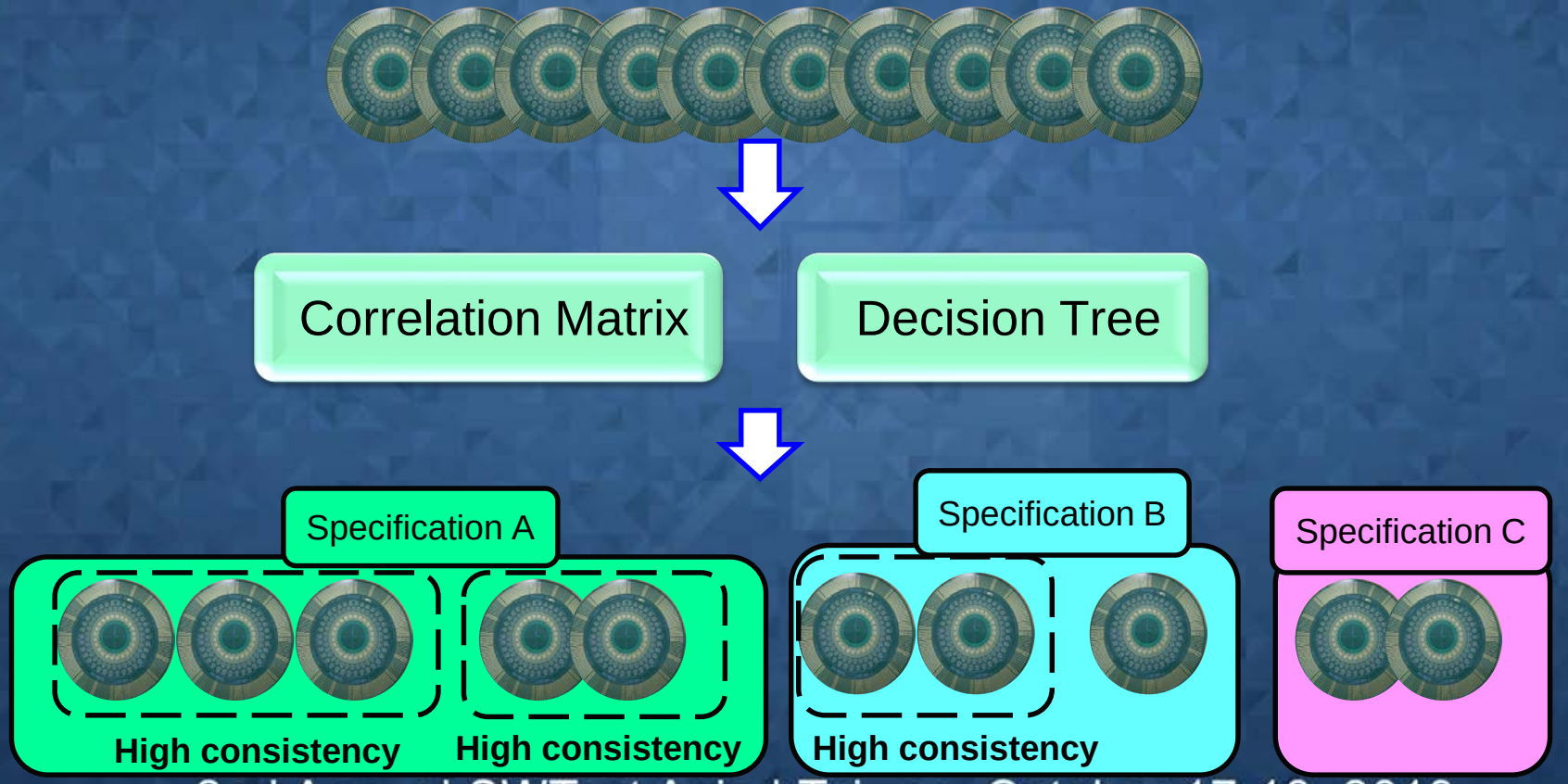
Probe Card Materials Electrical Quality Selecting

- As explained, how does we optimize electrical testing tools and maintain the measure quality. After getting the data, how to analyze and find out the relationship? Let us use data analysis (similarity and decision tree) to filter our materials.



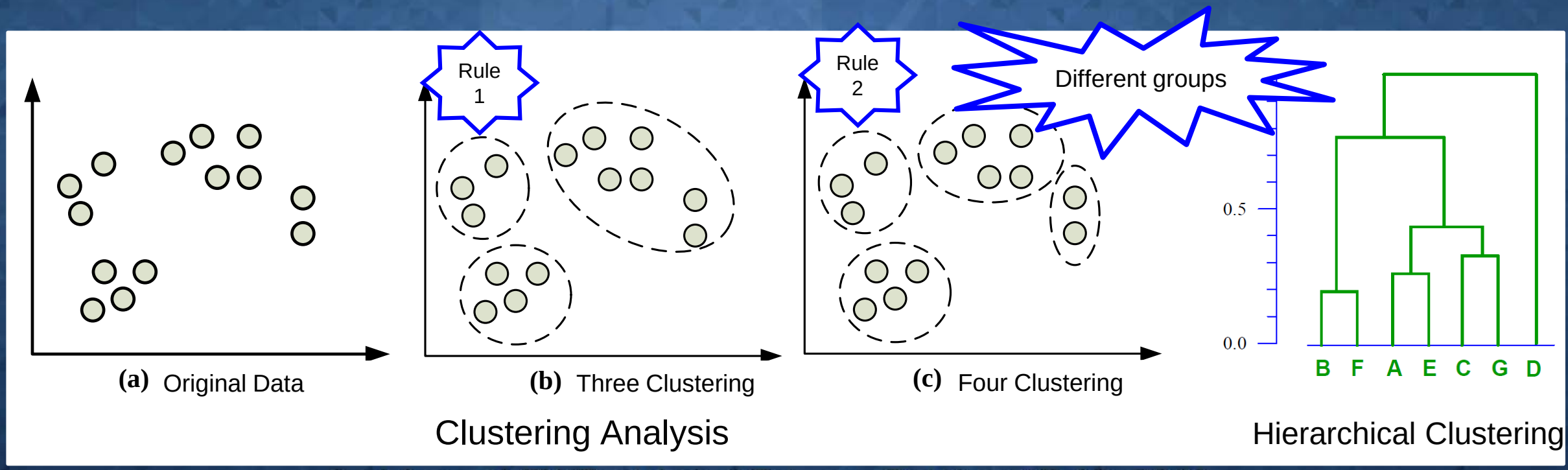
Key Materials Grading and Grouping

- From the material complete inspection data, firstly conduct the general direction quality classification (Spec A ~ Spec B), and then through the data analysis, according to the customer's requirements specifications for material quality grouping; by providing a standard material screening mode to provide more consistent material selection , providing customers with high quality consistent probe card products.



Data Analysis Application

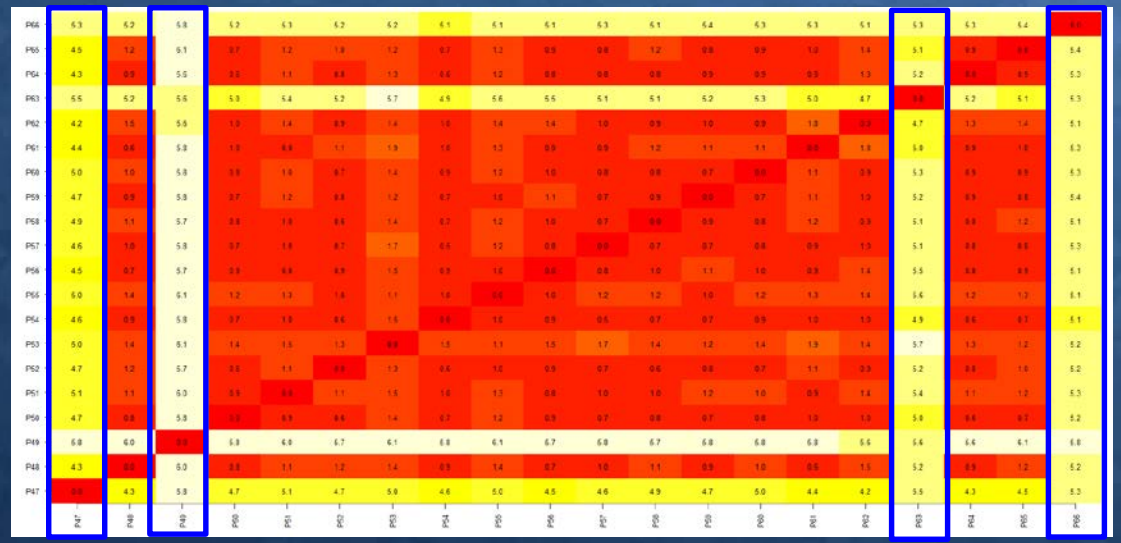
- On data analysis, we use clustered analysis and hierarchical analysis to help us filter our materials from a batch of qualified materials according to well-defined electrical specifications for numerous and complex data.
- Clustering Analysis
  - According to the similarity and dissimilarity to group the data to clusters
- Hierarchical Clustering
  - Each new cluster is split by a cluster of the next level or a cluster of the previous level, like a tree structure.



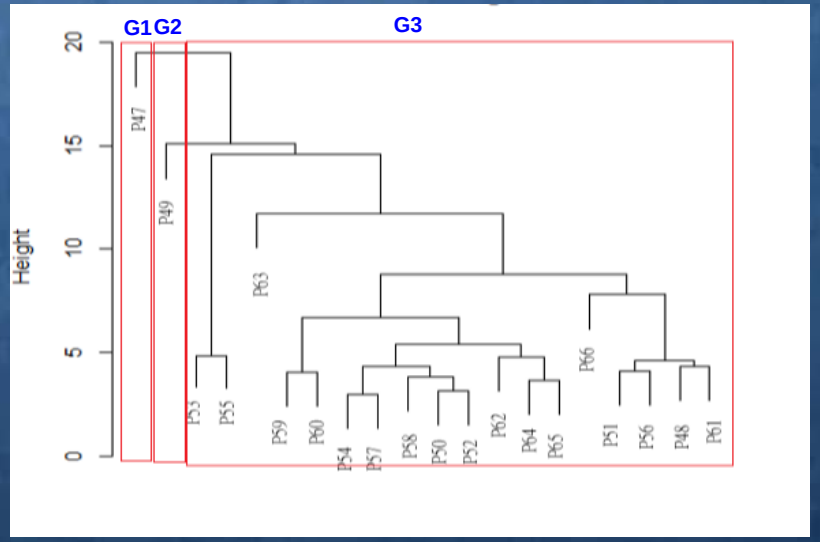
Preliminary Achievement

- Correlation Matrix
  - The difference of electricity between the materials. (small difference=red, big difference=yellow
- Hierarchical Clustering
  - Set electrical specifications (50Ω ± 10%) to provide the best clustering results.
- Decision Tree
  - Group1 grouping rule: Meets Channel 129≥49Ω, also conforms to Channel1≥48Ω
  - Group2 grouping rule: Meets Channel 129≥49Ω,but does not meet Channel1≥48Ω
  - Group3 grouping rule: Does not meet Channel1≥48Ω

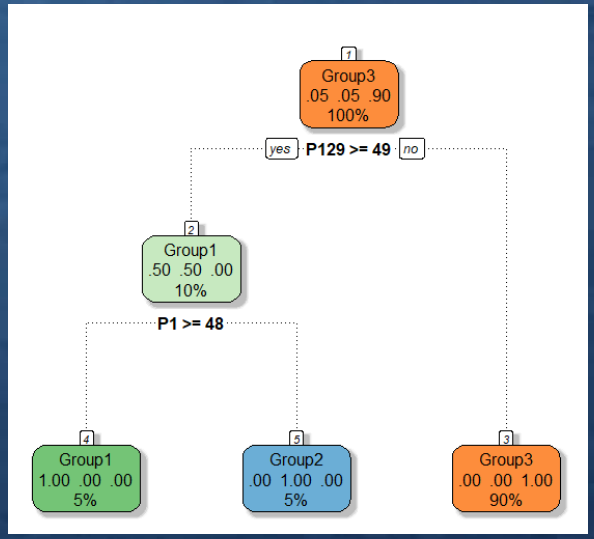
Correlation Matrix



Hierarchical Clustering



Decision Tree



Overview

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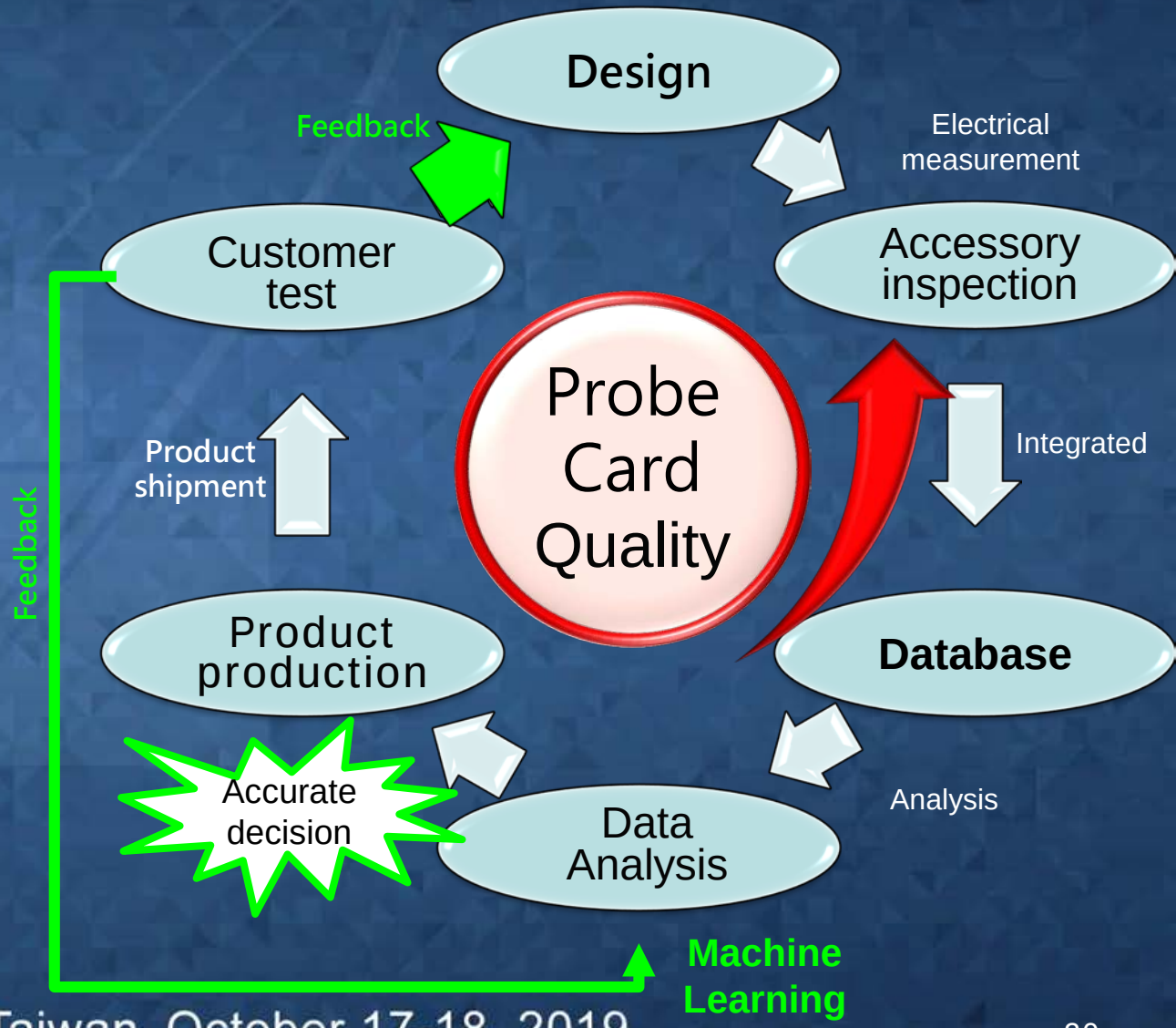
Conclusion

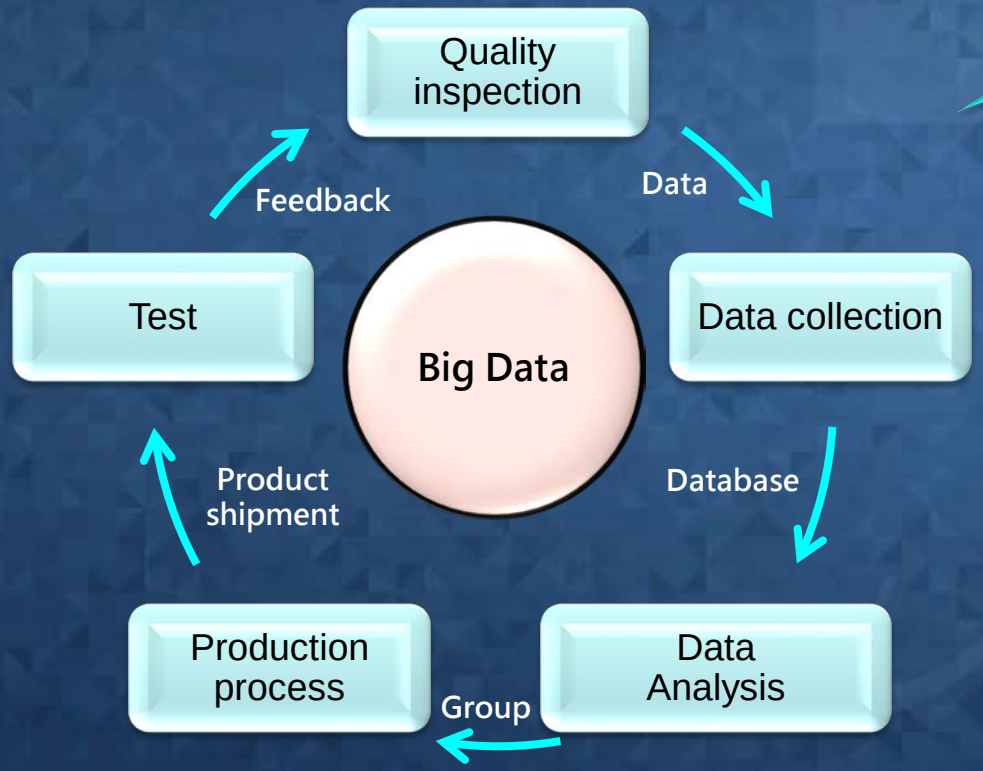
- TDR electrical comprehensive test and add the big data analysis technology to integrate the data to select the quality consistency of key materials to achieve the first step of probe card quality consistency.

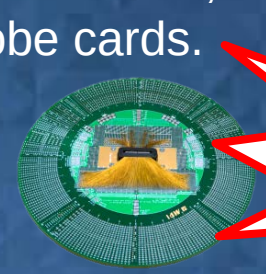
- Next step, through data analysis (similarity analysis, decision number analysis) and customer's feedback could not only improve the high speed specification design technology of MPI. But, let the data analysis system continue to learn repeatedly, providing proper analysis results and process recommendations to well-done the goal of production process monitoring and consistent quality to have probe card meet customer's requirement.



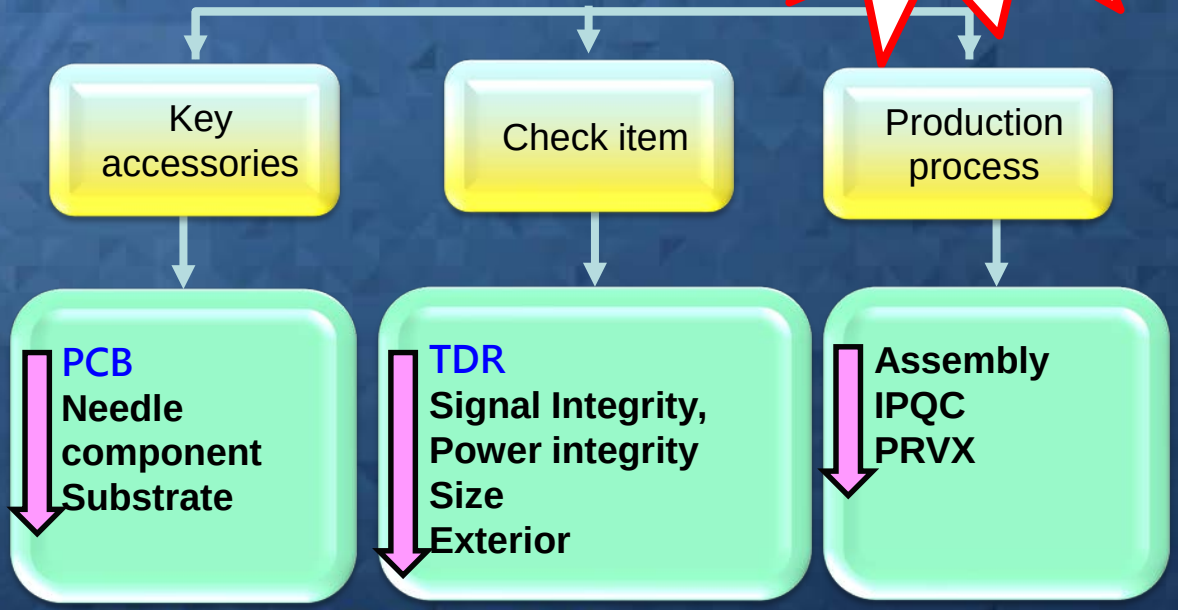
Follow-On Work

- Data Analysis Mode → Build up Standard Quality Process
- Apply the standard data analysis mode on probe card production process from key material inspection, manufacturing process differentiation, shipment inspection and customers' feedback, conduct process integration and repeated learning in order to provide consistent and quality probe cards.





Probe card consistent



Acknowledgment

Special Thanks to:

Alex Yang、Samson Tang、Jason Ho、Derrick Wang、Gary Tsai、Woods Chiang、Kimi Yu、David Yeh、Lily Liu、Morgan Ku、Mark Sun

Helen Fu、Christine Liu、Jeffrey Hu

Questions

SWTEST ASIA 2019

Testing the Spatial Pattern Randomness on Wafer Maps

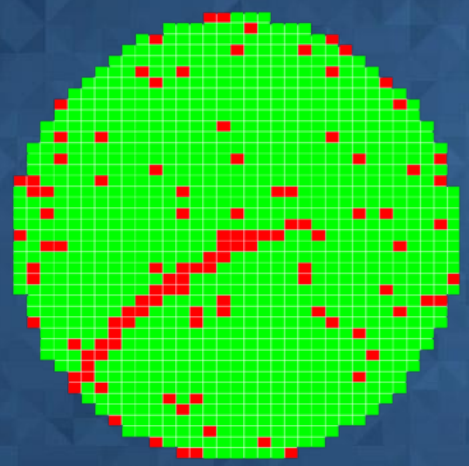
Prof. Jwu-E Chen,
Tung-Ying Lu
National Central University

Prof. Hsing-Chung Liang
Chung Yuan Christian University

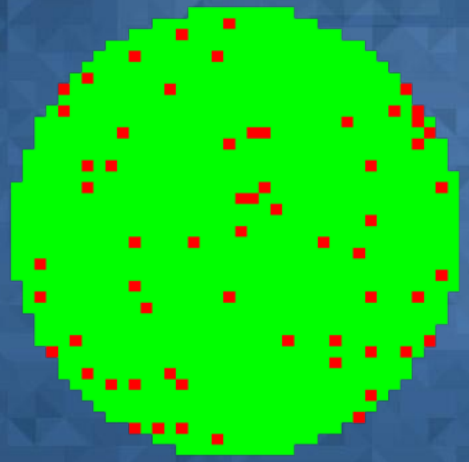
Hsinchu, Taiwan, October 17-18, 2019

Are These Random?

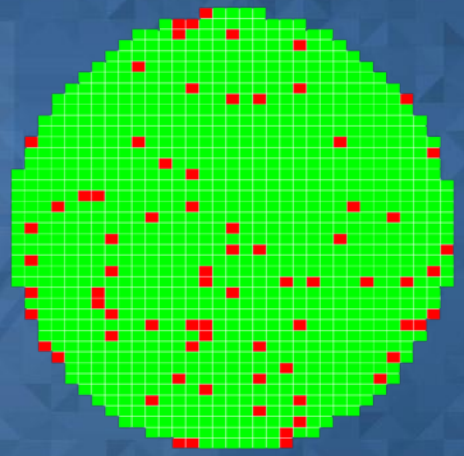
Local defect +
Global defect



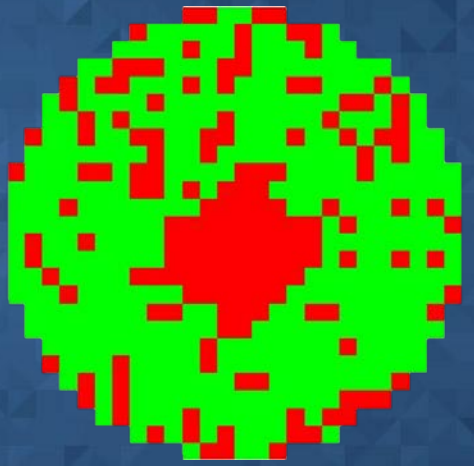
Global defect



Global defect



Local defect +
Global defect



How to classify which are random or non-random?

Outline

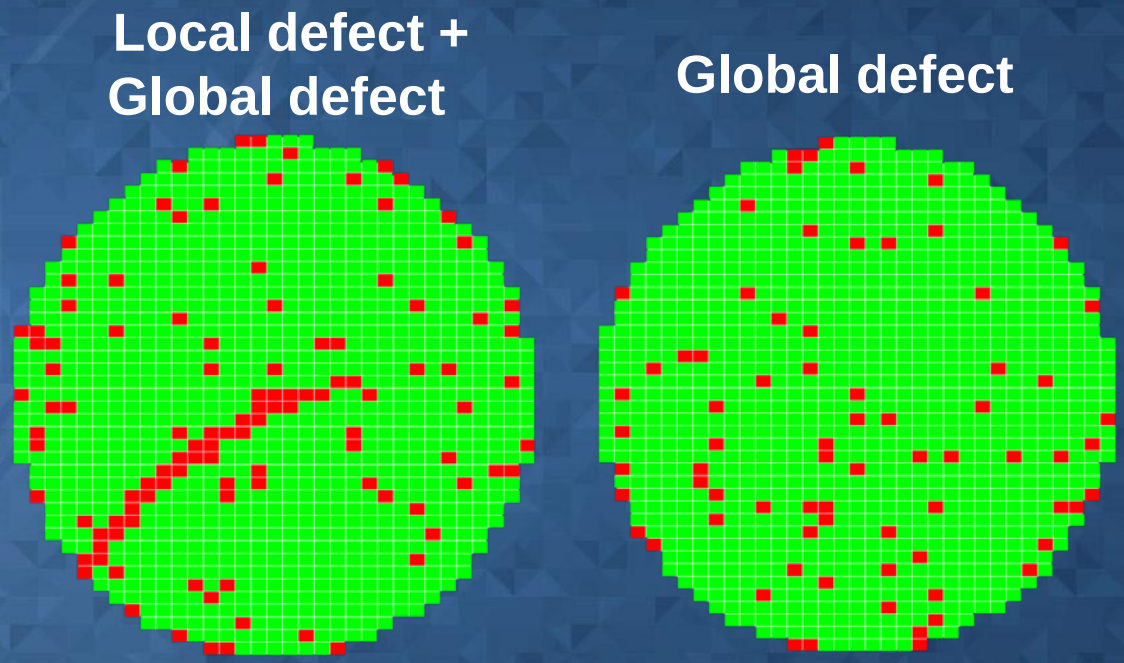
- Introduction
- B-score Transformation and Randomness Definition
- Hypothesis Tests
- Experimental Results of Randomness Test
- Conclusion

Outline

- **Introduction**
  - Global Defect and Local Defect
  - Defect Detection Method
- **B-score Transformation and Randomness Definition**
- **Hypothesis Tests**
- **Experimental Results of Randomness Test**
- **Conclusion**

Global Defect and Local Defect

- **Goal of wafer map analysis**
  - failure root cause determination
  - design-process sensitivities
  - cost-effective defect isolation
- **Local defect**
  - obvious patterns
  - possible causes
- **Global defect**
  - scatter over the whole wafer
  - difficult to address



Defect Detection Method

- **Previous work for local defect detection**
  - yield improvement by test error cancellation [2]
  - features extracted from wafer maps for using pattern recognition [4]
  - wafer map defect pattern classification and image retrieval using convolutional neural networks [7]

- **In our work for global defect detection**
  - test the spatial pattern of a wafer map from a randomness perspective
  - use a standard score to evaluate global and local defect

Outline

- Introduction
- B-score Transformation and Randomness Definition
  - Parameter Extraction
  - Boomerangs Chart
  - B-score Definition
  - Wafer Map Randomness
- Hypothesis Tests
- Experimental Results of Randomness Test
- Conclusion

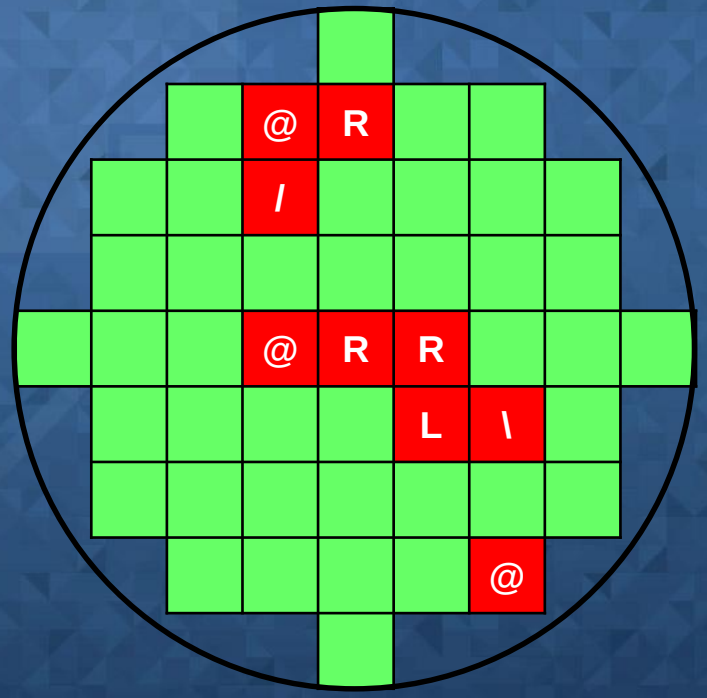
Parameter Extraction

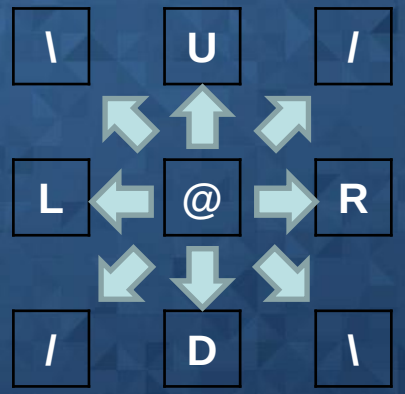
- **BD**
  - the normalized number of Bad Dice
- **CL**
  - the normalized number of Contiguous Lines covering the bad dice

DieSize: 49

Search direction	(NBD, NCL)
@ R /	(3,2)
@ R R \ L	(5,3)
@	(1,1)
Total	(9,6)

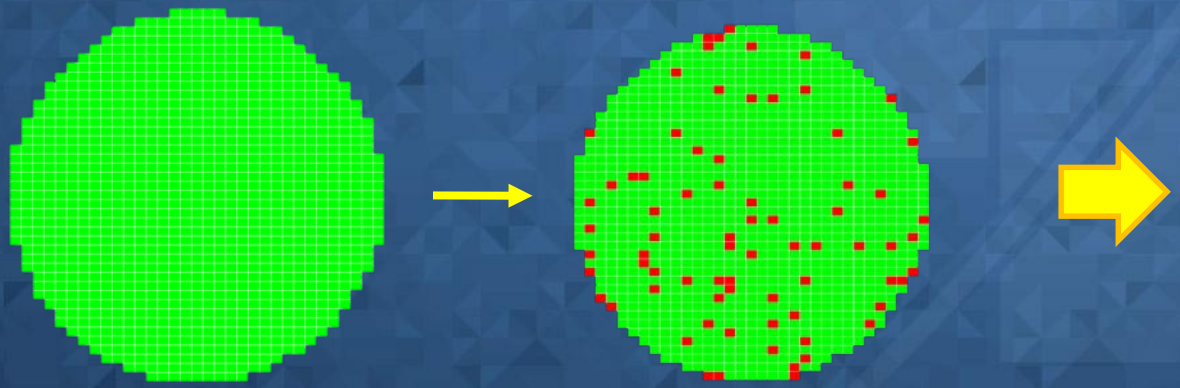
➡ (BD, CL) = (9/49, 6/49)

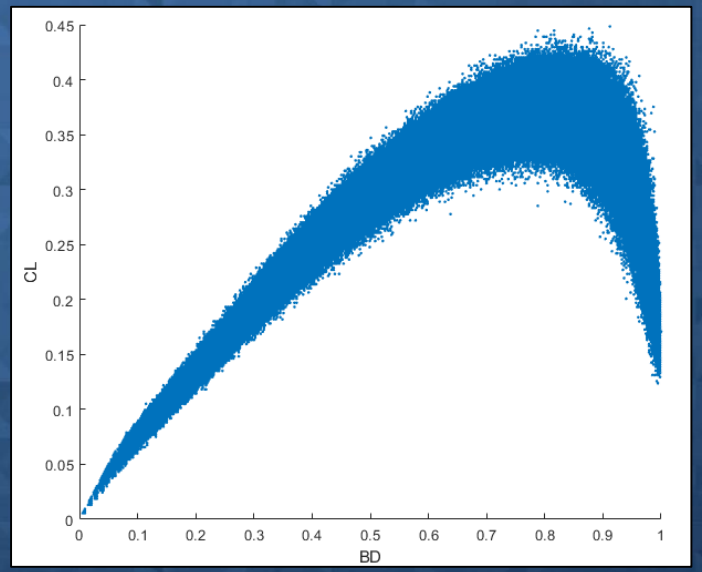




Boomerangs Chart

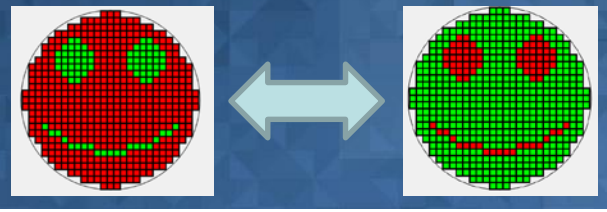
- **Random spread defect**
- **Large amount simulated data**
  - according to different BD

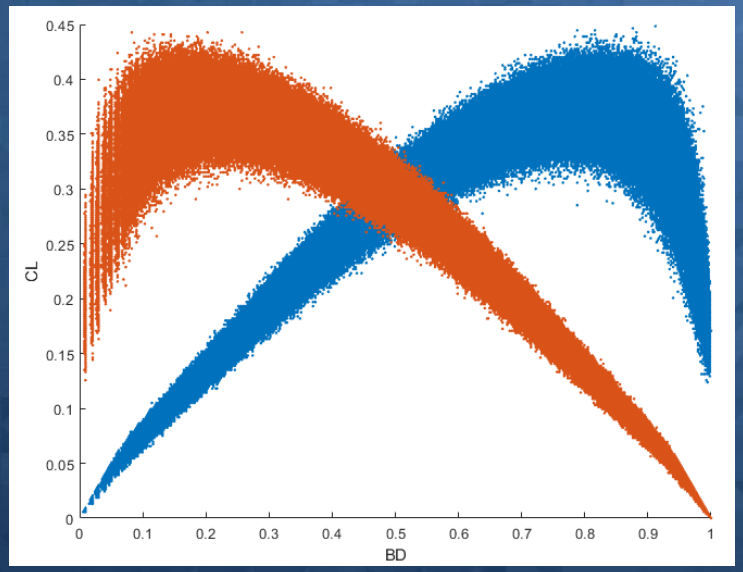




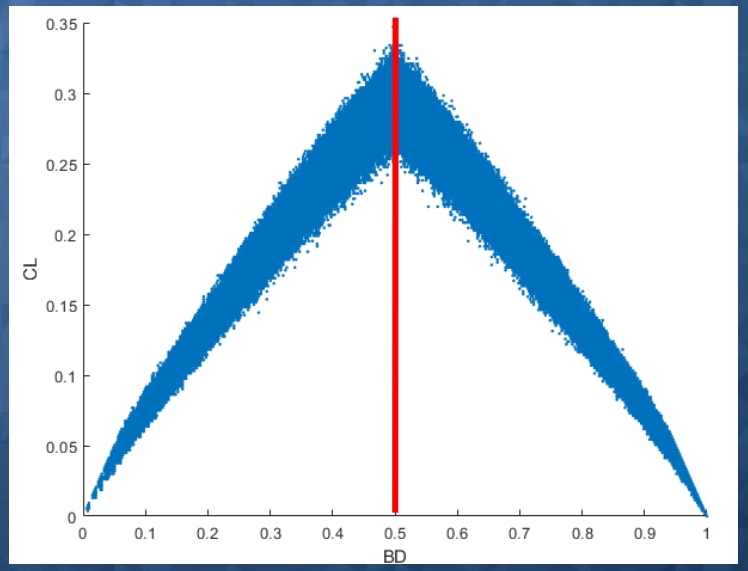
Boomerangs Chart

- **Symbiotic**
  - Only discuss bad die
  - Only discuss good die



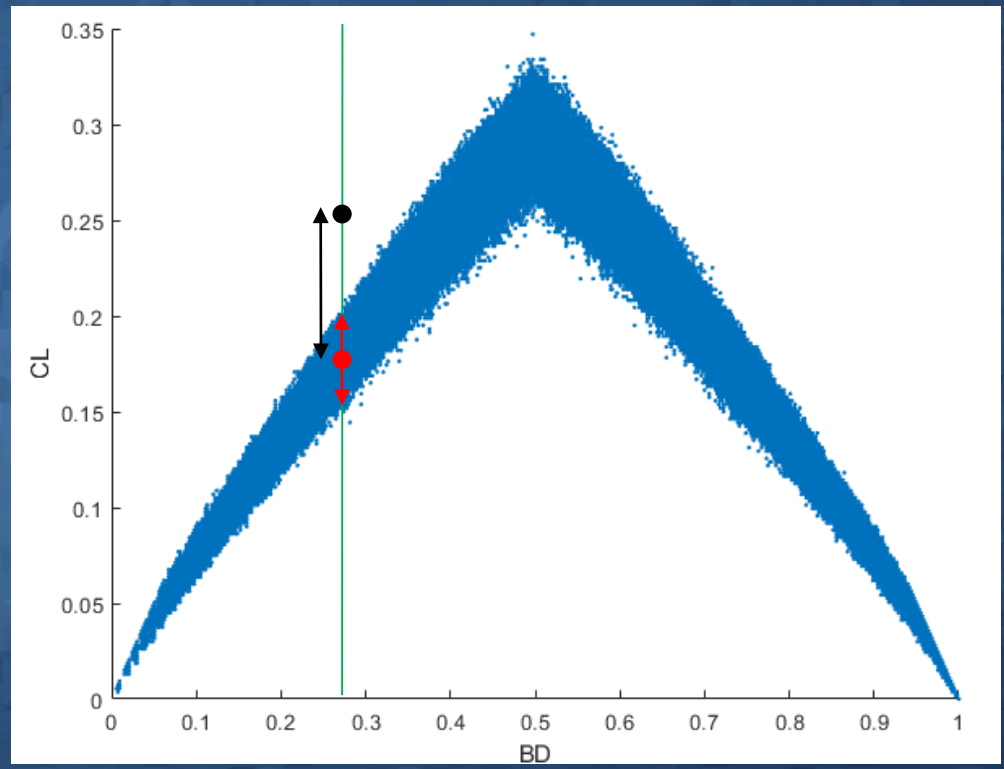


- **BD<0.5**
  - discuss bad die
- **BD≥0.5**
  - discuss good die



B-score Definition

- **Transformation into B-score**
  - B-score = (μ-CL) / σ
    - μ is the mean of CL
    - σ is the standard deviation of CL
  - B-score
    - the standard score of CL
    - evaluate the randomness of spatial pattern

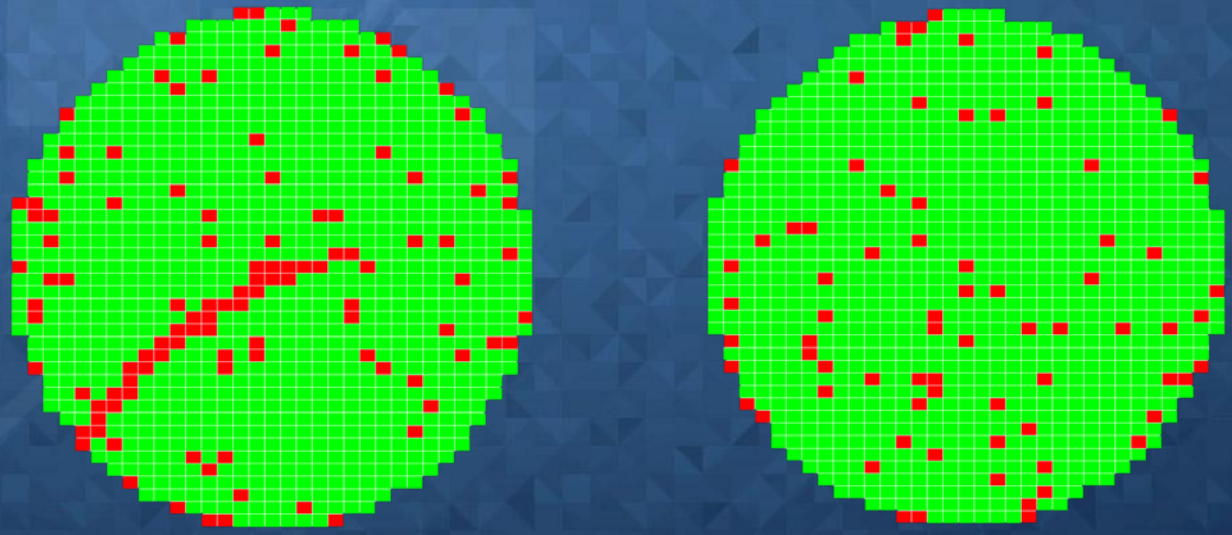


Wafer Map Randomness

- **The randomness of spatial pattern**
  - Spatial pattern of a wafer map
    - the regular arrangement of individual bipartite chips in a circle and the geographic relationships among them
  - Randomness of spatial pattern
    - the possibility of the appearance of the spatial pattern of a wafer map attacked by random point defects

Wafer Map Randomness

- **B-score meaning for the randomness of spatial pattern**
  - the absolute value of B-score larger
    - lower probability to get these spatial pattern
    - less randomness
  - the absolute value of B-score smaller
    - higher probability to get these spatial pattern
    - more randomness



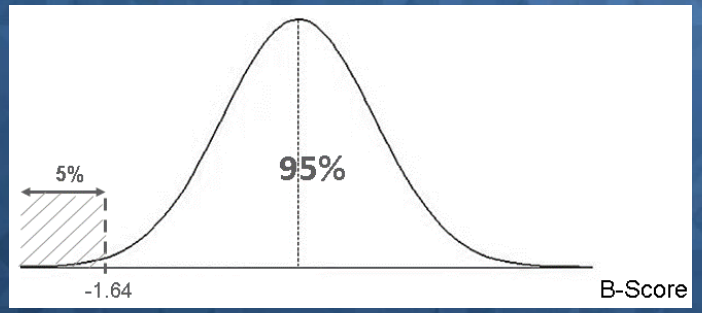
Outline

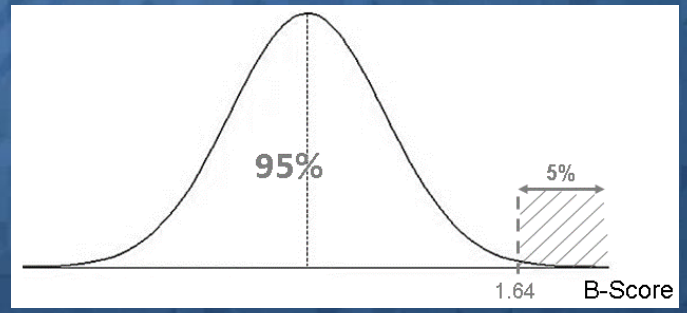
- Introduction
- B-score Transformation and Randomness Definition
- **Hypothesis Tests**
  - 3Ha Hypothesis Tests
  - Gateway Test Diagram for Standard Normal
- Experimental Results of Randomness Test
- Conclusion

3Ha Hypothesis Tests

- **Null hypothesis H0**
  - assume the defects of whole wafer are homogeneously distributed
  - complete spatial randomness (CSR)

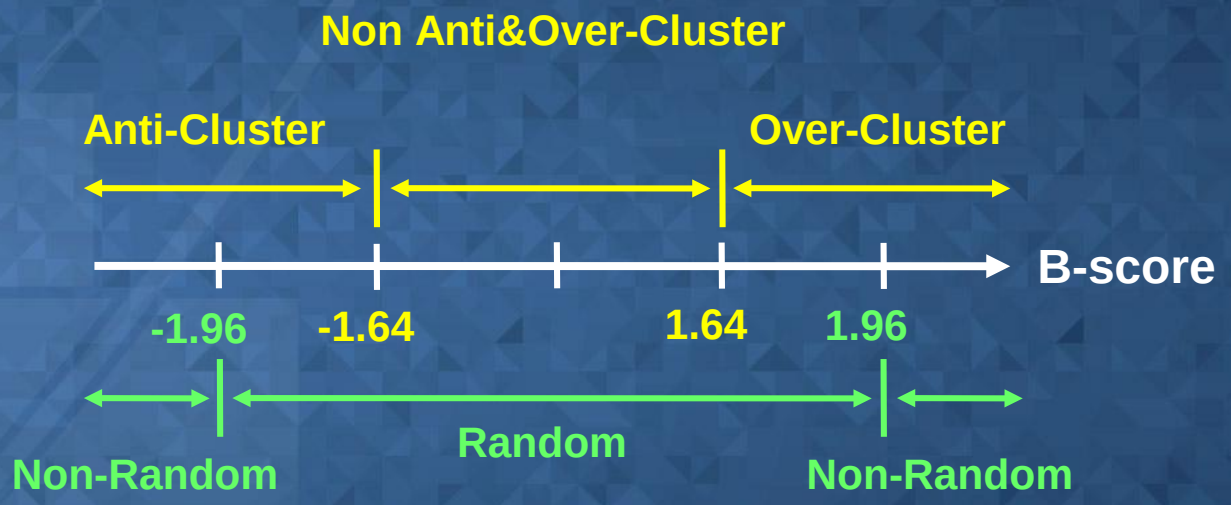
- **Significance level: 5%**





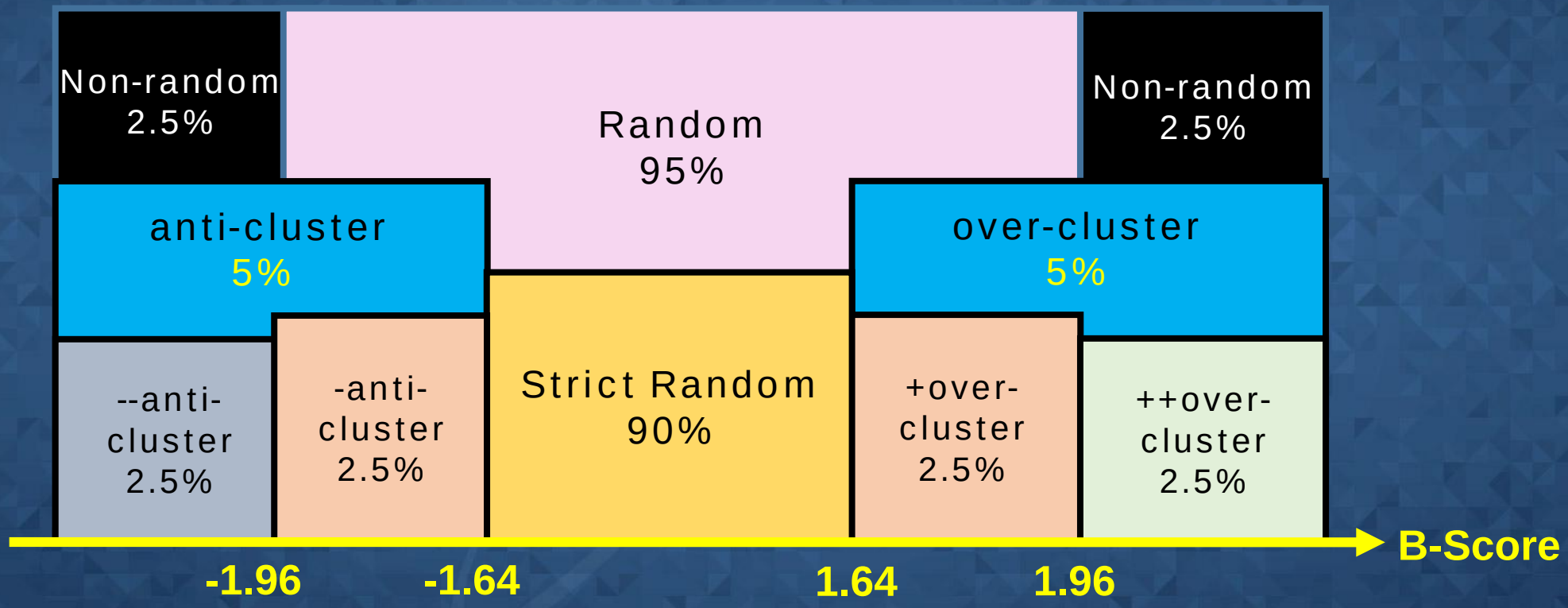
3Ha Hypothesis Tests

- **Alternative hypothesis**
  - Ha_OC
    - Is it over-cluster?
    - B-score > 1.64 → Over-Cluster
  - Ha_AC
    - Is it anti-cluster?
    - B-score < -1.64 → Anti-Cluster
  - Ha_NR
    - Is it non-random?
    - |B-score| > 1.96 → Non-Random



Gateway Test Diagram for Standard Normal

- **Non-Random, Over-Cluster and Anti-Cluster all are 5%**



Outline

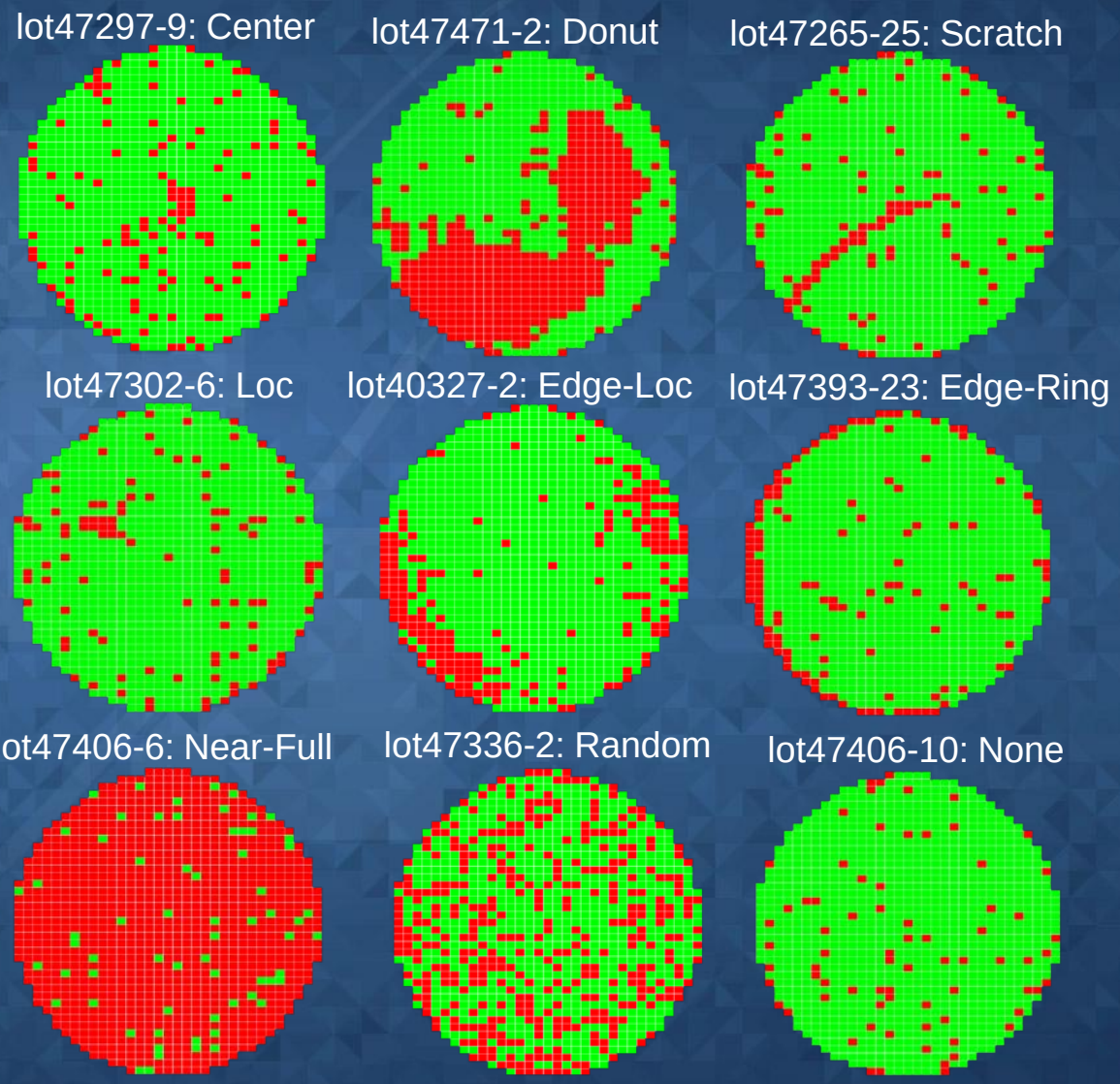
- Introduction
- B-score Transformation and Randomness Definition
- Hypothesis Tests
- **Experimental Results of Randomness Test**
  - WM-811K Benchmark
  - Gateway Test Diagrams
  - Randomness Test for Failure Types
  - B-score Case
- Conclusion

WM-811K Benchmark

- **WM-811K**
  - provide from TSMC
  - nine failure patterns
  - 811,457 wafer maps
    - 172,950 labeled wafer maps
    - 638,507 un-labeled wafer maps

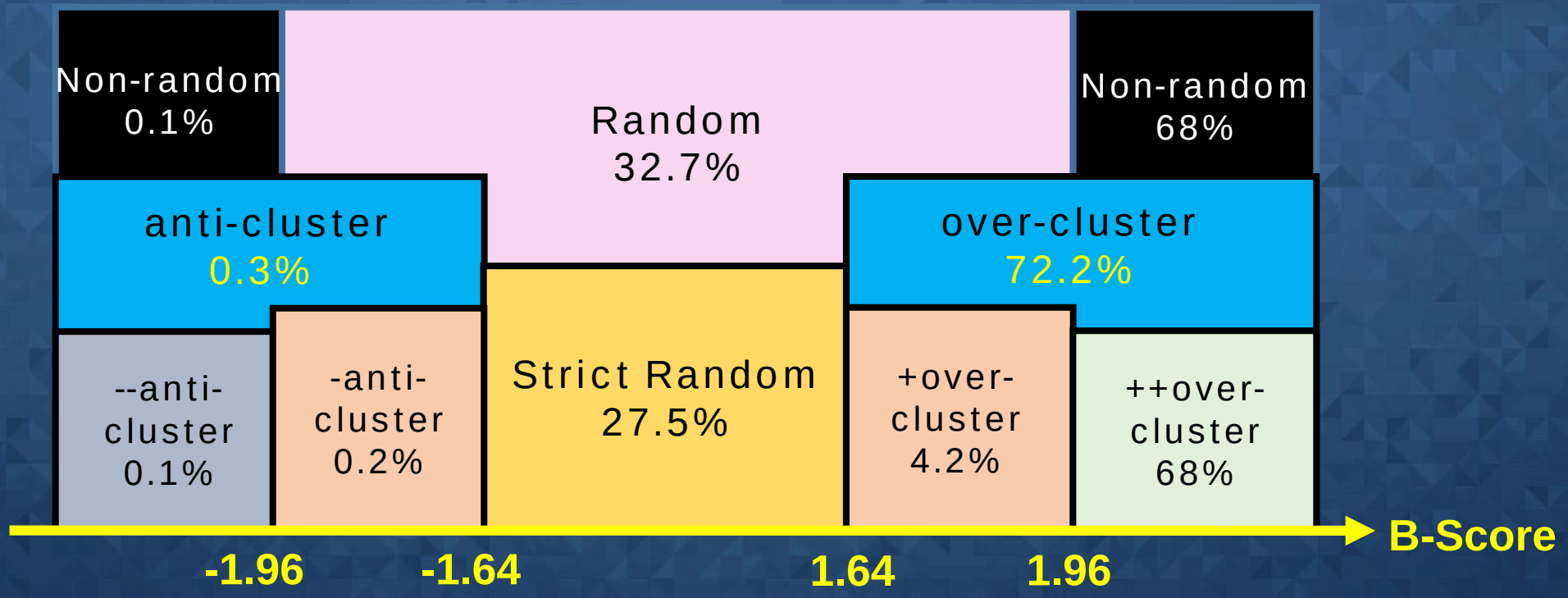
WM-811K Failure Pattern

- **Symptomatic**
  - Center
  - Donut
  - Scratch
  - Loc
  - Edge-Loc
  - Edge-Ring
- **Non-Symptomatic**
  - Near-Full
  - Random
  - None



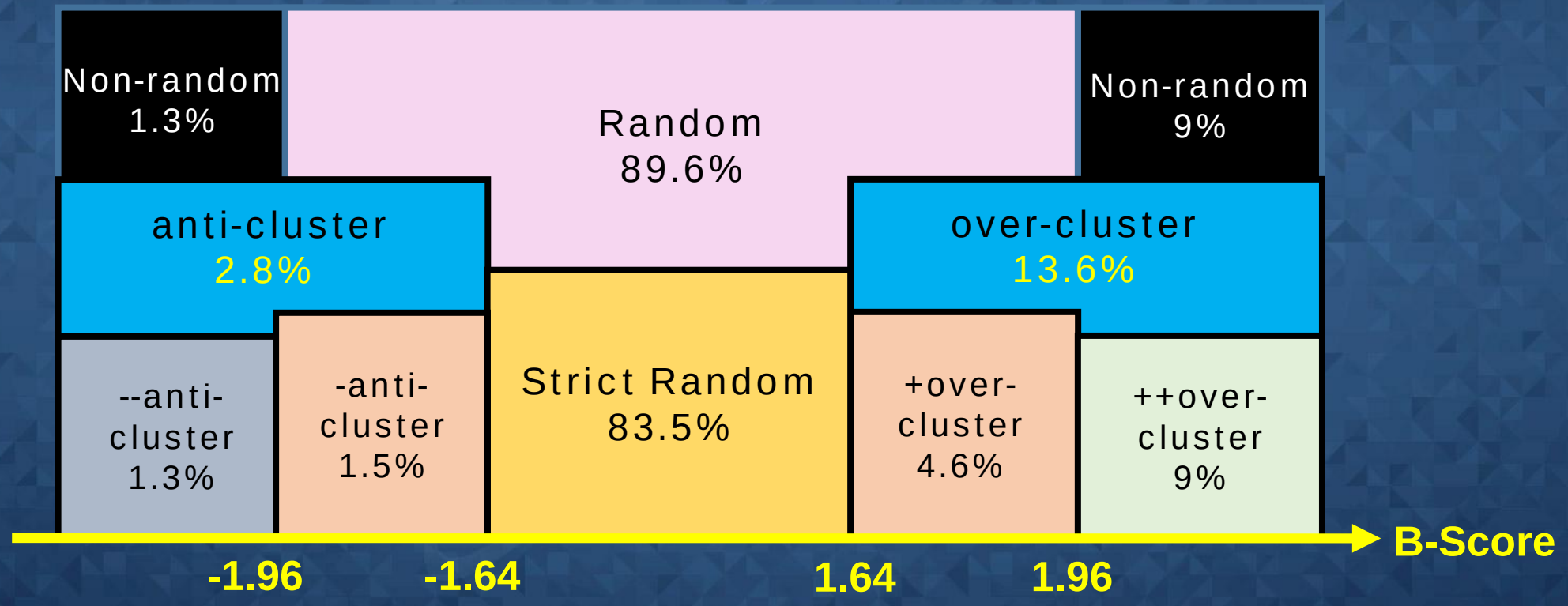
Gateway Test Diagrams for Symptomatic

- **For symptomatic wafer maps**
  - 72.2% classified as Over-Cluster
  - 27.5% classified as non-Over&Anti-Cluster
  - 0.3% classified as Anti-Cluster



Gateway Test Diagrams for Non-Symptomatic

- **For non-symptomatic wafer maps**
  - 89.6% classified as Random
  - 10.3% classified as Non-Random



Randomness Test for Failure Types

- **Ha_AC test**
- **Ha_OC test**

	anti-cluster	non-anti& over-cluster	over-cluster	Total
Center	26 (0.6%)	2461 (57.3%)	1807 (42.1%)	4294
Donut	1 (0.2%)	80 (14.4%)	474 (85.4%)	555
Scratch	5 (0.4%)	376 (31.5%)	812 (68.1%)	1193
Edge-Ring	3 (0%)	316 (3.3%)	9361 (96.7%)	9680
Edge-Loc	8 (0.2%)	1920 (37%)	3261 (62.8%)	5189
Loc	33 (0.9%)	1574 (43.8%)	1986 (55.3%)	3593
Random	7 (0.8%)	520 (60%)	339 (39.1%)	866
Near-full	14 (9.4%)	61 (40.9%)	74 (49.7%)	149
none	4154 (2.8%)	123422 (83.7%)	19855 (13.5%)	147431

Randomness Test for Failure Types

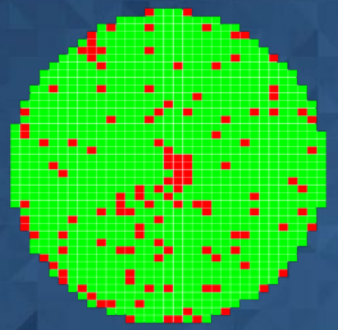
- **Ha_NR test**

	random	non-random	Total
Center	2772 (64.6%)	1522 (35.4%)	4294
Donut	95 (17.1%)	460 (82.9%)	555
Scratch	458 (38.4%)	735 (61.6%)	1193
Edge-Ring	420 (4.3%)	9260 (95.7%)	9680
Edge-Loc	2252 (43.4%)	2937 (56.6%)	5189
Loc	1799 (50.1%)	1794 (49.9%)	3593
Random	592 (68.4%)	274 (31.6%)	866
Near-full	65 (43.6%)	84 (56.4%)	149
none	132495 (89.9%)	14936 (10.1%)	147431

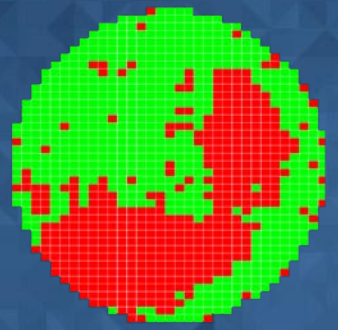
B-score Case for Nine Failure Pattern

- **Symptomatic**

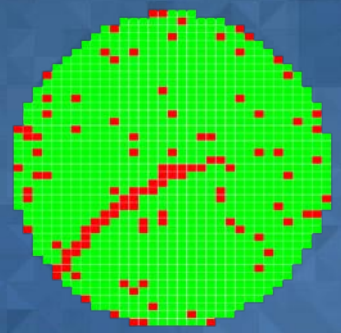
Center
B-score=0.64



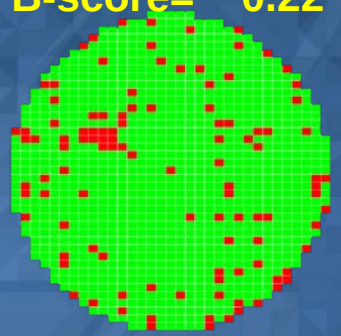
Donut
B-score=14.17



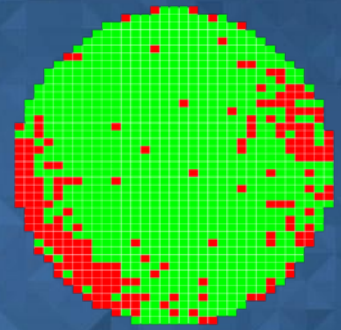
Scratch
B-score=1.86



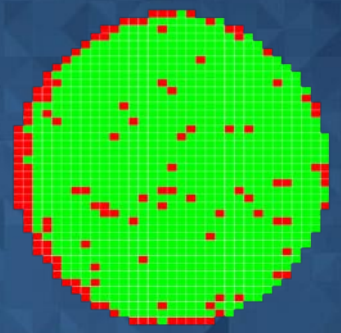
Loc
B-score=−0.22



Edge-Loc
B-score=3.94

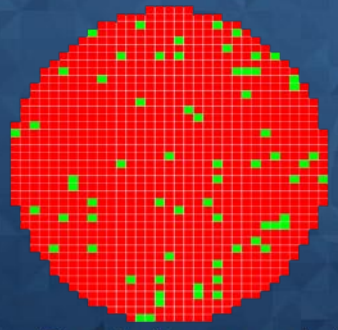


Edge-Ring
B-score=5.36

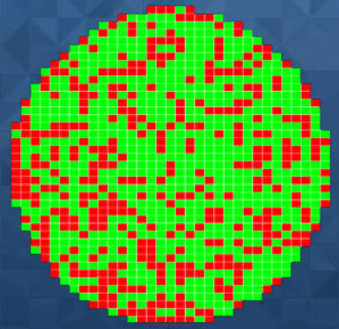


- **Non-Symptomatic**

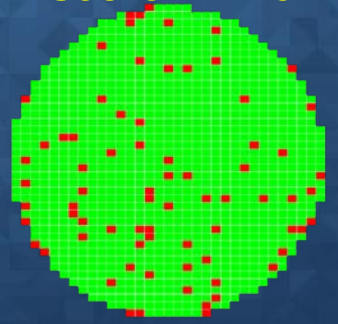
Near-Full
B-score=0.11



Random
B-score=1.19



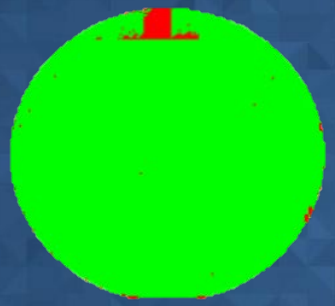
None
Bscore=−1.61



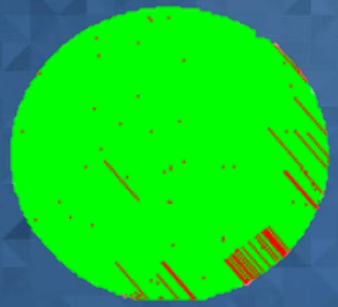
B-score Case - More Positive

- More salient pattern
- Less random defect

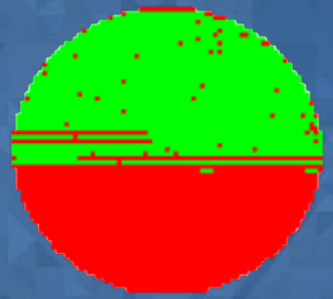
lot15286-13
B-core=66



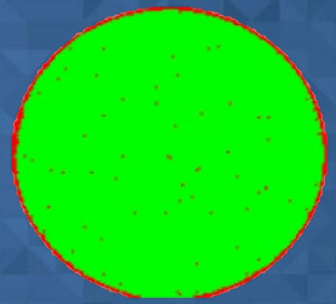
lot16703-14
B-core=60



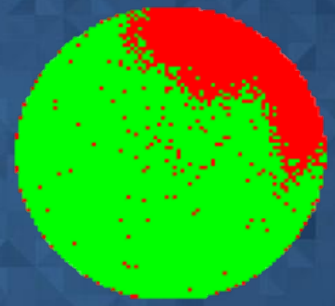
lot15865-6
B-core=48



lot15222-5
B-core=46

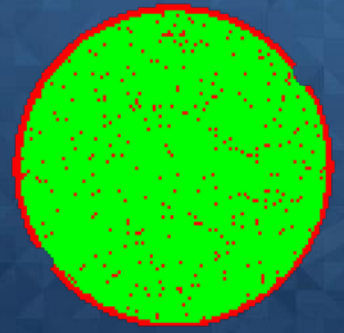


lot14687-24
B-core=39

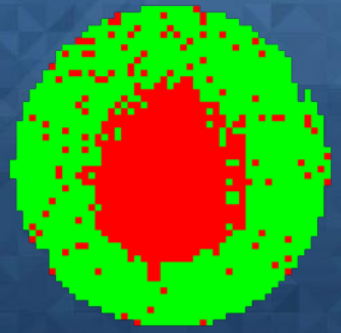


lot1419-23
B-core=33

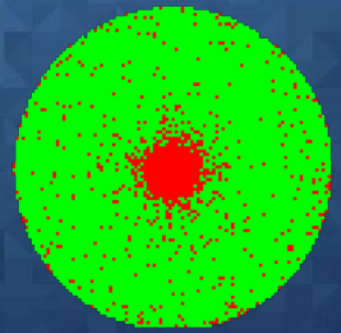
lot15226-5
B-core=25



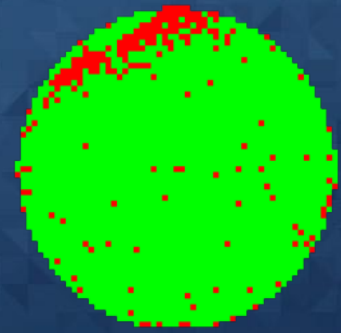
lot15330-7
B-core=18



lot18905-17
B-core=13



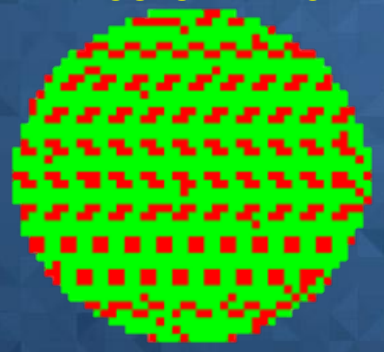
lot23474-5
B-core=7



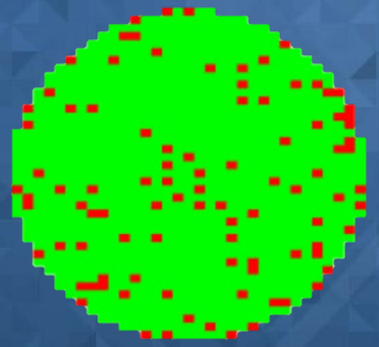
B-score Case - More Negative

- More uniformly distribution

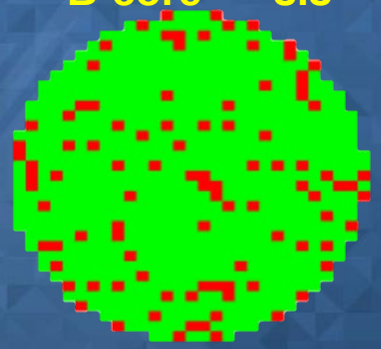
lot46034-12
B-core=－4.6



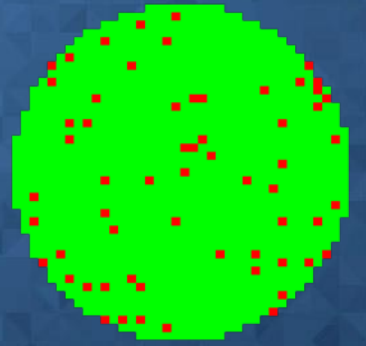
lot47045-15
B-core=－3.6



lot44078-21
B-core=－3.3

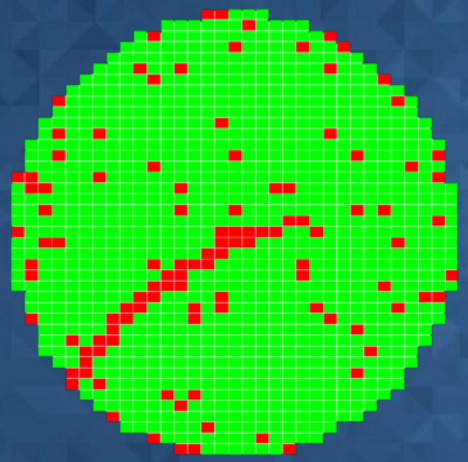


lot42521-1
B-core=－2.4



Are These Random?

Local defect +
Global defect

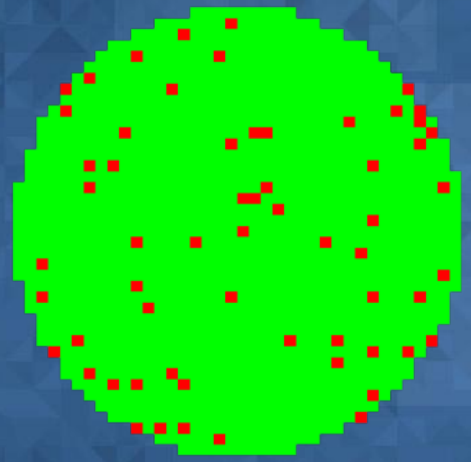


B-score = 1.86

Over-Cluster

Random

Global defect

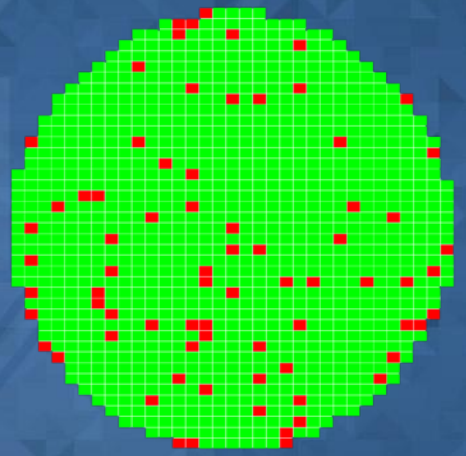


B-score = —2.4

Anti-Cluster

Non-Random

Global defect

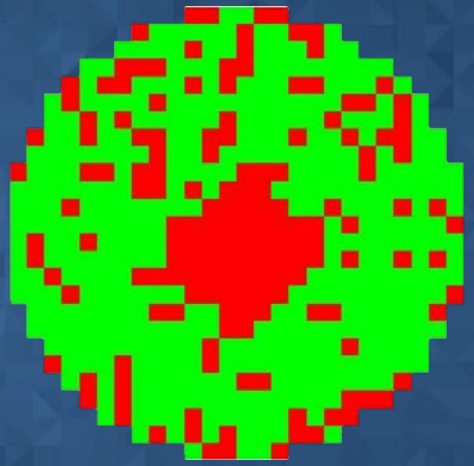


B-score = —1.61

Non-Over&Anti-Cluster

Random

Local defect +
Global defect



B-score = 1.46

Random

Outline

- Introduction
- B-score Transformation and Randomness Definition
- Hypothesis Tests
- Experimental Results of Randomness Test
- Conclusion

Conclusion

- **B-score**
  - use BD and CL to transform into standard score
  - as a classifier to test the wafer-map pattern randomness
  - the absolute value of B-score larger
    - lower probability to get these spatial pattern, less randomness
  - the absolute value of B-score smaller
    - higher probability to get these spatial pattern, more randomness

- **Applied the randomness test in WM-811K**
  - 72.2% in symptomatic classified as over-cluster
  - 89.6% in non-symptomatic classified as random

Reference

[1] International Technology Roadmap for Semiconductors, ITRS 2013
[2] M.J. Wang, J.E Chen, Y.S. Chang, S.C. Shyu, and Y.Y.Chen, “Yield Improvement by Test Error Cancellation”, ATS., pp.258-260, Nov. 1996.
[3] C. - K. Hsu, F. Lin, K. T. Tim Cheng, W. Zhang, X. Li, J. M. Carulli, and K. M Butler., “Test data analytics Exploring spatial and test-item correlations in production test data” Proceedings IEEE Int. Test Conference, pp.1-10, Sep. 2013.
[4] M.J. Wu, J.S. Roger Jang, and J.L. Chen, “Wafer Map Failure Pattern Recognition and Similarity Ranking for Large-scale Datasets”, IEEE Trans. on Semicond. Manuf., vol.28, no.1, pp.1-12, Feb. 2015.
[5] J. Yu and X. Lu, “Wafer Map Defect Detection and Recognition Using Joint Local and Nonlocal Linear Discriminant Analysis,”IEEE Trans. Semicond. Manuf., vol. 29, no. 1,pp. 33–43, Feb. 2016.
[6] M Piao, C-H Jin, J,Y, Lee and J.Y. Byun, “Decision Tree Ensemble-Based Wafer Map Failure Pattern Recognition Based on Radon Transform-Based Features,” IEEE Transactions on Semiconductor Manufacturing, vol.31, no.2, pp.250-257, May 2018.
[7] T. Nakazawa and D. V. Kulkarn, “Wafer Map Defect Pattern Classification and Image Retrieval Using Convolutional Neural Network,”IEEE Trans. Semicond. Manuf., vol. 31, no. 2,pp. 309–314, May 2018.
[8] J. E Chen, C.-H. Gau, W.-Y. Lin, H.-K. Hu and H.-C. Liang, “The Test to Classify the Non-random Pattern on Wafer Maps,” 29th VLSI Design/CAD Symp., 2018.
[9] “Statistical Hypothesis Test”, Wiki, [Online]. Available: https://en.wikipedia.org/wiki/Statistical_hypothesis_testing
[10] Y-S Wu, C-J Lin, J E Chen and H-C Liang, “The Rainbow Transformed from a Set of Uniform-defect Wafer Maps,” Int’l Test Conf., (Poster P05), Oct. 2017.

SWTEST ASIA 2019

Reducing Wafer Parametric Test Costs by High Speed Test Solution

Semitronix

Mark Lu
VP of Sales & Marketing
mark.lu@semitronix.com

Hsinchu, Taiwan, October 17-18, 2019

Thanks to NI, for close collaboration and invitation to this great event

Content

- Technology Roadmap
- Semitronix Solutions Profile
- Fast Testing Portfolio
- Summary

Content

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Technology & product roadmap---Fast Tester

---*Semitronix Tester Development Roadmap*

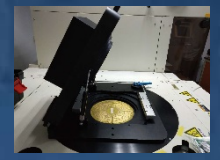
2010
Research and Development

2013
Gen I,
Partnership with NI
>100pA

2015/2016
Gen II, purchased by fab and fabless
100pA

2017


Gen III,
CE Certification
10pA

2018


Gen IV,
LCR meter
Test head
sub-pA

2019

T4100S
Testers in production lines

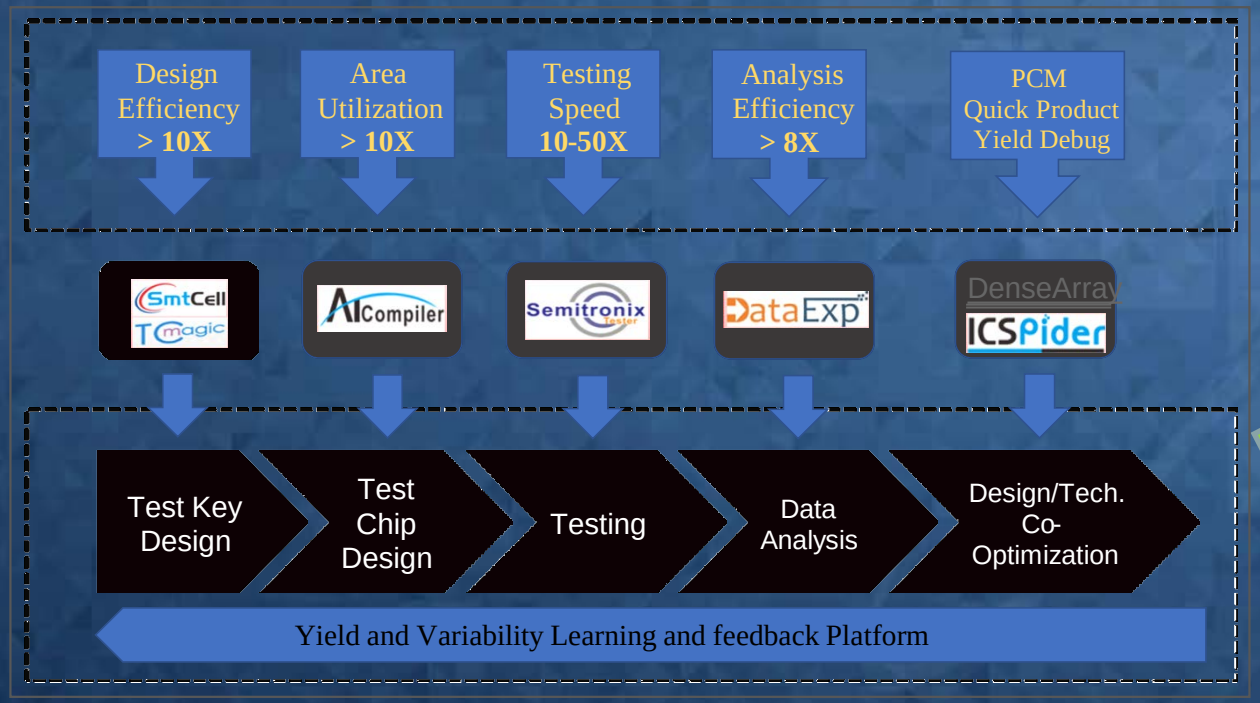
Content

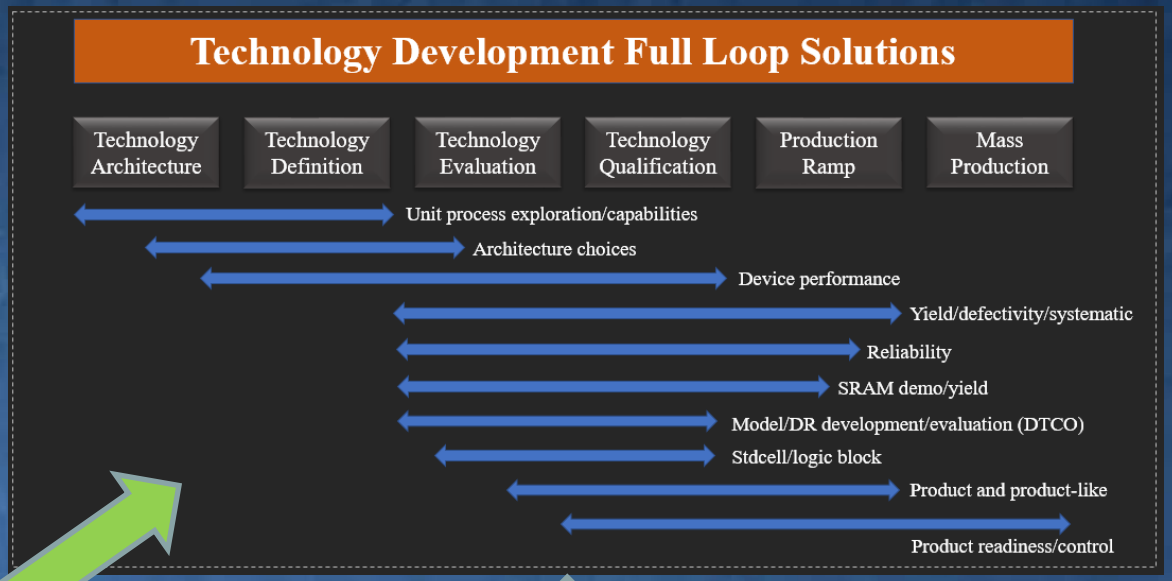
- Technology Roadmap
- **Semitronix Solutions Profile**
- Fast Testing Portfolio
- Summary

The **Design-Testing-Analysis** Eco System

- Semitronix is specialized at wafer level electrical characterizations
- Solutions include EDA software and IPs for test chip design and fast parametric tester

Infra-structure Platform





Customized Services

- Test chip design service
- Wafer test service
- Technology evaluation service

Breakthrough -- Fast Parametric Tester

Hardware: fast SMU with continuous sampling rates up to 600k samples/second. Fast switch matrix that allows multiple connection simultaneously

Better software system: allows users to optimize the testing algorithms to speed up tests

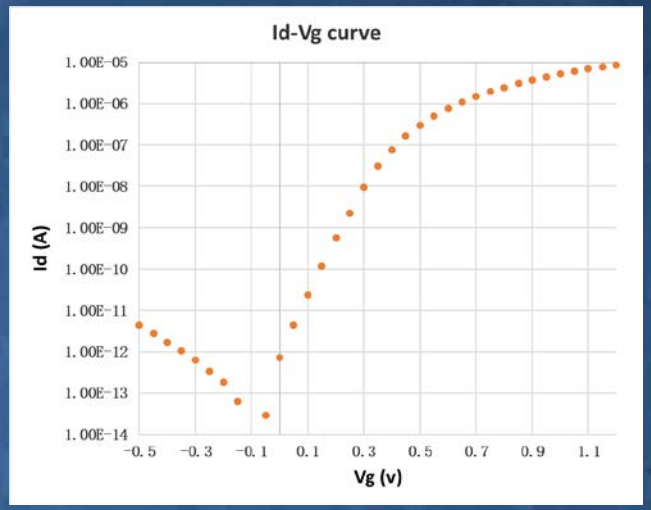
True Parallel testing allows multiple SMUs to work at the same time

Co-optimized with addressable test chip design: parallel test structure design/architecture supports parallel testing mode and reduces probe moving time

Semitronix tester

break-through ~ 10x speed

Traditional tester



Excellent current resolution

10.8%

Testing time compare to Other parametric tester

	Test items	Test dies	Total time (mins)	Time per die (mins)
Semitronix SMT	3516	21	110	5.23
Other parametric tester	3516	21	1020	48.57

Up to 2.6%

Testing time compare to Agilent (Addressable Yield open/short)

Items/Die: 1,803 ; Dies/Wafer:77 ; Items/Wafer:138,831

Agilent		471mins
SMT-IV	Single testing	41mins

Making Choices – Optimization Evolution

parallelization

Semitronix tester

Production application

Making choices also means staying reasonable in these choices.

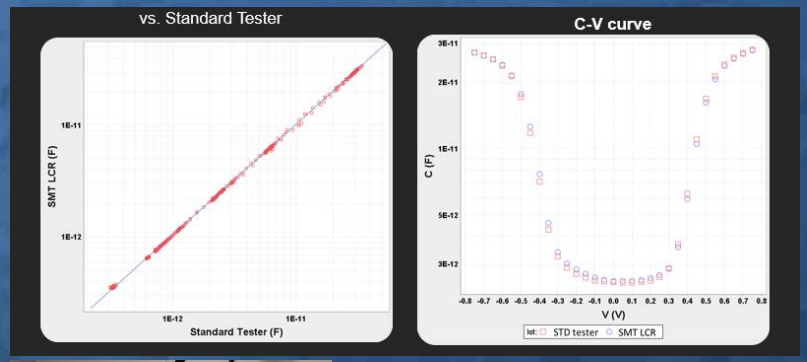
Semitronix Base T4000

Parallelization

Production readiness

Semitronix T4100 deploys 4-way parallization

Agilent		471mins
SMT-IV	Single testing	41mins
	4 Parallel testing	12mins

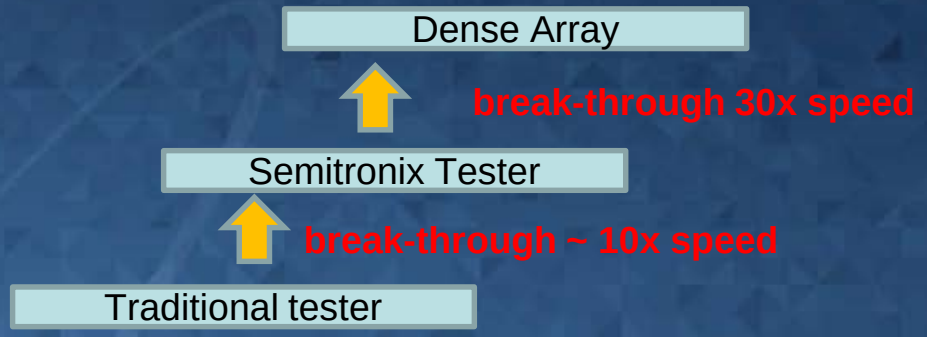


LCR addition

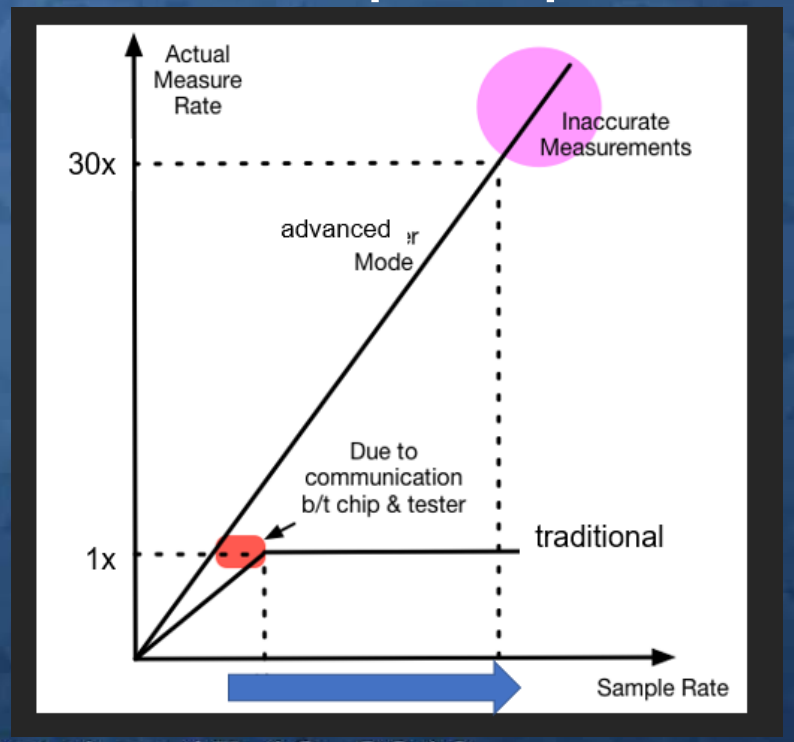
Prober integration with test-head

Next 10~100X Breakthrough: Co-optimized Design-Hardware

Bypass with BIST-like IP & test strategy



30x Speed-up



- Careful study of the test speed bottleneck yielded the opportunity for the next order
  - Advanced tester HW mode enables 30X speed-up
  - Test strategy and on-chip control unlocks the head-room by removing the bottleneck of setup and stabilization during test

Our Vision on Dense Array Framework

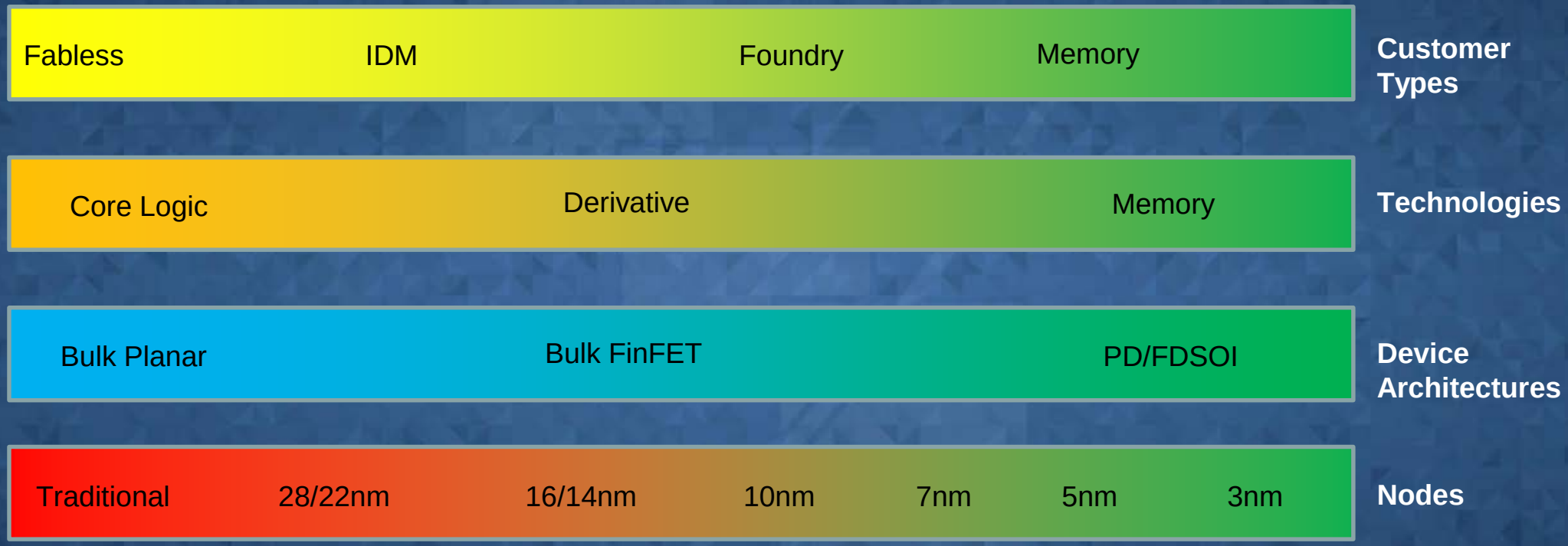
Dense array takes advantage of design/hardware co-optimization to achieve the next >10x improvement in test-site methodology

We envision that we make choices and evolve our full methodology based on this frame-work to address a variety of customer applications.

We believe with dense array, we can cover most of the TD test-keys within one partial design tape-out, instead of forcing TD team to fight for area on TD tape-out.

Semitronix Penetration

Semitronix test-site infra-structure successfully adopted broadly in the industry



- Our customers take advantage of our solution to drive more efficient business and technical results

Content

- Technology Roadmap
- Semitronix Solutions Profile
- **Fast Testing Portfolio**
- Summary

Why is Semitronix Tester much Faster ?

01 **Hardware**: fast SMU with continuous sampling rates up to 600k samples/second. Fast switch matrix that allows multiple connection simultaneously

02 **Better software system**: allows users to optimize the testing algorithms to speed up tests

03 **True Parallel testing** multiple node switching, parallel forcing and measuring

04 **Co-optimized with addressable test chip design**: parallel test structure design/architecture supports parallel testing mode and reduces prober moving time

The Fast Parametric Testing Solutions---**Hardware System**

SMU selections

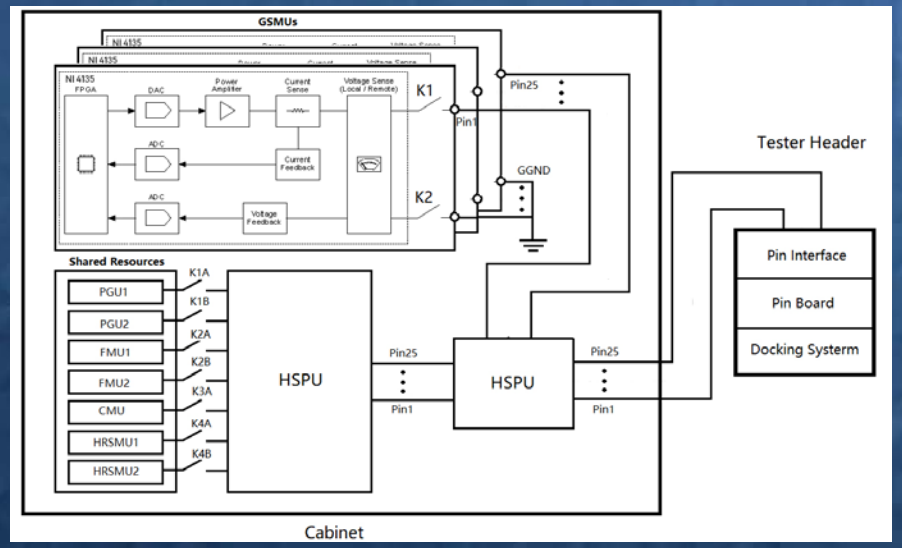
Our tester provides three types SUMs to meet different requirements, including High resolution SMU and High Speed SMU, details listed below

SMU Type	Highest Resolution	Highest Accuracy	Comment
High resolution II	100aA	<1pA	• Support high resolution measurement • Suggest use this SMU to measure microcurrent that <10pA, such as Ioff
High resolution I	10fA	5pA	• Support high resolution measurement • Suggest use this SMU to measure microcurrent that >5pA, such as Vt, Ioff
High Speed	10pA	400pA	• Support High Speed Measure • Suggest use this SMUs to measure large current, such as Id, Vt, Resistor measurement

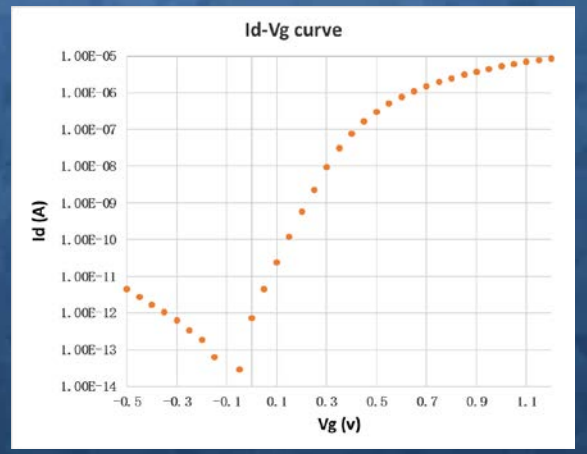
T4100 Architecture

软硬件协同开发

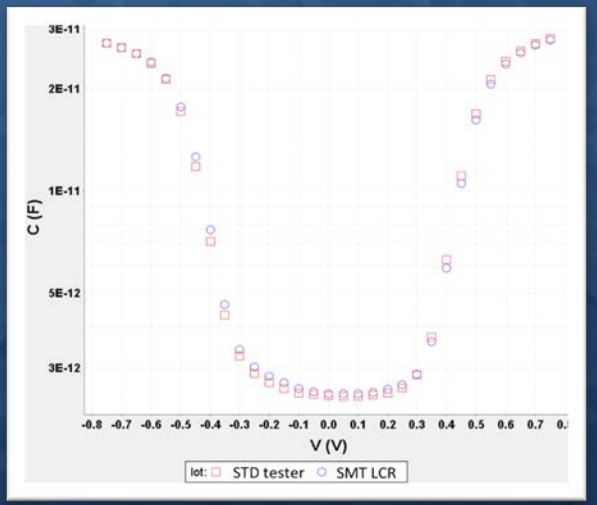
- Based on matured PXI platform, with good stability
- Hardware and Software co-optimization to ensure good accuracy with faster speed
- Close collaborations with vendors, and crucial parts are designed by ourselves
- Meet both AC and DC measurement requirements



Id-Vg curve



C-V curve



4th generation tester: T4100S

- **T4100S is Semitronix 4th generation Tester. It adopts per-pin architecture for SMUs**
- **Compared to SMT-III, it has following improvements:**
  - Low leakage current accuracy improves to sub-pA
  - Settling time for low leakage current is much improved (so that the testing time of Ioff and other low leakage measurement is greatly improved)
  - LCR, PGU, and FMU all go through switch matrix, so that manual connections are not necessary
  - Added test head, so that standard probe cards can be used and changing probe card also becomes easier
  - Support dense array testing (40,000 I-V measurements per second)
- **Benchmark showed >50% WPH improvements**

T4100S Spec

Item	T4100S
Standard Resources	Group SMU (25)
	High Precision SMU II(2)
	Pulse generator (2)
	Signal analyzer (2)
	LCR meter
Number of measurement pins	25
Voltage/Current Coverage	±100 V at ±20 mA
Voltage measure sensitivity	Group SMU:100 nV
	High Resolution SMU II:100 nV
Current measure sensitivity	Group SMU:10fA
	High Resolution SMU II:100aA
Current measurement accuracy	sub-pA
Maximum SMU sample rate	600K samples/sec
Measurement Functions	DC Current
	DC Voltage
	Kelvin
	Differential Voltage
	Frequency
	Arbitray waveform/clock generation
	Synchronization (triggering mode)
	C-V scan
Mean time between failures (MTBF)	> 1000 hours
Mean time to repair (MTTR)	< 6 hours
Uptime rate	> 97%

Content

- Technology Roadmap
- Semitronix Solutions Profile
- Fast Testing Portfolio
- **Summary**

Design more with yield penetration

Testing more with efficient way

Big data integration & analysis

Thanks for your Time !

SWTEST ASIA 2019

Advances in position measurement and analysis for guide plate microholes

Mike Cullimore

Oxford Lasers

OXFORD LASERS

Hsinchu, Taiwan, October 17-18, 2019

Contents

Oxford Lasers

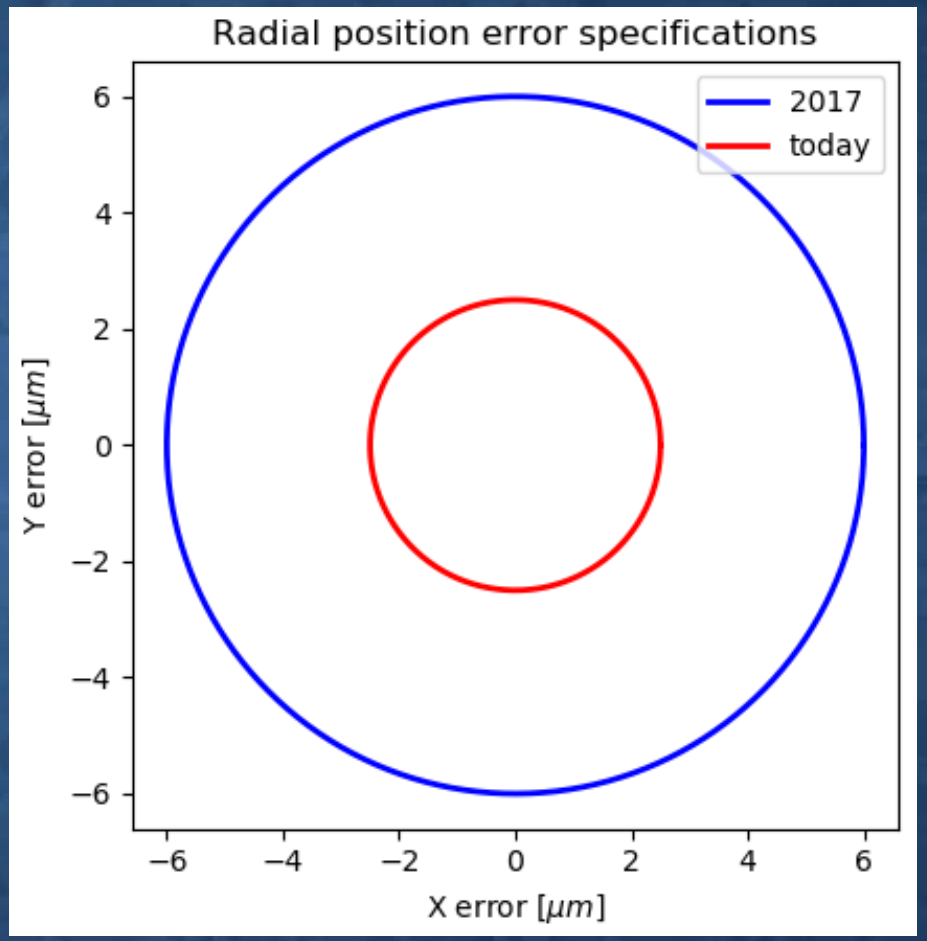
- Founded 1977
- 17 years' experience of guide plate production
- Subcontract micromachining
- Manufacture laser systems
- Multiple grants to support R&D for this application

Guide Plates for Probe Cards

- Guide Plates contain microholes to hold probes in position
- Hole counts can be tens to tens of thousands
- Typical Probe Card uses several Guide Plates
- Materials include silicon nitride, alumina, Kapton, Photoveel, Vespel, Cirlex, Macerite etc.
- Position accuracy is *critical*

Background

- **Position error specification:**
  - 2.5µm radial
  - 6µm only two years ago!
- **Measuring to this precision is a *significant challenge to the industry***
  - “System X does not agree with system Y”
  - “Results different after recalibration”
- **Measurement itself adds an error**
- **Here we share our work to address this challenge**



Objectives

1. Identify position error of the measurement system
2. Minimize this contribution
3. Maximize throughput
4. Design the system to be easy to operate

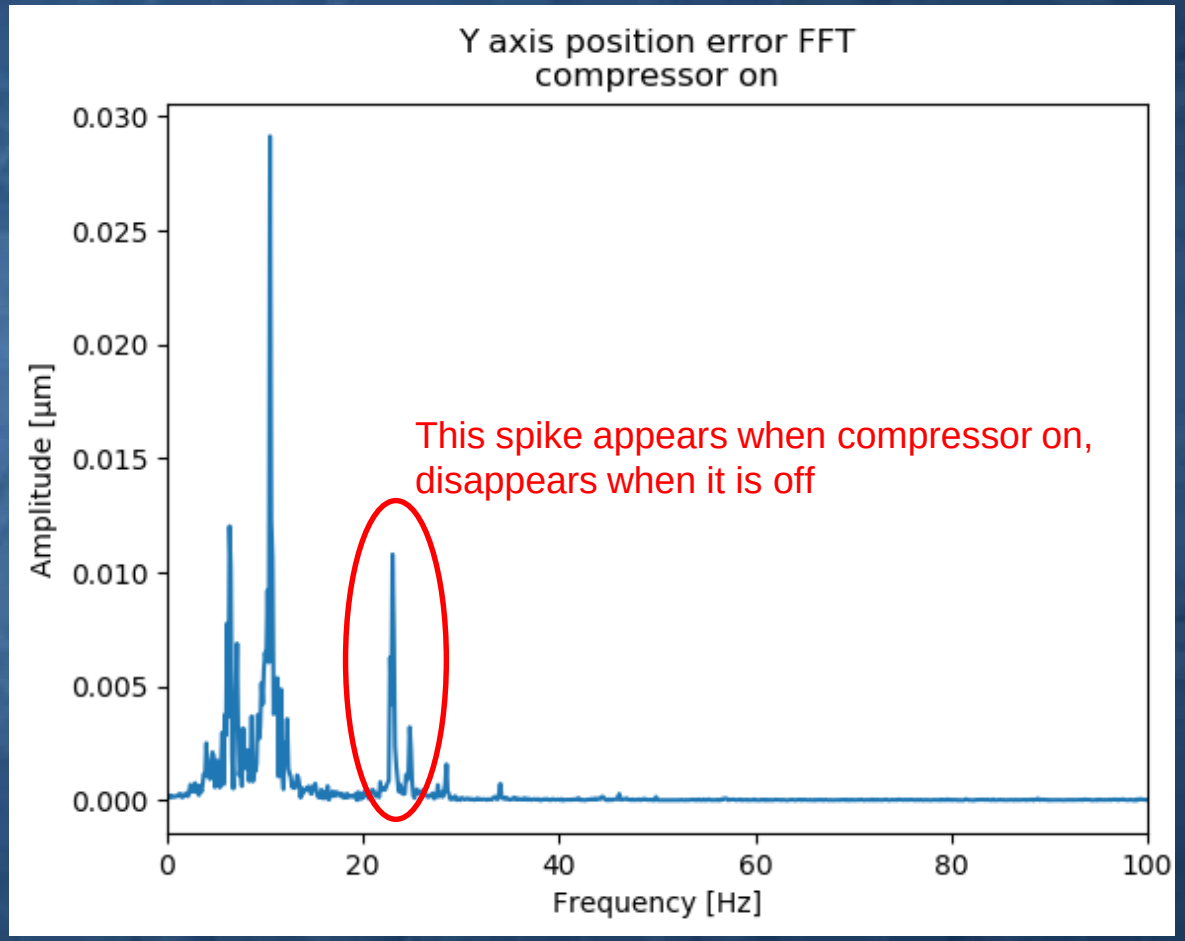
Sources of measurement error

1. Dynamic errors
2. Camera calibration
3. Camera rotation relative to XY stages
4. Calibration of XY stages
5. Thermal effects

- These slides focus on *dynamic errors*
- (Ask me after the talk and I'll be happy to discuss our work on the other terms)

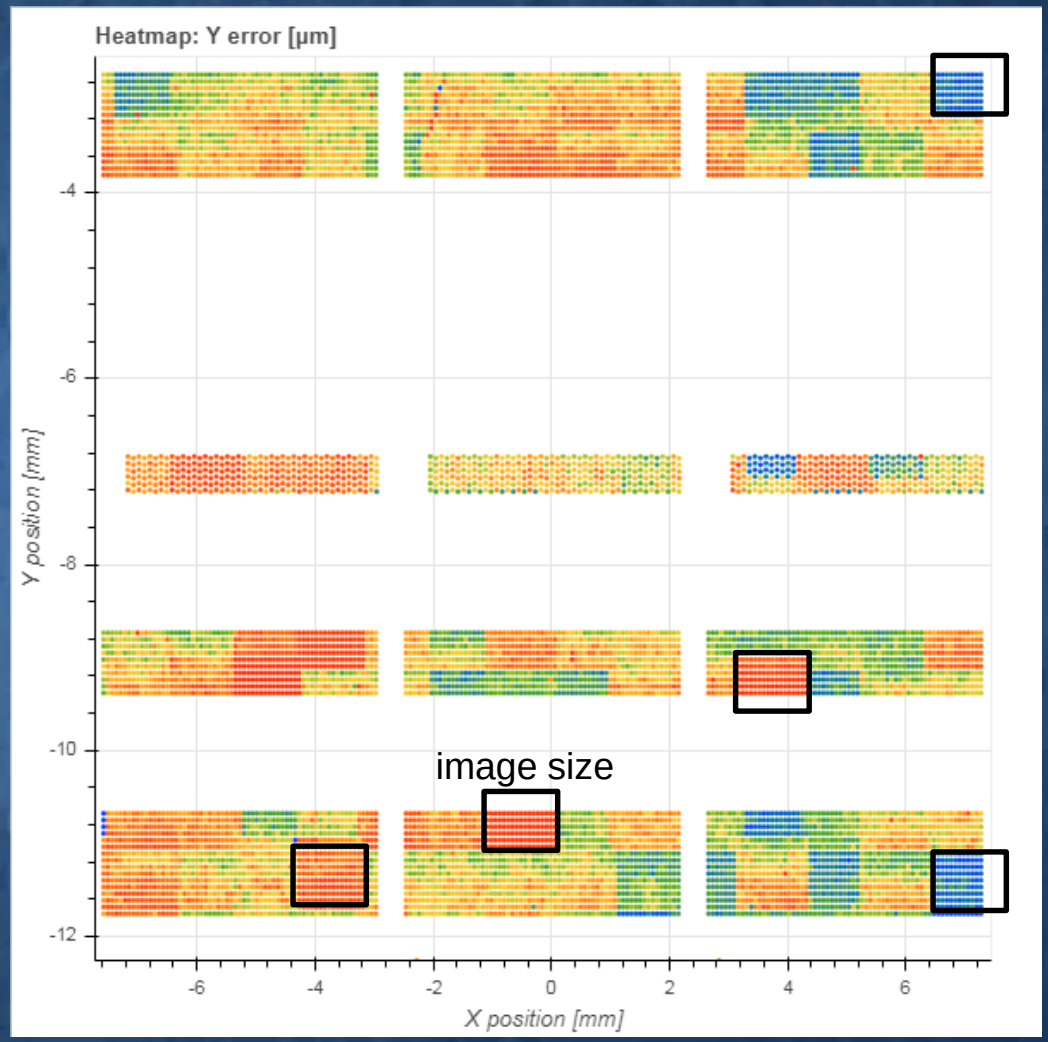
Vibration

- Many sources of vibration in factory e.g. air compressors
- Need to isolate measuring system from them
- Fourier Transform (right) useful to identify frequencies present
- Anti-vibration mounts put under granite to dampen



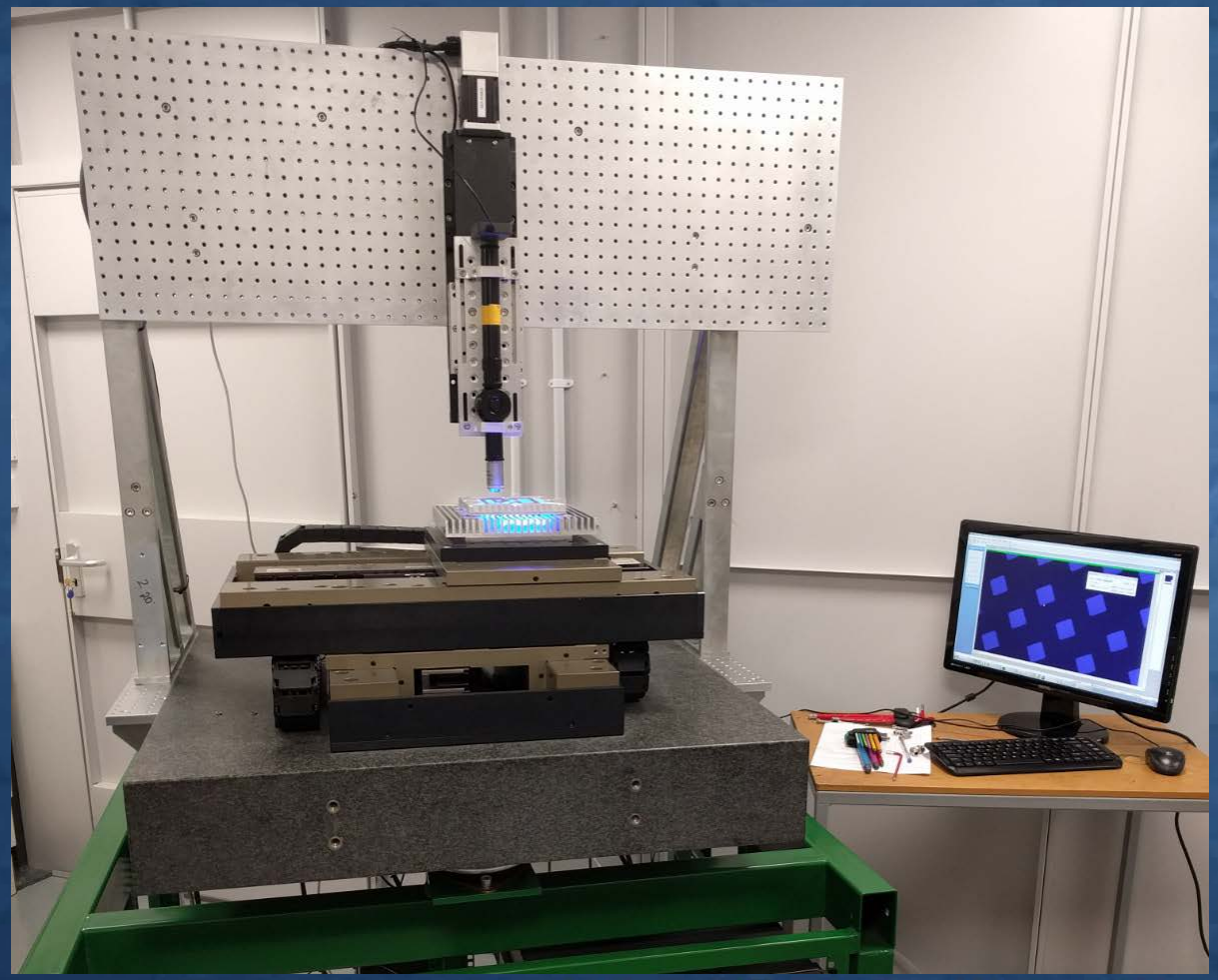
Heatmap: block artefacts

- Plot shows hole positions coloured by error (±3µm)
- This early result has blocks of colour, same size as image
- We were able to link these artefacts to gantry resonance
- Stiffer gantry made of granite (next slide) resolved this



Gantry stiffness

Version 1: metal gantry

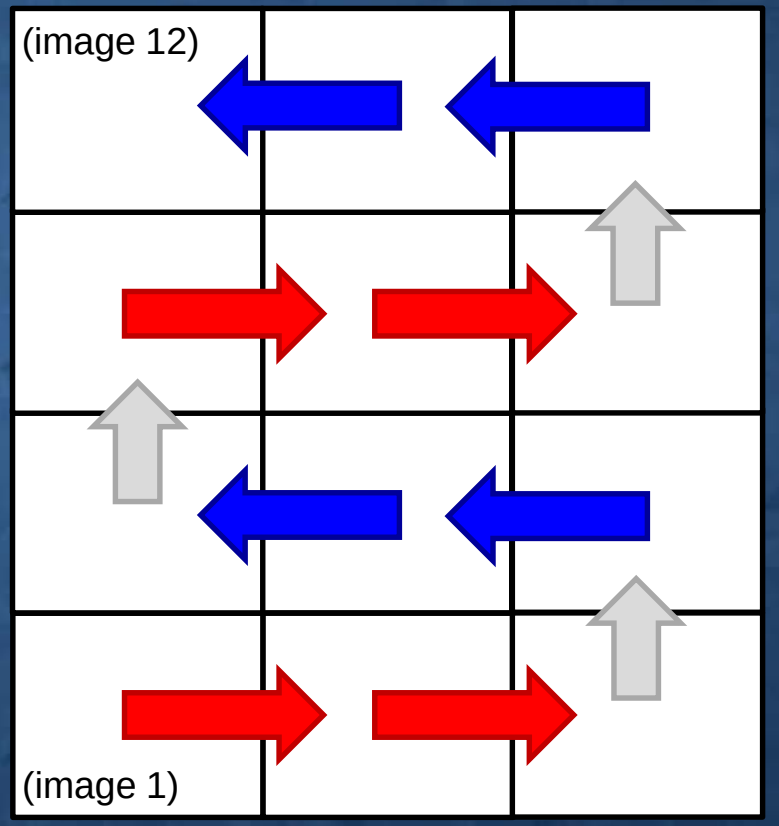


Version 2: granite gantry

Move speed test

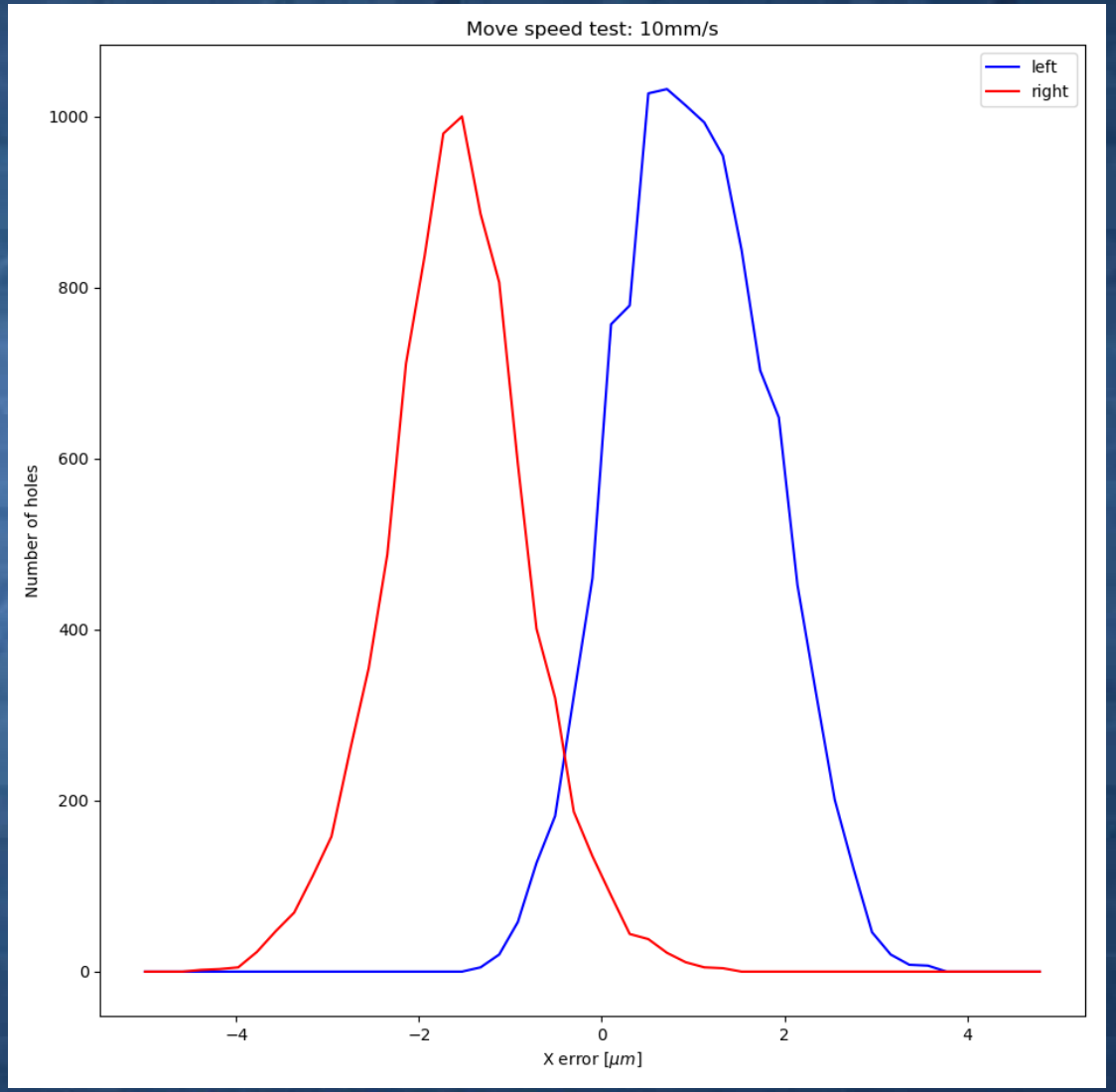
- **Perfect measurement system contributes nothing to position errors**
- **Would be unable to tell where XY stages had moved**
- **Test:**
  - We *do* know where XY moved: exploit this
  - Illustration right: red arrows for right moves, blue arrows for left moves
  - Group errors by move direction (left or right) and plot distribution

Move order



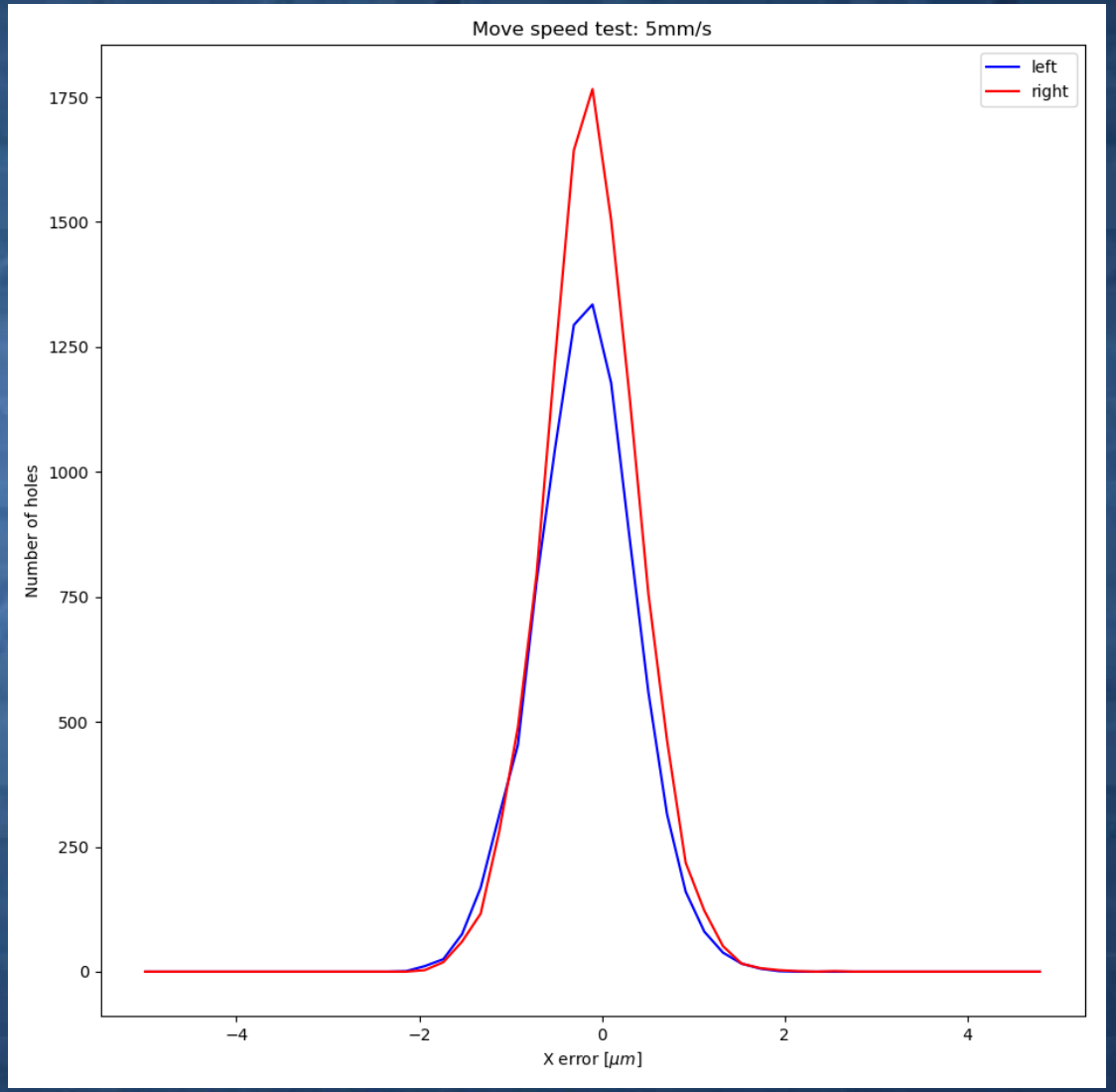
Move speed: 10mm/s

- **How fast can it move?**
  - Faster -> higher throughput
  - … but what about measurement error?
- **Plot right shows clear separation between the two groups**
- **Moves were too fast**

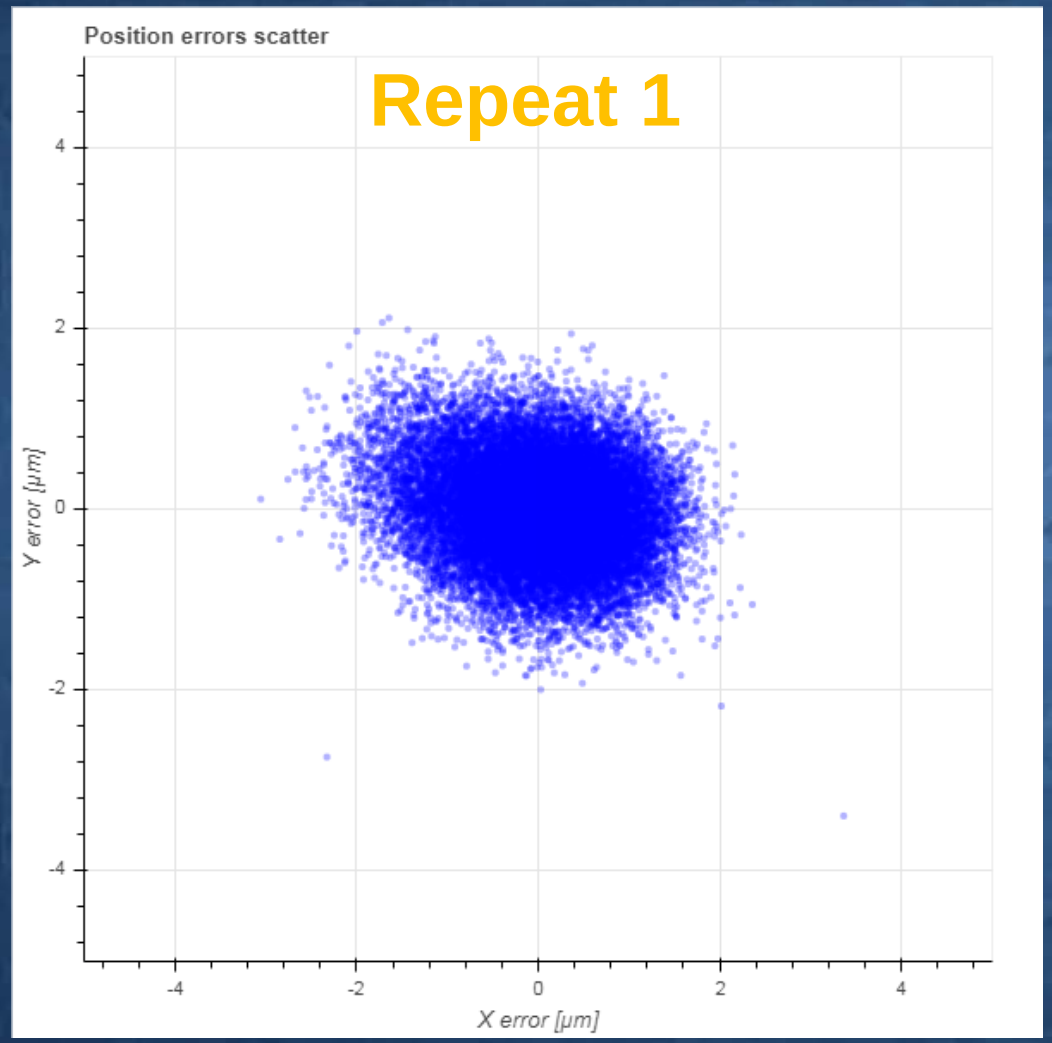


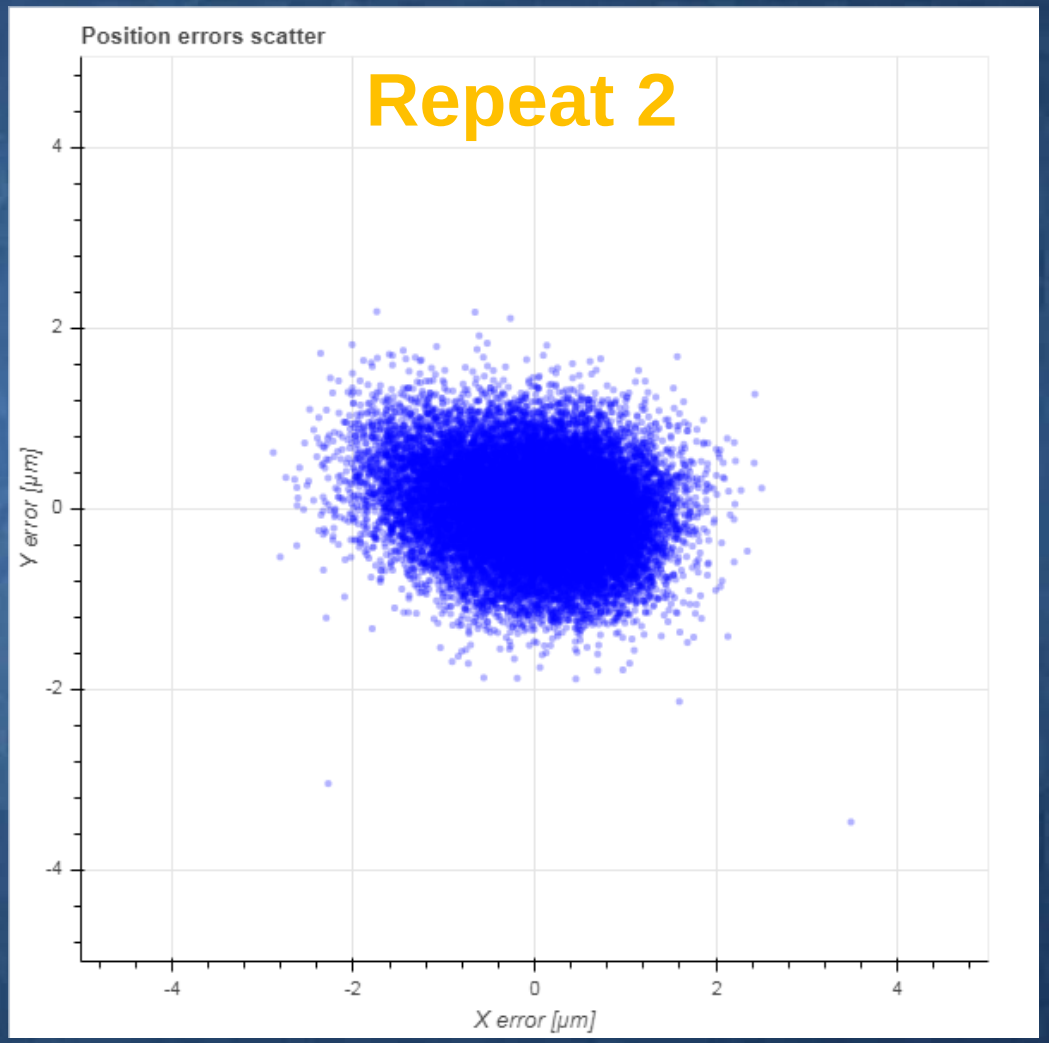
Move speed: 5mm/s

- **This plot is as it should be**
  - Both distributions: mean zero
- **Can't tell whether measuring machine was moving left or right**
- **5mm/s is now default speed**
  - Could test values between 5 and 10mm/s but time gain would not be worth it



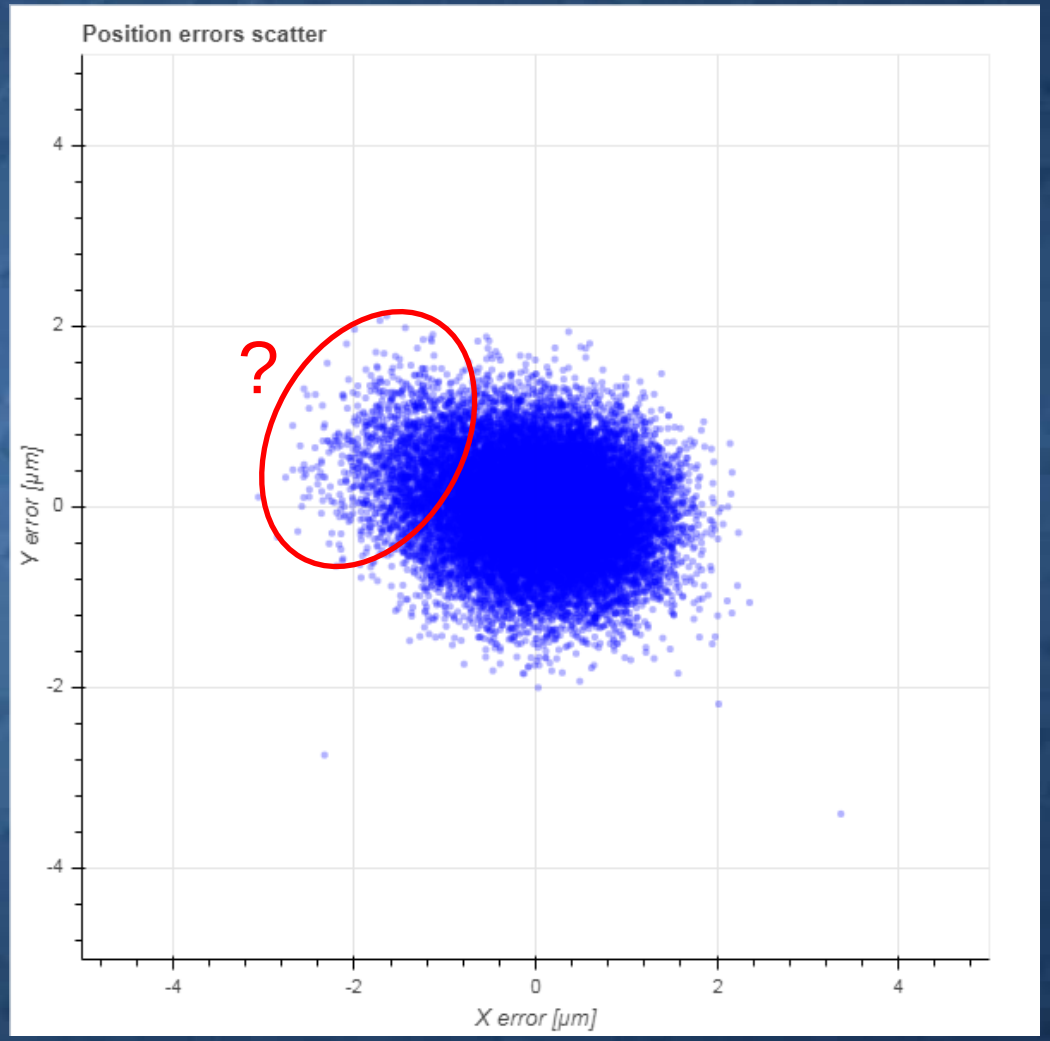
Measurement repeatability



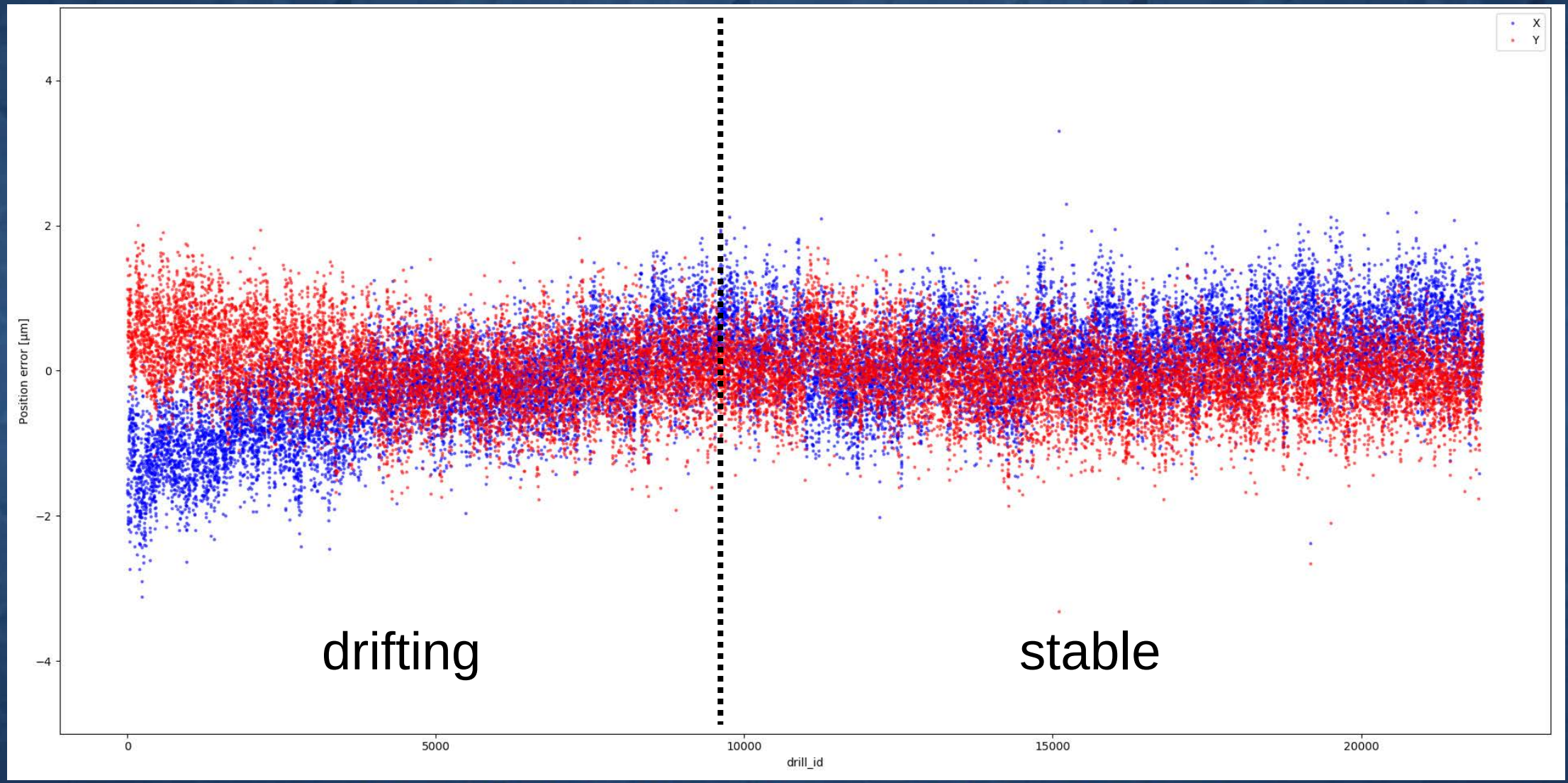


But why the teardrop shape?

- Want to see tight Gaussian distribution
- But there is a tail on the scatter plots
- Exploit known drill order: see next slide
- Shows that there was drift at the start of the drilling



Same data plotted vs drill order

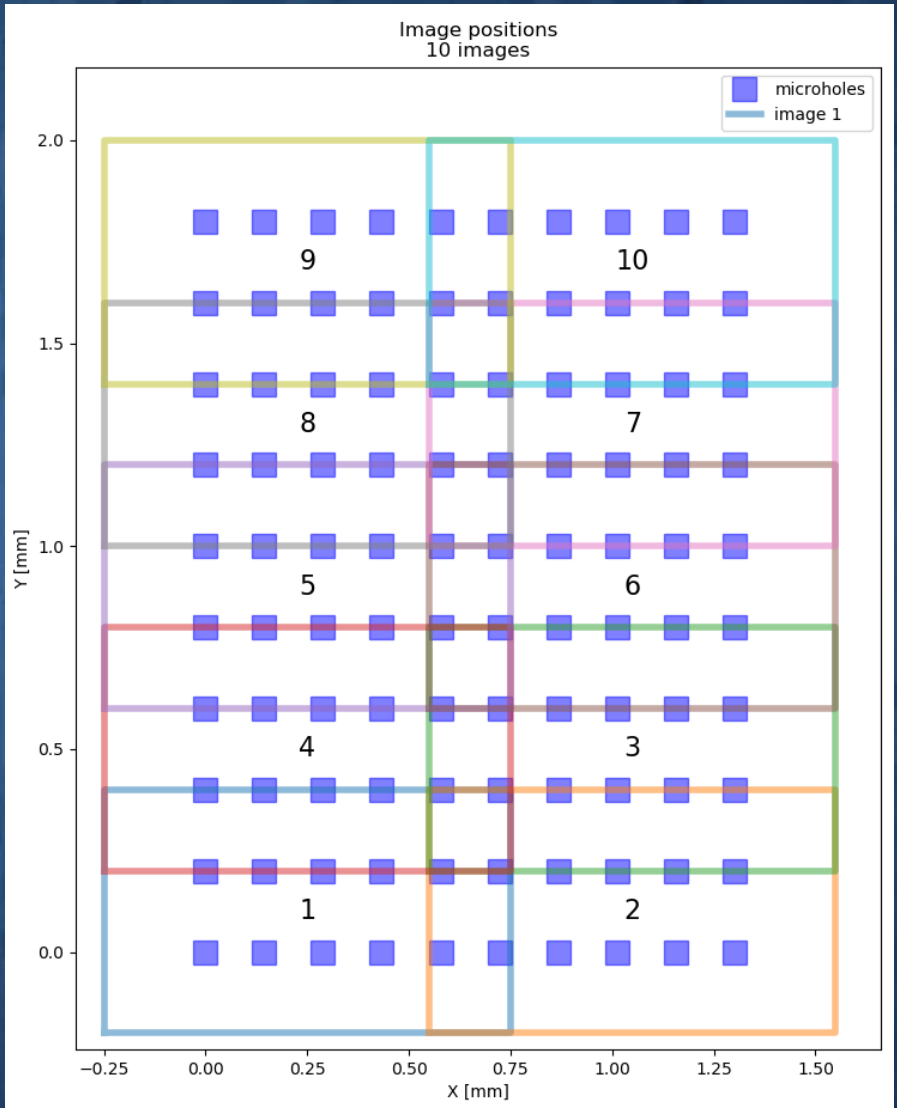


Speed and throughput

- **Given production volume, need high throughput**
- **Design features for high speed:**
  - Large field of view (image): many holes per image
  - Sub-pixel interpolation to keep accuracy high
  - Highest move speed without compromising error (see test above)
  - Air bearing XY stages
- **Simple process also an important part**
  - See alignment section below

Image positions

- Ideal: take fewest images which capture all holes
- Current solution: overlapping mosaic (example right)
- Sort them to minimize move distance
- Move X then Y: stage with less weight has lower error
- Calculated automatically



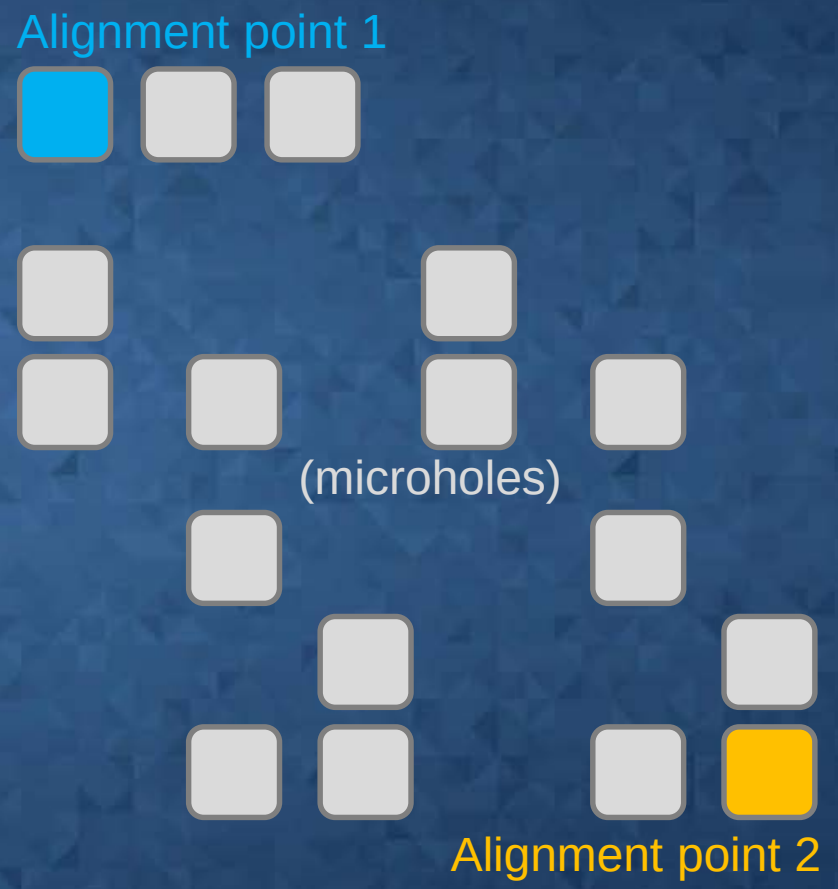
Process times

test	*images*	*holes*	*time [MM:SS]*	*images/s*	*holes/s*
1	918	22,000	15:38	0.98	23
2	918	22,000	12:40	1.21	29
3	924	22,000	12:29	1.23	29
4	990	38,000	16:44	0.99	38

- 1 image per second is typical
- 20+ holes per second
- (These depend on layout of microholes)
- ~15 minutes to capture images
- (Alignment not included: see next section)

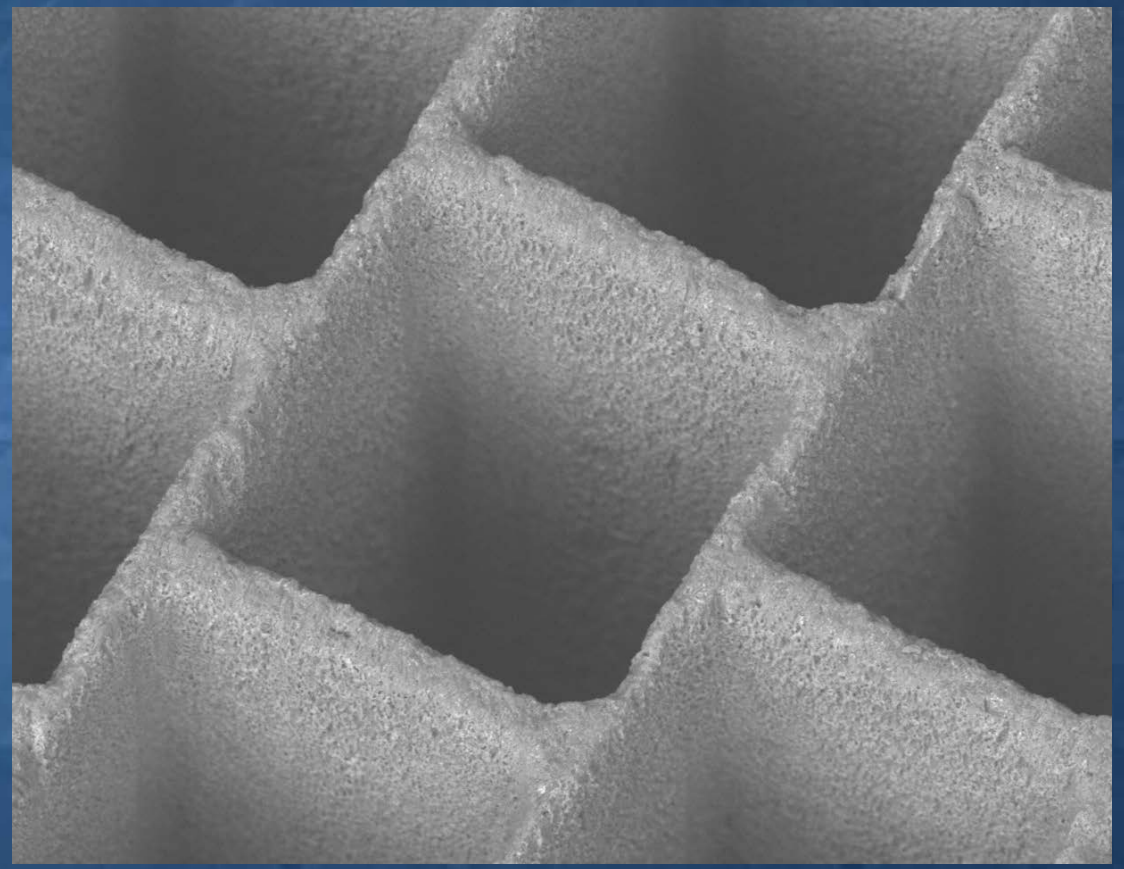
Alignment

- **Alignment is critical**
- **Coarse alignment: two points**
  - Points selected *automatically*
  - User aligns first
  - XY moves to second *automatically*
  - User aligns second (small adjustment)
  - Simple, user-friendly and fast: <5 mins
- **Fine alignment: least-squares**
  - Uses all holes for accuracy
  - Removes error in coarse step



Quality control and process improvement

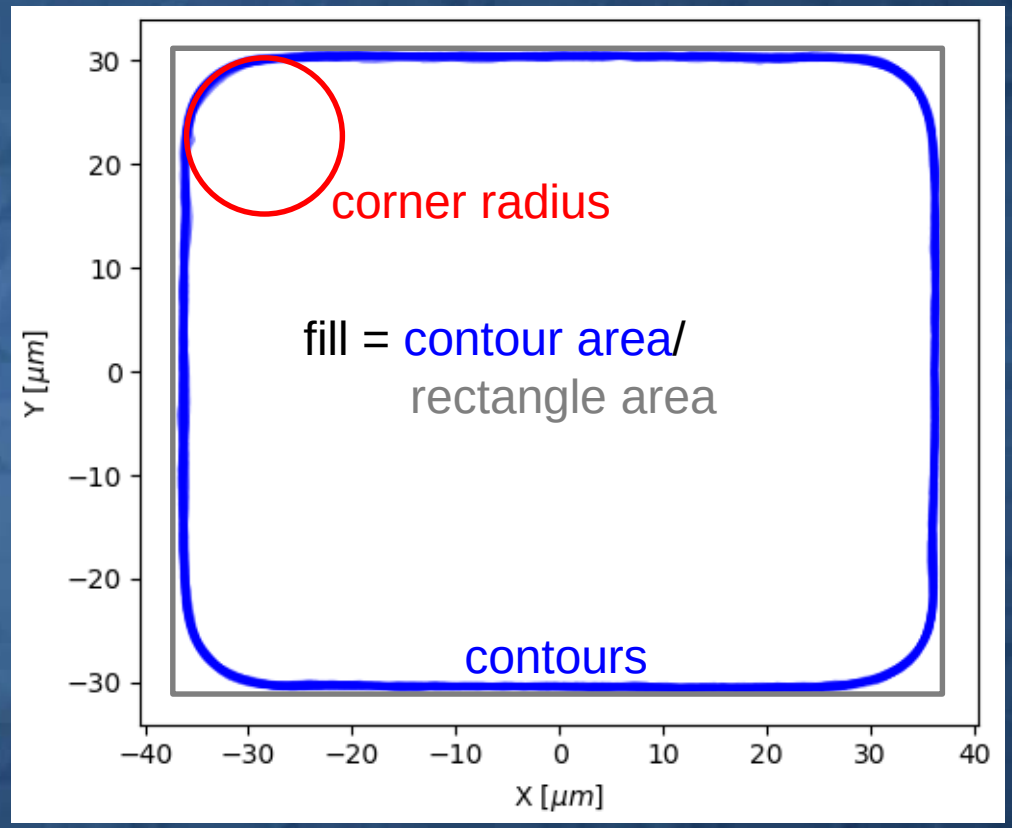
- **Our measurement system will address two needs:**
  1. Quality control: ensuring parts we ship meet customer specifications
  2. Process improvement: feedback to achieve better drilling results
- **Position error drift identified above is example of latter**



Microholes in silicon nitride with 9µm exit land

Not only position

- **Focus in these slides has been on position data**
- **System also measures:**
  - Hole size distribution
  - Hole contours (shape)
  - Corner radius
  - Fill (perfect rectangle is 1)



Summary

- **We are consistently able to meet 2.5µm radial tolerance**
- **Our measurement system is helping us improve further**
- **Measurement system features:**
  - Typical measurement time ~20 minutes for 30,000+ holes
  - Sub-micron repeatability
  - Anti-vibration mounts to isolate from other equipment
  - Stiffer granite gantry removed mechanical resonance
  - Move speed 5mm/s: fast without compromising on accuracy

Follow-on work

- **Continue using feedback to improve drilling processes**
  - New processes presented at SW Test (US) under evaluation

- **Database integration**
- **Thermal: monitor system temperatures**
- **Alignment relative to macroholes/fiducials**
- **Vibration: improve isolation from environment**

Thank you for your time.

Does anyone have any questions?

SWTEST ASIA 2019

2D MEMS Probe to Parametric Testing and Other Probe Technology

Takao Saeki
Formfactor

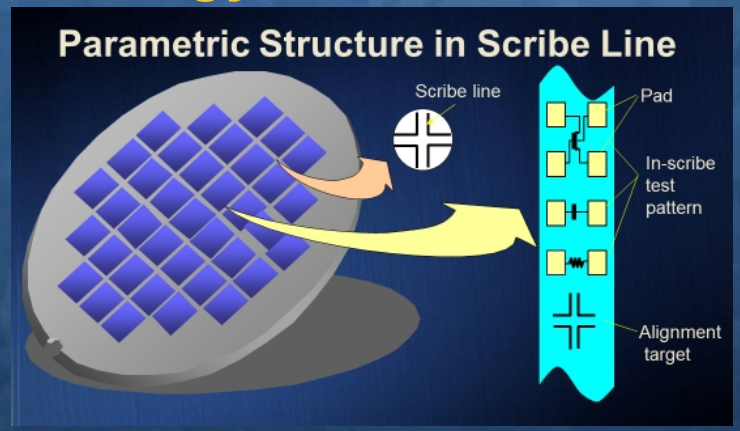
Hsinchu, Taiwan, October 17-18, 2019

Overview

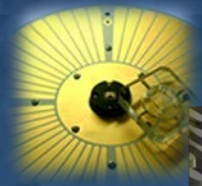
- Introduction
- History of Parametric Probe Card
- Objective
- 2D MEMS Probe to Parametric Test
- Customer Evaluation Results
- Probe Technology Comparison for Parametric Testing
- Summary

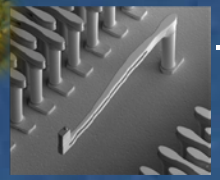
Introduction

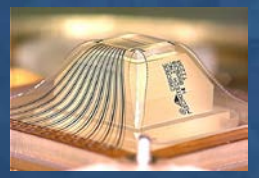
- **Parametric Testing(WAT; Wafer Acceptance Test) is unique application for probe card suppliers**
  - Basically similar and simple probe layout – 1 or 2 lines, 10 – 100 probes
  - NO device type specific test – DRAM, NAND, SoC, Logic, CIS
  - Each semiconductor company has each special requirement
  - Circuit, Test condition, Pad size, material and treatment, Sample size and etc
  - Many different Probe technologies are available by each probe card supplier
- **Formfactor also providing many probe technology**
- **Added 1 more probe technology to Parametric card – 2D-MEMS, T18**

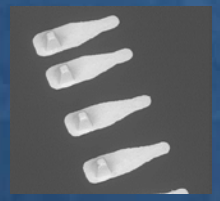


History of Parametric Probe Card







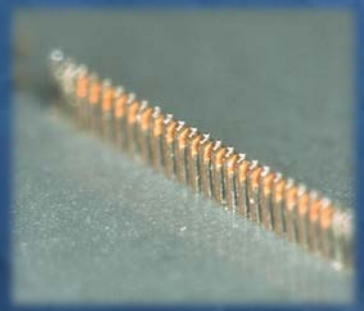


2000 2005 2010 2015 2020

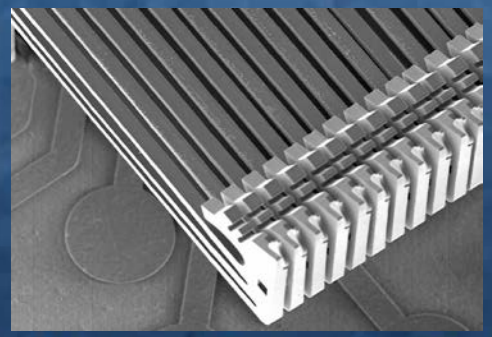
- Cantilever Needle

- 3D MEMS(Takumi T3, T11)

- Pyramid Membrane



- Vertical MEMS



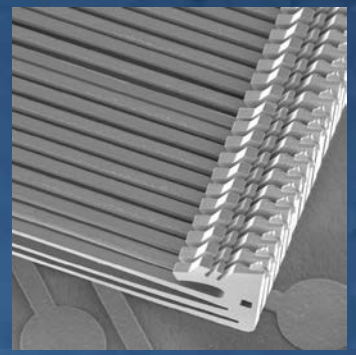
- 2D MEMS – Takumi-CL

Objective

- Introducing T18, 2D-MEM Cantilever type spring under evaluation by A Semiconductor company.
- Evaluation is showing some difference from 3D-MEMS type probe
- Hopefully this presentation will be one of guidance for probe technology choice for Semiconductor company

T18, 2D-MEMS Probe to Parametric

- **Formfactor T18, 2D-MEMS Cantilever type spring was originally developed for Wafer Sort application**
  - Take advantage from Cantilever type and Vertical type
  - Low Scrub Ratio; 4% OD with saturating
  - Less Particle generation
  - Excess Over Travel capability; 250um Max OD



- **Potentially good for Parametric Probe Card !?**
  - Low Scrub Ratio → Stay in Small pad(<30um) with ease of use
  - Less Particle generation → Good for everybody
  - Excess OD capability → Absorb thermal Z movement with ease of use

2D-MEMS and 3D-MEMS Difference

- **2D and 3D Comparison for some important factors**

T18, 2D-MEMS	Item	T11.2, 3D-MEMS
Square Pole (10x10x >20um)	Probe Tip Shape/Size	Truncated Pyramid (6x6 ~ 25x25um)
+/-5um	Tip Placement Accuracy	+/-5um
Fixed - 35-50um	Spring Body - Width	Tapered – More Robust
PA-II	Tip Material	PA-II
4% Saturating - Smaller	Scrub Ratio	10% Linear
250um - Larger	Maximum Over Travel	150um

T18, 2D-MEMS Probe Tip

- **2D-MEMS Tip Shape maintains same tip size for life**
  - Polishing probe tips by Abrasive cleaning will not change the tip X&Y size

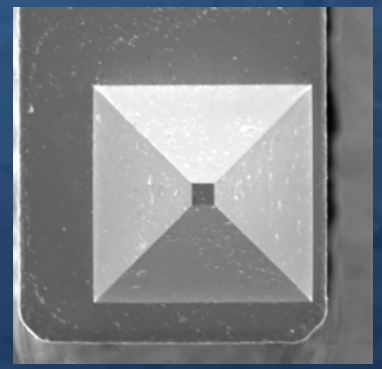
Angled View
- T18, 2D

Side View
-T18, 2D

- **T11, 3D-MEMS Pyramid Shape**
  - 6x6um tip size increases by tip wear and abrasive cleaning
  - Scrub mark size also increases
  - # Recent ITS Waffle cleaning maintains tip size small

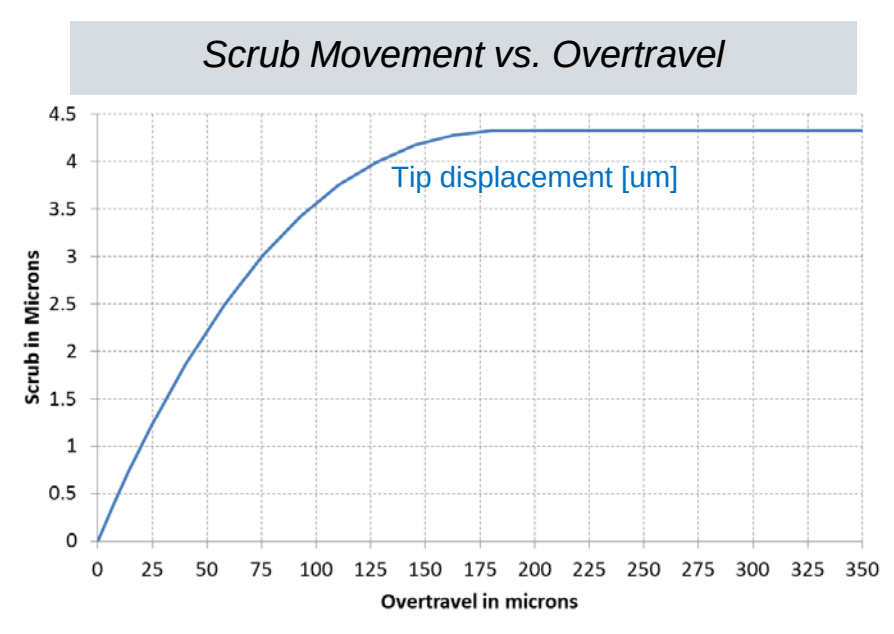
by aggressive cleaning and rounding tip

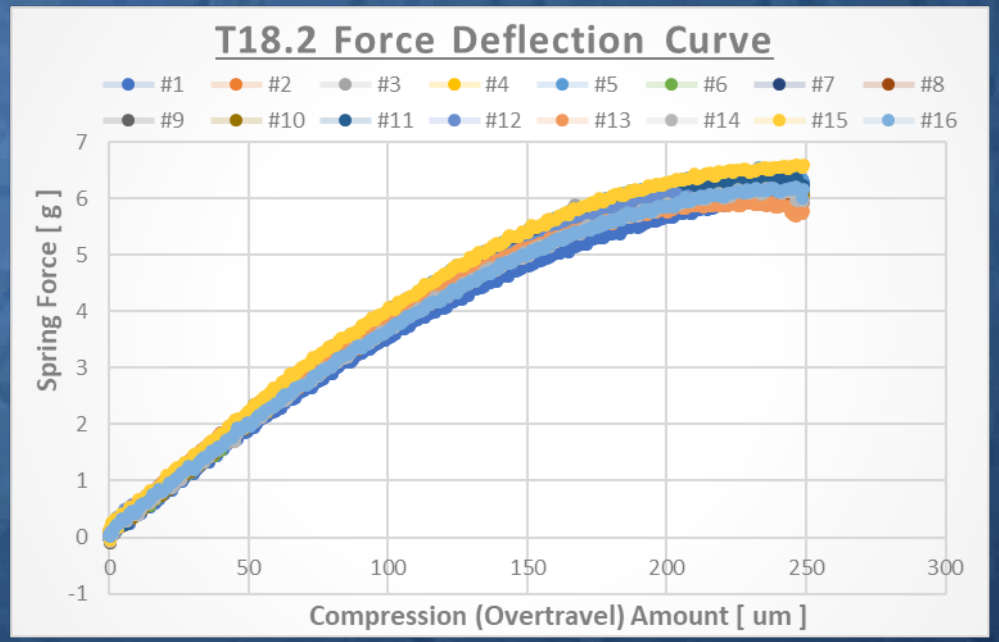
Top View
– T11, 3D



T18, 2D-MEMS Scrub Ratio and Force

- **Scrub Ratio; ~4% with decreasing at high OD**
- **Spring constant(K-value); 0.6 – 0.8[g/mil] decreasing at high OD**



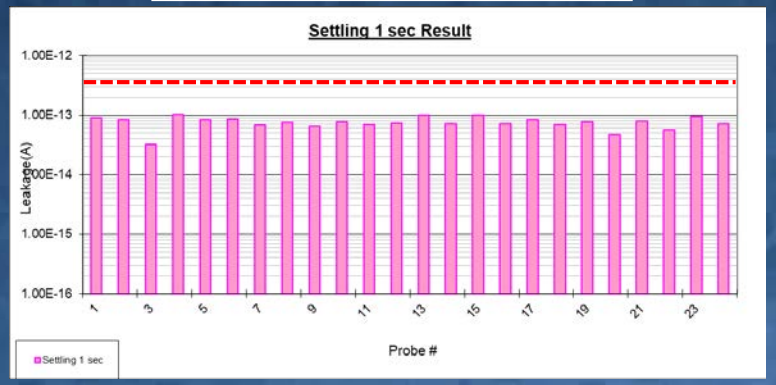


T18, 2D-MEMS – Low Electrical Leakage

Experimental Procedure

Tester; Agilent 4156C
Measured voltage: 10V (100V)
Temperature: 23+/-5C
Humidity: 50+/-10%
Measurement pin count: 48 ch
Measurement setting time: 1sec, 10sec

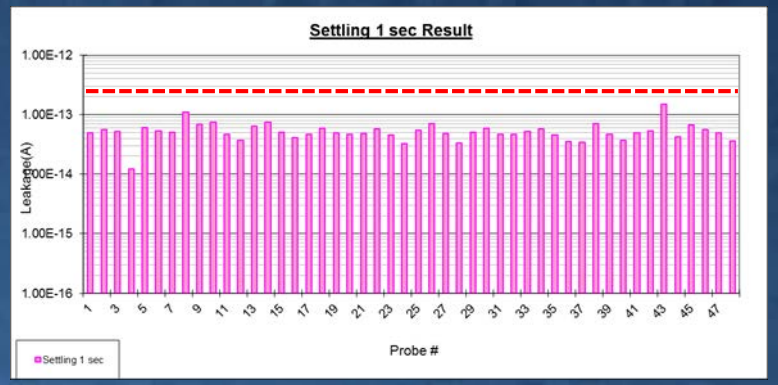
3D-MEMS, T11 - Takumi

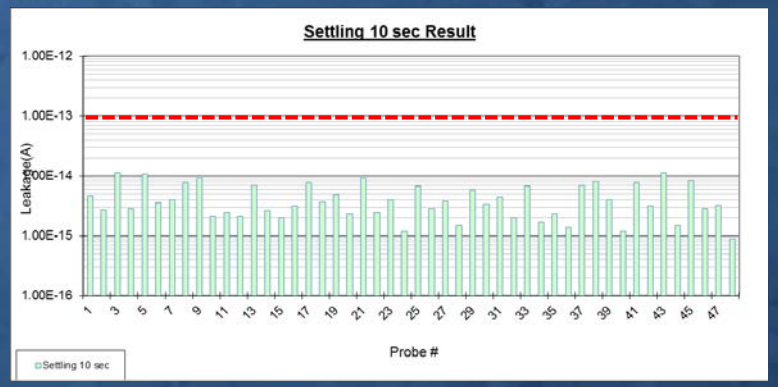


<250fA @ 1 sec settling

<100fA @ 10 sec settling

2D-MEMS, T18 - Takumi-CL



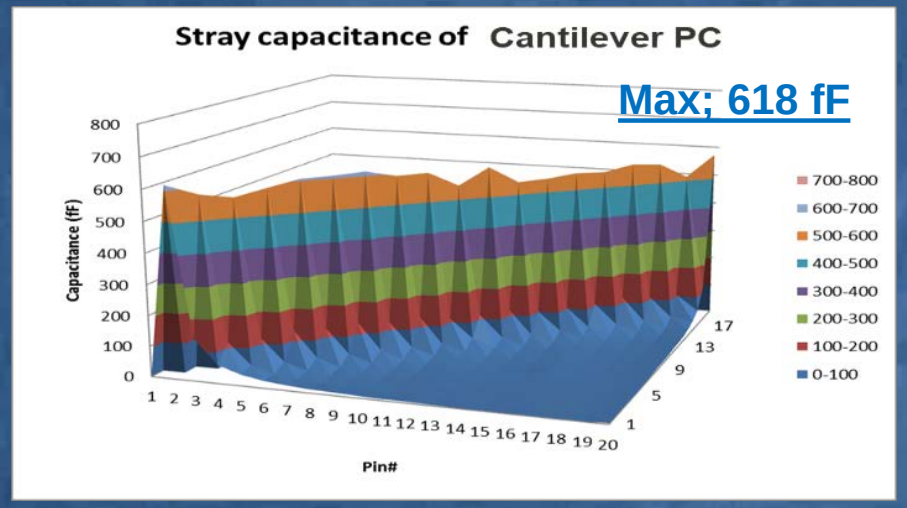


- **2D-MEMS & 3D-MEMS probe card both showed equivalent low electrical leakage performance**
- **MEMS type leakage performance rely on substrate and PCB, which requires experienced design and material selection**

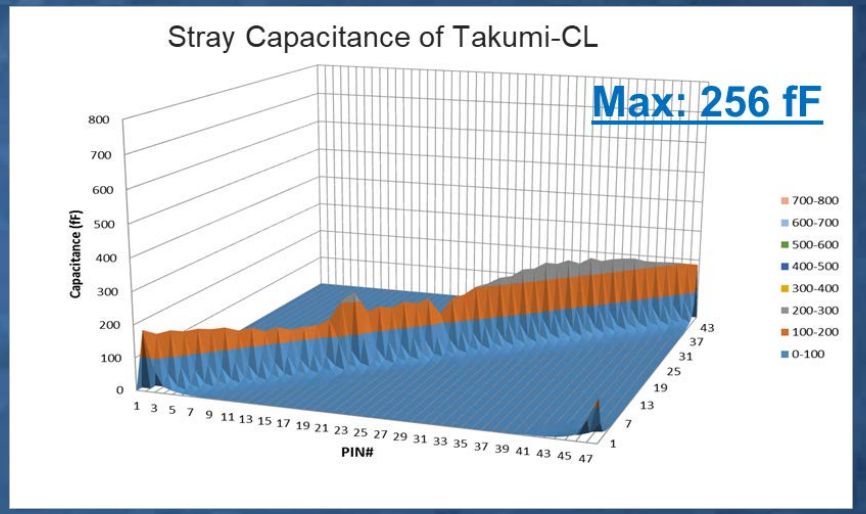
T18, 2D-MEMS – Low Parasitic(Stray) Capacitance

Tester; Agilent E4980A
Measured voltage: 1V
Measurement frequency: 1MHz
Temperature: 23+/-5C
Humidity: 50+/-10%
Measurement pin count: 48 ch

Typical Cantilever Probe Card



2D-MEMS, T18
Takumi-CL



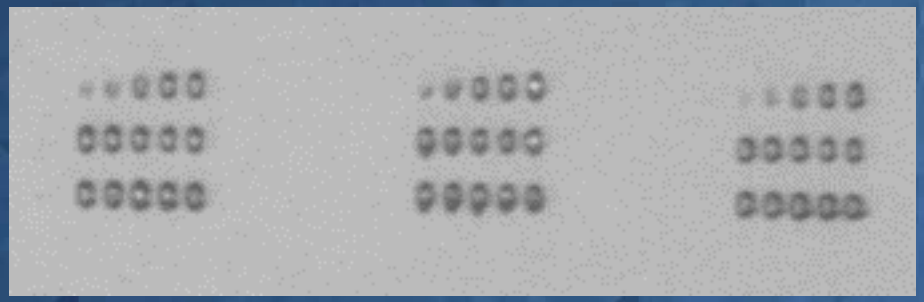
- **2D-MEMS probe card showed low stray capacitance equivalent with 3D-MEMS type**
- **Careful Substrate design and material selection are important to utilize MEMS stable mechanical performance and realize consistent electrical performance.**

Customer Evaluation Results

- A semiconductor company has been evaluating T18 probe card with actual wafers
- Important to evaluate the actual Scrub mark size and Electrical Contact performance with actual wafer, which varies with pad metallization condition

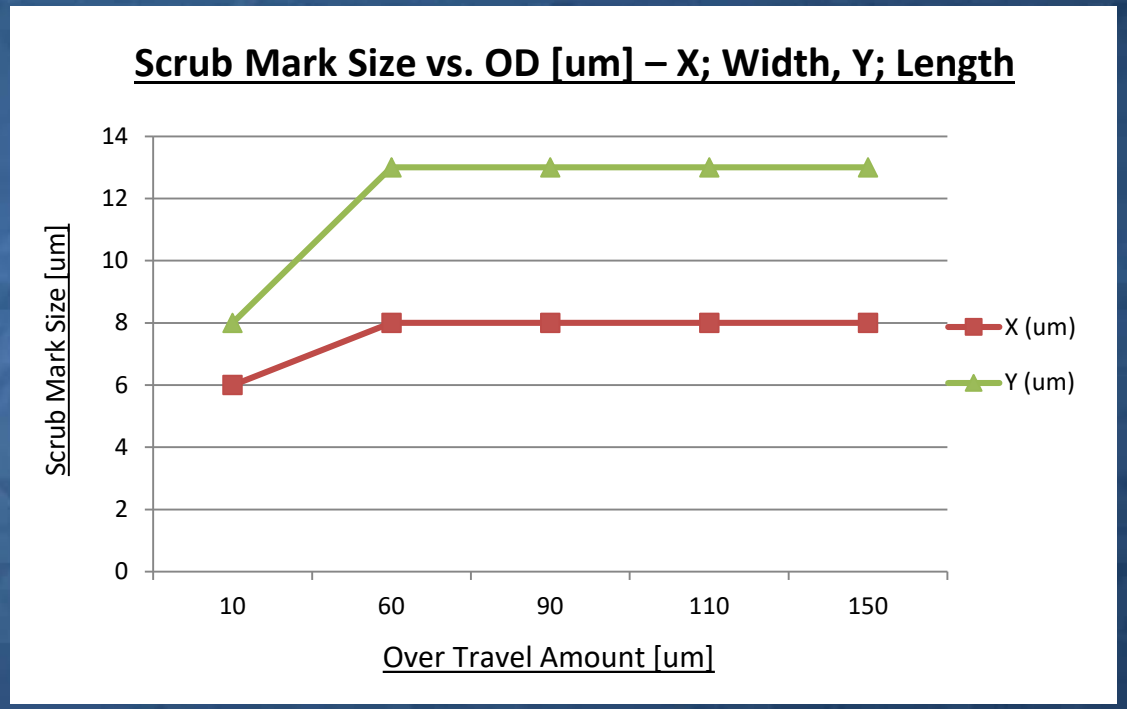
Customer Evaluation Results
– Scrub Mark Size, T18, 2D-MEMS

- **Scrub Mark Size saturated on actual customer wafer also**
  - Saturated Scrub Mark Size; 8 x 13um (NSxS direction)



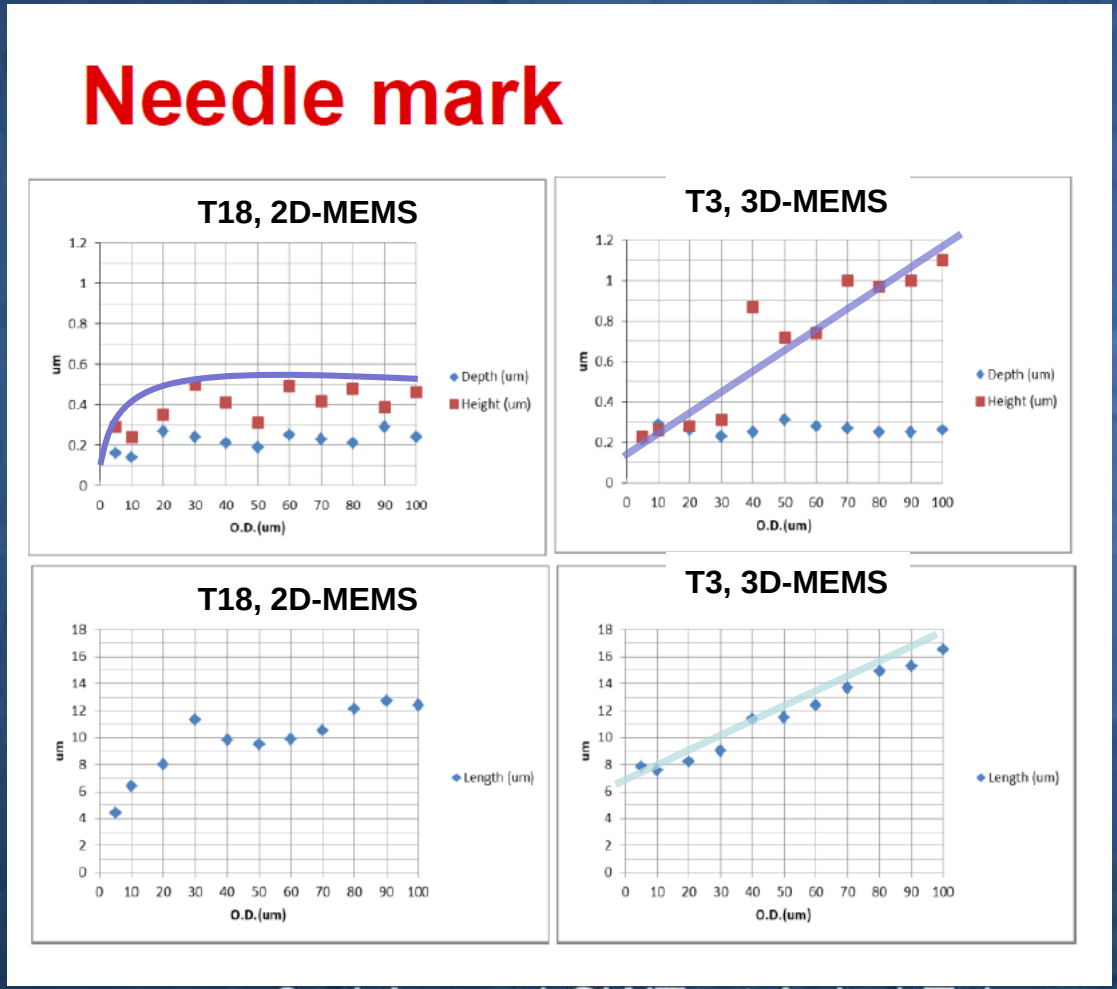
OD (um)

10	20	30	40	50
100	90	80	70	60
110	120	130	140	150



Customer Evaluation Results
– Scrub Mark – Depth & Prow Height

- **Customer Special Requirement: Prow Height**



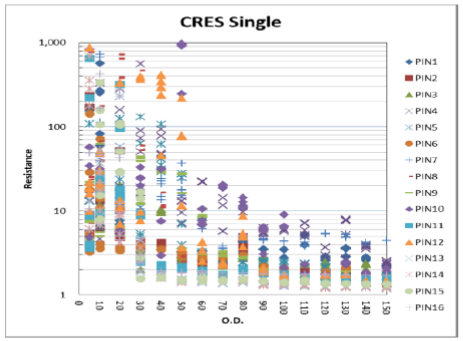
- **Due to following process, Prow height limitation required**
  - T3 type 3D-MEMS showing proportional increase
  - T18 type, 2D-MEMS showing saturated prow height and passed customer criteria

Customer Evaluation Results
– CRES vs. OD Performance

- **Production Overtravel amount was set with 100um with margin**
- **Evaluation continues**

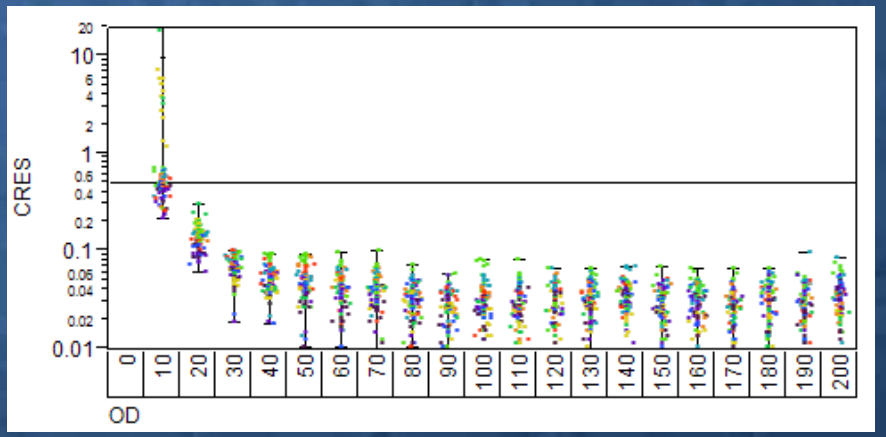
Customer Data

CRES



Takumi-A option3 O.D. spited C-res data.

- Stable C-res looks stable above 90um O.D. in this evaluation.
- We choice 100um O.D. temporary standard.
- Spring force will increase 2.2g to 3.8g (about 40%)



CRES[Ohms] vs. OD[um]
Stable after 90um Overtravel
CRES + Path Registance

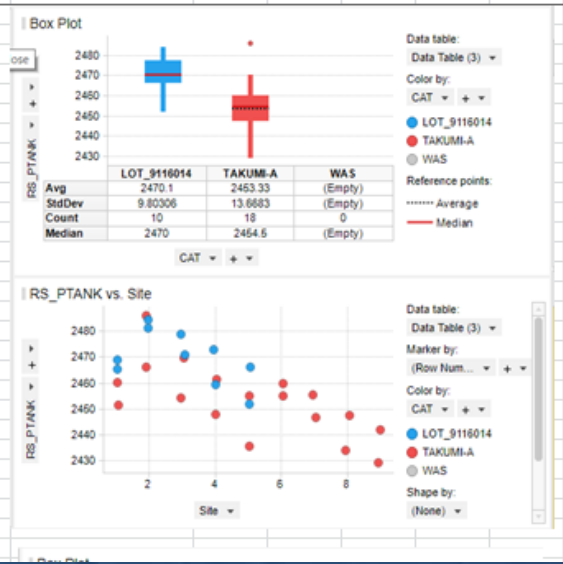
CRES[Ohms] vs. OD[um]
FFI Internal Measurement

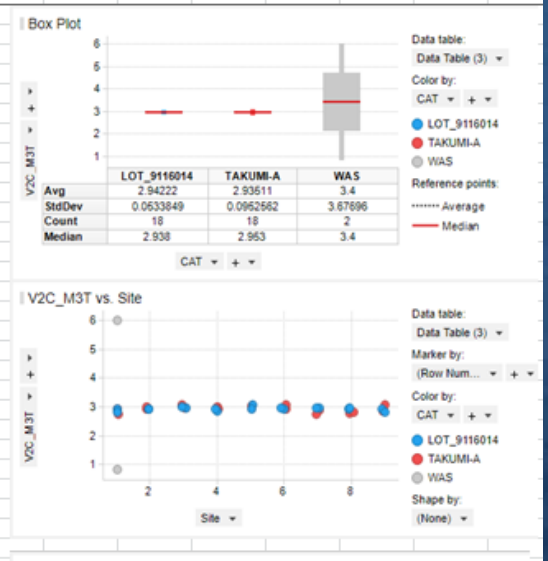
Customer Evaluation Results
– Electrical Data Correlation #1

- **Data Correlation between Cantilever card and T18 card performed with +/-2.5% difference specification on 110 items**

Parameter Name			Sameness1	Summary
Example A	Link to SFC	Green	94	94
Example B		Yellow	8	8
Example C		Red	8	8

Parameter Nar	Baseline Mea	Baseline Std	Split Mean	Split Std	Sameness		ABS(DEL%)
S1P_VTLS	-0.7	0.01	-0.7	0.01	100.03%	0	0.0%
X12N_VTL	0.57	0.01	0.57	0.01	100.03%	0	0.0%
X20P_VTL	-0.65	0.01	-0.65	0.01	100.03%	0	0.0%
X28N_VTL	0.59	0.01	0.59	0.01	100.03%	0	0.0%
X30P_VTL	-0.55	0.01	-0.55	0.01	100.03%	0	0.0%
X33N_VTL	1.51	0.01	1.51	0.01	100.03%	0	0.0%
X40P_VTL	-0.55	0.01	-0.55	0.01	100.03%	0	0.0%
HZEN_BV	6.34	0.01	6.34	0.01	100.03%	0	0.0%
RS_NBL	49.92	1.72	50.39	1.64	100.06%	0	0.9%
NV_BVBS3	-21.95	0.16	-21.82	0.12	100.12%	0	0.6%
RS_M2SRP	92.55	1.97	93.25	1.76	100.14%	1	0.8%
RS_PHSR	304.83	0.62	304.94	0.57	100.17%	0	0.0%
S3P_BVDW	-8.1	0.11	-8.12	0.1	100.18%	#	0.2%
S7PABVDS	-13.1	0.11	-13.12	0.1	100.18%	#	0.2%
V2K_M3T	2.72	0.17	2.67	0.15	100.18%	#	1.9%
BP_IDET	39.08	1.33	38.88	1.21	100.19%	#	0.5%
S3NIBIDS	20.76	0.24	20.63	0.19	100.21%	#	0.6%
CC_PMOAT	10.44	0.45	10.54	0.39	100.22%	0	0.9%
NV_HPE_M	61.91	1.81	61.61	1.58	100.23%	#	0.5%
NV_BVEBO	17.15	0.07	17.1	0.05	100.23%	#	0.3%
NV_BVGEO	10.28	0.16	10.3	0.14	100.23%	0	0.2%
S7PAIONS	-238.05	1.79	-237.35	1.42	100.25%	1	0.3%
NV_BVECS	17.13	0.06	17.12	0.05	100.26%	#	0.1%
CC_NMOAT	10.49	0.29	10.47	0.24	100.27%	#	0.2%
V1K_NOM	4.08	0.16	4.1	0.13	100.27%	0	0.5%
X20N_ION	338.85	0.91	339.46	0.6	100.28%	1	0.2%
RS_HFE_M	21.08	0.52	21.03	0.41	100.29%	#	0.2%
X28N_ION	282.36	5.83	282.25	4.37	100.29%	#	0.0%





Customer Evaluation Results
– Electrical Data Correlation #2

- 16/110 items showed >2.5% spec. And customer confirmed all of 16 items are caused by other testing root causes.
- And passed the correlation test.

Takumi-A electrical part update

Result

-Compared the CRES between released cards.
Slightly shift between Cantilever and Takumi/Takumi-A.
The cause is as a shift from the difference in contact area.
Cantilever : 0.26 ~ 0.28 Ω
Takumi : 1.03 ~1.30 Ω
Takumi-A : 1.11 ~ 1,35 Ω

-Compared the sameness by totally 110 items.(*WAS only)
Did not found abnormal matter by Card issue. @R/Y color.

	Sameness1	Summary
Green	94	94
Yellow	8	8
Red	8	8

3

- "CRES" this case means "(CRES)+(Path Resistance)x2Ch value

Parametric Probe Card Comparison

		Cantilever Needle	3D MEMS - T11	Pyramid Memblene	Vertical MEMS	2D-MEMS, T18
Mechanical Characteristics	Pad Pitch	>50um	>50um	>50um	>74um	>70um
	Layout Capability - 2 Row	40um	60um	60um	74um	70um
	Probe Tip Size	10x10	4x4	8x8um	10x10um	10x10um
	Tip size growth by tip wear	Yes	Yes	Yes	No	No
	Probe Tip Placement Accuracy - X & Y	+/-5um	+/-5um	+/-5um	+/8.5um	+/-5um
	Scrub Ratio (% to OD)	Long	Midium	Short	Short	Short
	Accuracy durability	+/-10um	+/-5um	+/-5um	+/-8.5um	+/-5um
	Pad Size - Production level	>50x50um	>25x25um	>30x30um	>30x30um	>30x30um
Electrical Characteristics	Leakage Performance	Moderate - Low	Low	Moderate	Moderate	Low
	Path Resistance	Low	Midium	Middium	Midium	Midium
	Contact Stability	Moderate	High	High	Moderate	High
Special Require ment	RF	Moderate	Moderate	-3dB@40GHz	Moderate	Moderate
	Bump wafer parametric	Capable	Height Limit	NA	Capable	Height Limit
Utilization	Life Time	Moderte	Long	Moderate	Moderate	Moderate
	Probe Insert Replaceable	Some	Yes	Yes	Yes	Option
	Unit Cost	Low	Moderate	Moderate	Moderate	Moderate
	NRE Cost	None	Moderate	Moderate	Moderate	Moderate
	New desgin Lead Time	Short	Moderate	Moderate	Moderate	Moderate

- **Each Probe Technology has each strength and weakness**

Consideration and Next Step

- T18, 2D-MEMS evaluation with A Customer showed a special benefit, Low prow height
- Continuing customer qualification to optimize the utilization and look for other benefits for customer satisfaction
- Depends on priority, one of characteristics will fit on all Semiconductor company.
- Will accumulate the experience to find out the fastest way