Product Brief

Universal Network Probe Demo Design

Overview

Aliathon Ltd. in partnership with Nallatech brings to market a demo design based on the Universal Network Probe technology described in Aliathon Application Note 06. This design demonstrate the key attributes of the Aliathon / Nallatech strategic partnership in the Network Analytics/Assurance market space. These are;

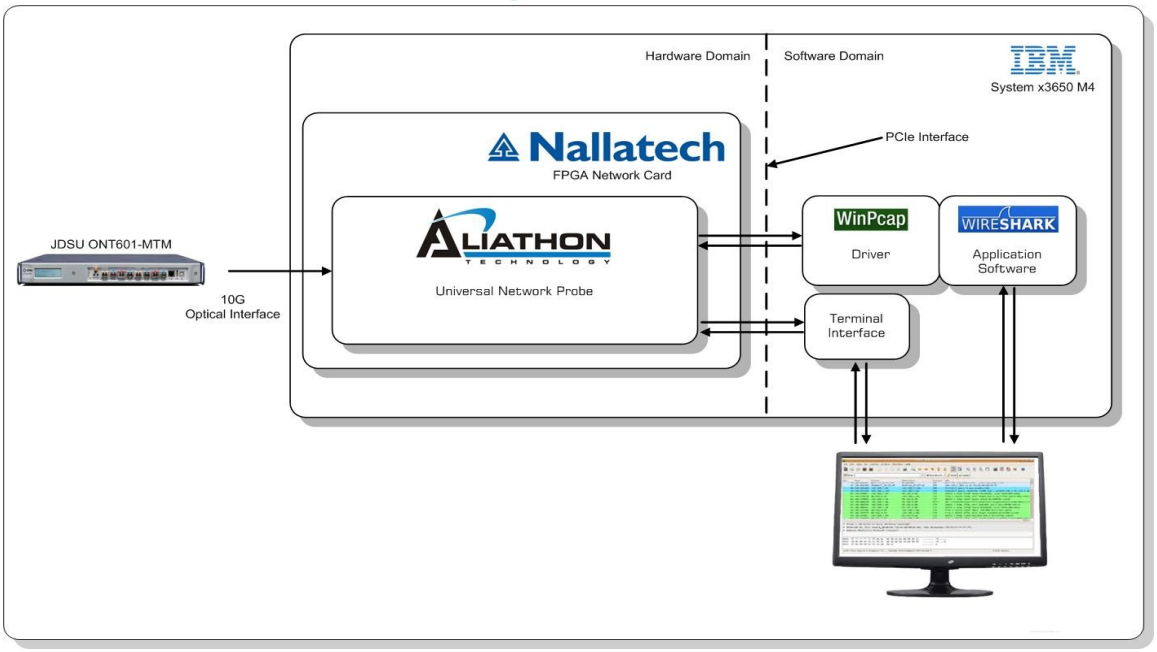
- Rapid Platform Deployment: Allows clients to concentrate their efforts on application software.
- Flexible & Feature Rich: Any TDM / packet protocols, scalable number of optical channels, FPGA/server platform & software interface.
- Cost Effective: The combination of Aliathon's IP & Nallatech's Network card gives our clients a high quality, tried & tested solution that competes with any alternative NIC card on the market.
- Future Proof: The solution can evolve to take advantage of changing market (or standards) requirements as well as being easily ported to newer FPGA device families & network cards.

System Level (IT) Benefits

Although the demo shown below used a single 10G channel of the Nallatech card, it can be applied to all 4 channels. By filling all 6 PCIe Gen-3 slots in the IBM server with 4-channel Nallatech cards the server can deliver up to **240Gbps** of real time channel processing.

In IT terms this solution offers a **dramatic reduction in system power consumption (i.e. simplified cooling)** AND **delivers significantly higher channel density per server chassis** vs. any other solution in the market place today.

Functional Block Diagram



Detailed Feature Set

Line Interface

OTN

- OTU2e or 1e

Ethernet

- 10Gb

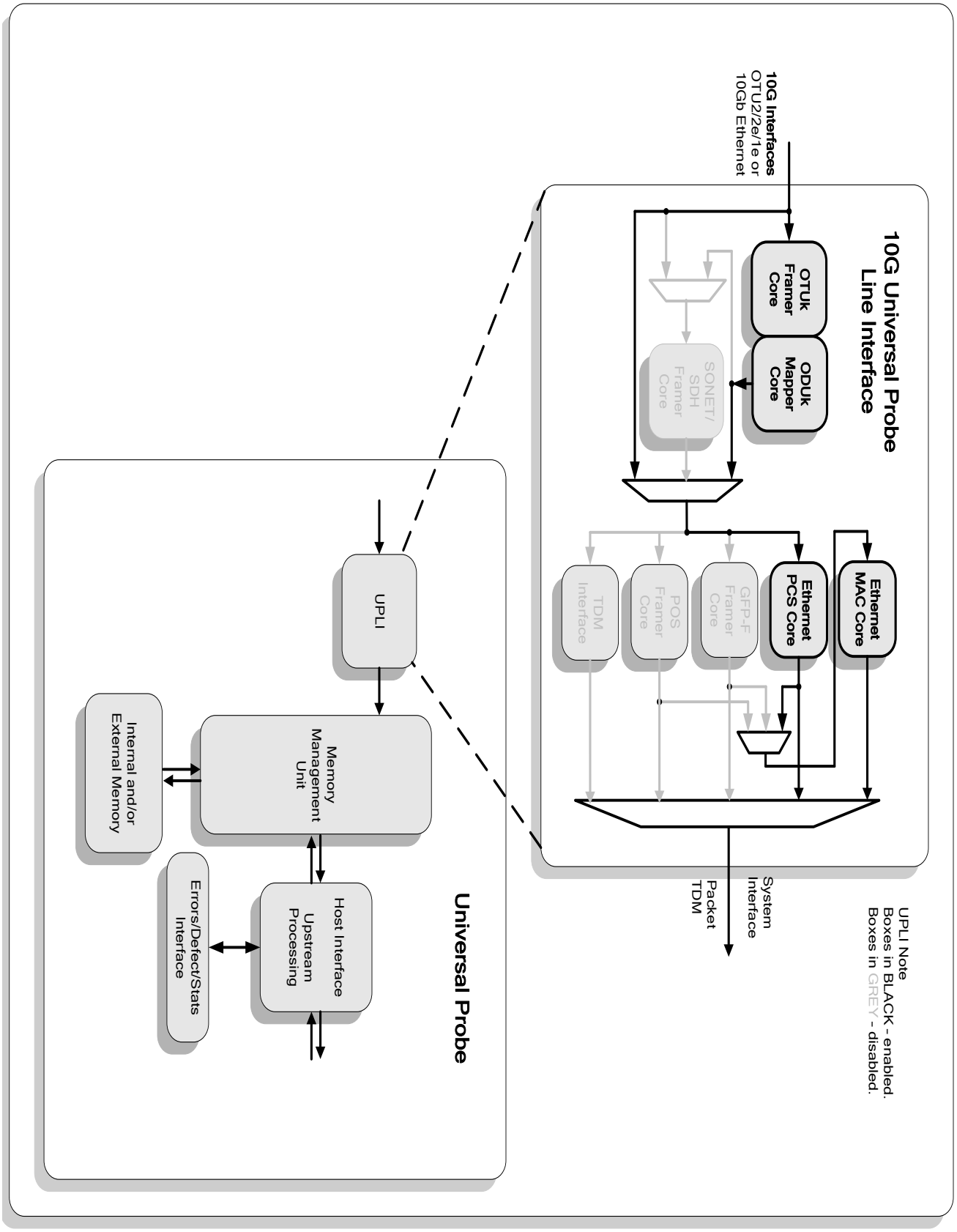
Hardware Platform

- FPGA Platform: Nallatech Inc. PCIe-287n FPGA Network Card.
- Server Chassis: IBM System X3650 M4.

Upstream Processing

- Packet Data & Frame/ packet stats (defects, errors etc) delivered to application layer via WinPcap drivers.
- Wireshark Application (user interface.

FPGA Architecture (per port)



FPGA Architecture Overview

The design can be configured to have as many universal probe line interfaces (UPLI's) as is required for the application and/or can be supported by the target FPGA. For this demo only 1 port is connected. Each UPLI feeds to the memory management unit which is configured to buffer the data in the granularity required by the upstream WinPcap/Wireshark system.

Each UPLI is individually configured with the protocol mappings as is highlighted in the diagram on page 2.

The host interface core delivers the raw data + line health info to the WinPcap/Wireshark system. The defects/errors/stats registers and data memory locations are read by the upstream processing unit over the same interface.

The client signal is deframed and demapped in accordance with the relevant standards G.709 (for bit-transparent mapping of 10GBASE-R signals) and IEEE802.3 (for LAN-PHY Ethernet)

Statistics, errors and defects are provided for all protocols and all layers of the design via Aliathon's configurable micro-processor link that can be altered to suit any standard or proprietary bus format.

Alternative 10G Datapath Options

SONET/SDH

- Native OC192/STM64 (or proprietary SDH structure).
- OC192/STM64 -> 10GbE (WANPHY Ethernet transport).
- OC192/STM64 -> PoS -> Packet (legacy packet transport).
- OC192/STM64 -> GFP-Packet (modern packet transport).

OTN

- Native OTU2/2e/1e (or proprietary OTU2k structure).
- OTU2 -> STM64 (legacy TDM transport).
- OTU2 -> STM64 -> 10GbE (SDH packet transport extender).
- OTU2 -> GFP -> Packet (legacy packet transport).
- OTU2f/1f -> FC (modern FC transport).

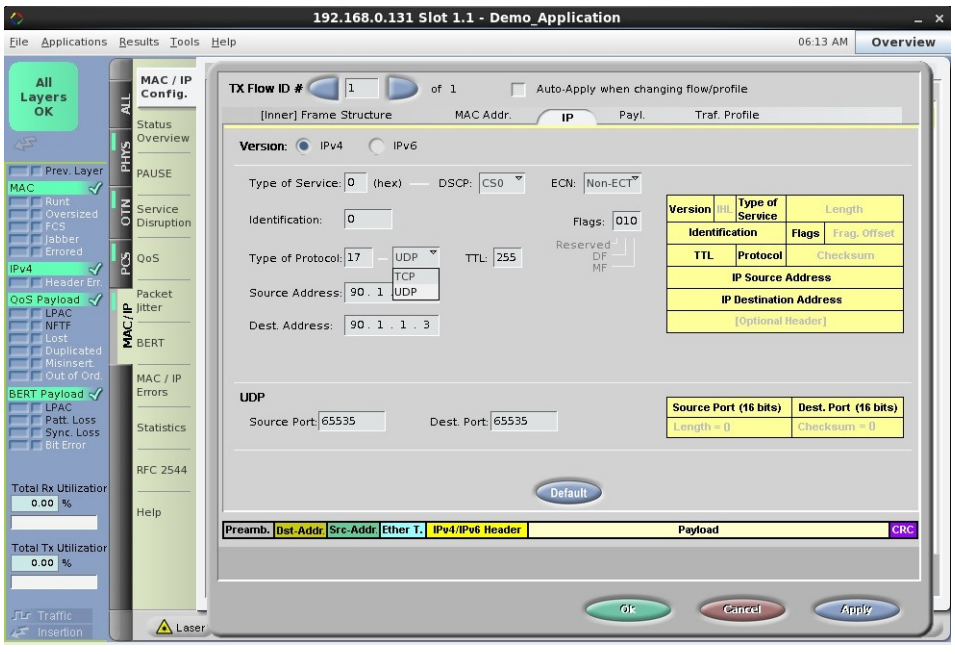
Demo Overview

Client Source (JDSU)

As per the functional diagram on page 1 the JDSU 601 MTM tester is used to provide the synthetic client signal.

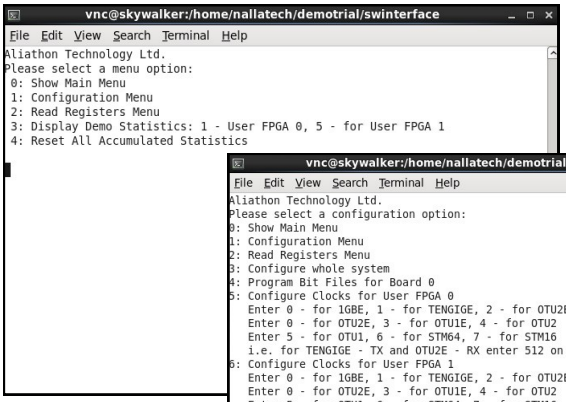
The tester is configured to provide both OTU2e/1e (containing a 10GbE client signal) and a basic 10GbE (LAN-PHY).

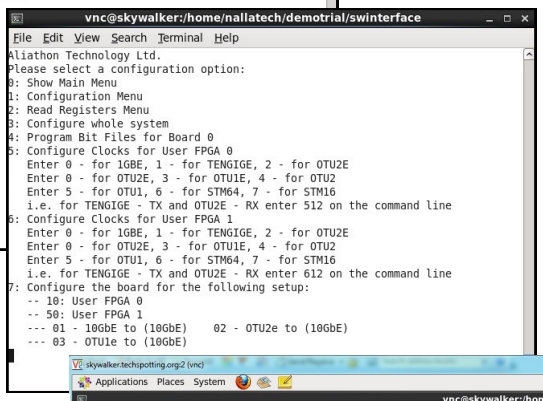
In both cases the tester is able to fully exercise the frame overhead (OTU2e/1e) and the packet header (Ethernet) by forcing errors and defects.



As an additional feature the FPGA design also adds a proprietary real-time stamp to the individual frames as they pass through the datapath (time 0 from Wireshark data capture start).

Demo Overview (Cont)





Aliathon Terminal Interface

As shown in these screenshots , the terminal interface has complete control of the demo design.

The terminal provides deep access to the FPGA registers controlling the following attributes;

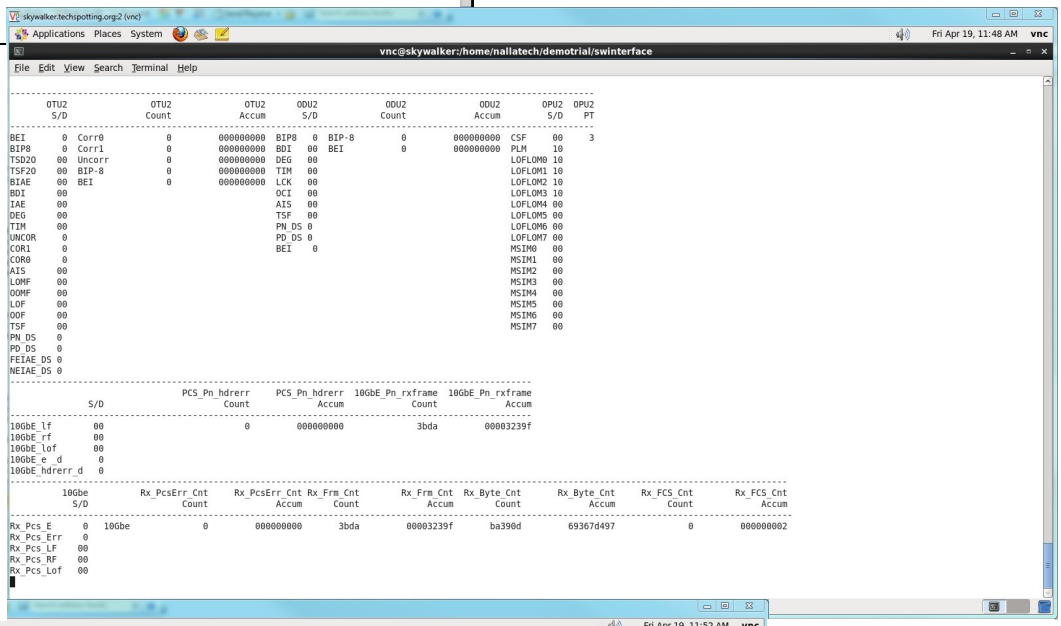
- High speed I/O.
- Client reference clocks.
- Deframing/demapping datapaths.
- Frame/packet transport statistics, defects and errors.

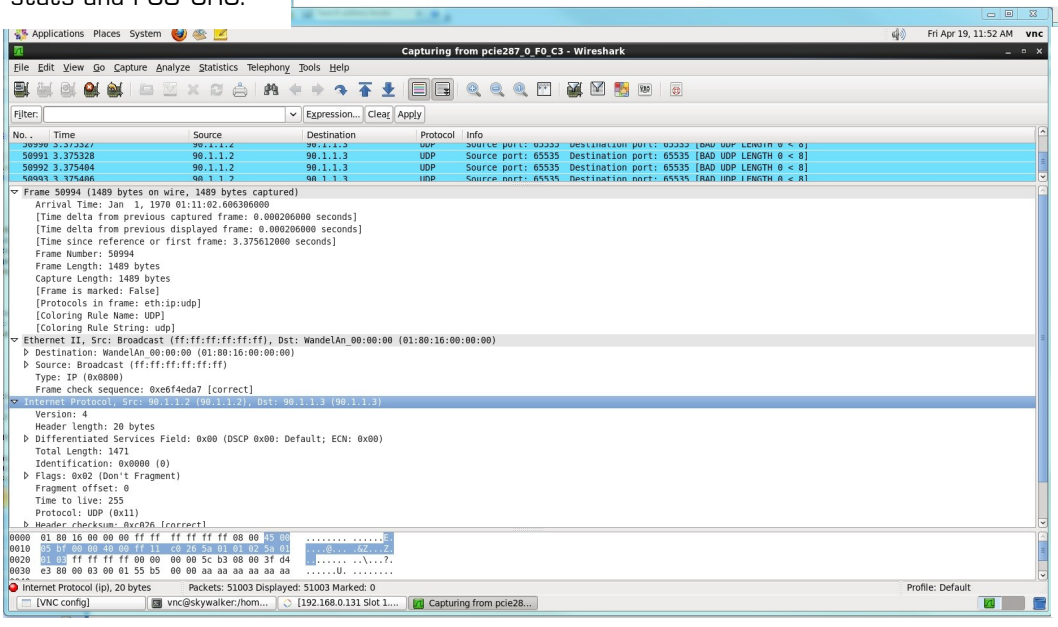
Terminal Stats Page

As described above the stats page provides register level access to the client signal transport layer statistics, defects and errors.

For OTN this means access to overhead info such as OOF, LOF, AIS, BEI and FEC performance.

For Ethernet this means access to info such as PCS stats and FCS-CRC.





Wireshark App

The Wireshark app allows us to examine the contents of the captured packets. A sample of statistics available are;

- Frame size.
- Timestamp.
- Source/ Destination.
- Protocol.
- FCS status.
- Payload content.

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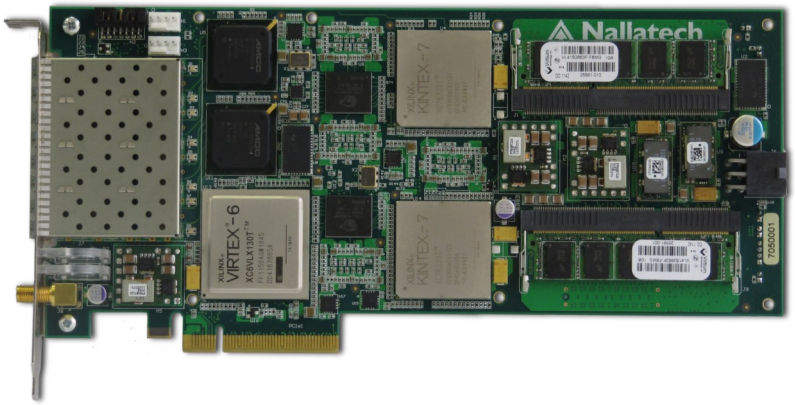
Hardware Platform

Nallatech PCIe-287N 7-Series FPGA Network Processing Card



- Full-height, full-length PCIe Gen2.
- 4 x SFP+ Ports.
  - Supporting OTN, SONET/SDH & GbE rates from 1-10G.
- Dual Xilinx Kintex-7 K325T FPGAs.
- 6 x banks of 9MB QDRI-II SRAM
- 2 x banks of 1GB DR SDRAM.

IBM x3650 System x3650 M4 Server

- 2U Rack.
- Up to two 8-core Intel Xeon E5-2600 series processors. 20MB CACHE per processor.
- Memory: Up to 768 GB via 24 slots (UDIMM/ RDIMM/LRDIMM/HyperCloud DIMM).
- Expansion: 4-6 PCIe 3, 4 PCI-X and 2 double-width PCIe (GPU).
- SAS/SATA Storage: 16TB (2.5") or 18TB (3.5").
- OS: Microsoft Windows SERVER, Red Hat Enterprise Linux, SUSE Linux Enterprise SERVER, VMWare vSphere.

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