

# MINIATURIZATION OF HEARING AID ELECTRONICS USING EMBEDDED DIE PACKAGING

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## ABSTRACT

The continuous drive to increase the density of electronic packaging began long before the invention of the transistor. This effort has grown on multiple fronts including telecommunications, aerospace, military, automotive, medical and consumer products. The hearing aid business has always demanded the use of extremely small electronic packaging due to the minimal space within the ear canal. In fact, in 1952, the first commercial device to make use of transistors was the hearing aid.

Complete hearing aid systems were created using ceramic hybrid-based system-in-package technology. In recent years hearing aid microelectronic packaging has been migrating away from ceramic hybrid-based packaging to flexible circuit-based technologies such as chip-on-flex. The introduction of wireless systems in hearing aids sharply increased the electronic component count from less than 20 per device in 2005 to more than 70 in 2010. All available space is essentially used. The densest packages yet were introduced in 2015 using embedded die modules in the smallest hearing aid sizes called *invisible-in-the-canal* or IIC. Additionally, more powerful processors and more memory are enabling sophisticated algorithms that are able to greatly improve sound quality. There continues to be a strong marketing desire to add more features to hearing products while consistently decreasing the size and visibility when worn. These added features are further increasing component count and therefore drive the need to make smaller electronic assemblies.

This paper will examine the use of second generation embedded die packaging, also called chip-in-flex, to drive significant further size reduction in custom hearing instruments over what can be achieved using chip-on-flex and ceramic hybrid-based technologies. The construction, size reduction, performance improvement, supply chain challenges, and electronic package reliability will be discussed herein [1, 2].

Key words: Embedded die, hearing aids, chip-in-flex, chip-on-flex

## INTRODUCTION

It should be obvious that consumers of today's electronic devices are looking for the smallest, thinnest and most powerful electronics available. The telecommunications industry has been a significant driver for many advancements reducing size and increasing functionality over the recent years. This trend, however, is not limited to cell phones, but applies to nearly all electronic devices such as life-sustaining implantables and wearable fitness trackers. Consequently, companies worldwide now share the common need to develop methods to increase the volumetric efficiency of electronic packaging.

A largely forgotten early adopter of cutting edge electronic packaging is the hearing aid industry, which has always concentrated on the efficiency and size of microelectronics due to the extremely limited space of the ear canal. Hearing aids were leading the market for reduced-size electronics long before cell phones were even a concept. In fact, the first commercial application for the transistor, a groundbreaking new device at the time, was a hearing instrument produced by Sonotone (model 1010) in 1952. It was a hybrid two vacuum tubes, one transistor hearing instrument measuring 3 inches (7.62 cm) by 2-3/4 inches (6.99 cm) by 1/2 inch (1.25 cm) thick. This use occurred prior to the first commercialized transistor AM radio, which wasn't introduced until 1954. Since then the technology used in hearing aids has continued to advance and successful hearing aid manufacturers have been quick to adopt the latest in microelectronic packaging technology.

Today's hearing aids, such as Starkey's Z-Series™ and SoundLens™ products, are far removed from their vacuum tube ancestors. Modern hearing aids have serious computing power, running complex hearing algorithms that have an enormous impact on a patient's quality of life. The current industry trend is continued advancement by adding more memory, more signal processing capability and more wireless functionality into the hearing aids to increase feature count and to improve performance. In order to continue to achieve this level of performance increase, the hearing aid business has consistently taken the lead in electronics size reduction. They have made the most of

emergent and leading edge technologies for the development and execution of novel 3D packaging innovations well ahead of other industries.

**BACKGROUND**

The mainstream hearing aids of the late 1990’s and early 2000’s primarily used thick film ceramic hybrid technology to make exceedingly small hearing amplifiers that consisted of digital signal processors (DSP) tied together with memory (EEPROM’s) and the required capacitors and resistors [3]. Total part count per device was typically in the neighborhood of 12 components and the pad count was usually less than 16. Both custom and standard hearing aids were made in this fashion, with the custom aids having wires soldered directly to pads on the hybrids and the standard hearing aids using hybrids that were terminated with solder pads in a ball grid array (BGA) format. These BGA’s were often soldered to moderately complex flexible printed circuit boards (FPCs) using surface mount technology (SMT) assembly [4]. Hybrids intended for standard hearing aids were typically more complex and had additional components SMT attached to the BGA surface and on occasion required cutouts on the FPCs to enable mounting.

Around 2006 ceramic hybrid technology was becoming extremely complex with the implementation of vertical interconnects (VIC) to connect multiple ceramic interconnect surfaces. Concurrently, the addition of wireless technology into hearing aids had begun. The thick film ceramic technology was no longer capable of supporting the rapidly increasing part count and required interconnect density to attach the 75 or more components necessary without increasing the package size to unacceptable dimensions. The dawn of chip-on-flex for hearing aids had begun [5].

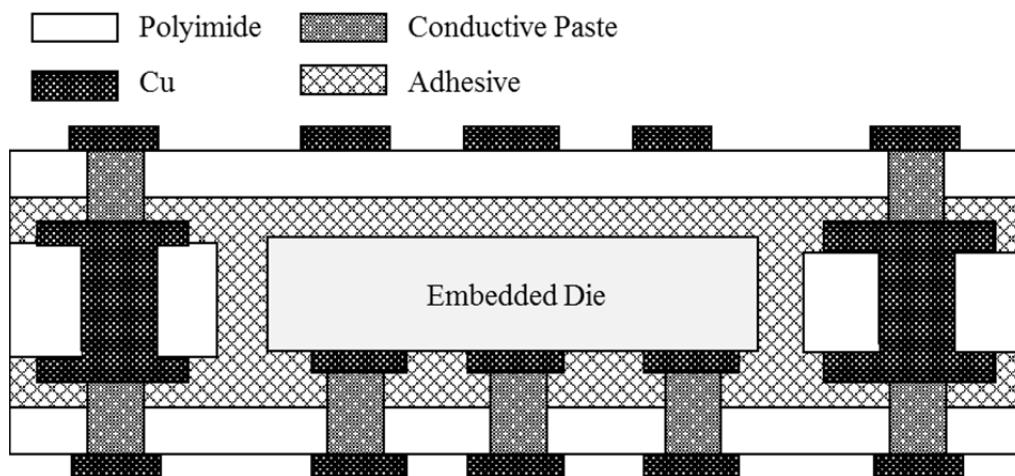
Many of the first chip-on-flex devices used four-layer FPCs having 100 um copper lines and spaces with 100 um vias and 200 um capture pads. These circuits enabled wireless hearing aids at various frequencies without thick film

hybrids [6]. Since this time additional features have continued to be added and the limits of flexible circuit technology consequently pushed to the degree that few companies can produce what is needed. Current products are now being designed with 50 um lines and spaces with 50 um vias and 150 um capture pads in four layers. Next generation chip sets will require even more aggressive (and expensive) routing density, down to 25 um lines and spaces with 50 um vias and 125 um capture pads with five or six layers.

The process of embedding components into circuit boards has been possible for a number of years. Significant performance improvements have been demonstrated by embedding capacitors adjacent to surface mounted die in very close proximity; however, cost has always been a drawback. Embedding processes have continued to improve, most recently with the development of embedding processes for active components in rigid and flexible circuits [1, 7 - 9]. The capability to embed both active and passive components now provides the advantage of significant circuit size reduction.

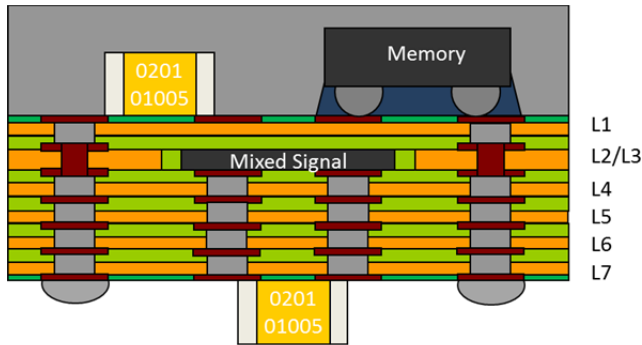
For the hearing aid industry, the combination of moving circuit complexity into an ultra-small embedded die module, referred to herein as chip-in-flex (CIF), and delaying migration to even more complex FPCs is an ideal solution. Starkey Hearing Technologies released its 1<sup>st</sup> generation embedded die package into hearing aid production in 2014. It was built for the smallest hearing aid style, the *invisible-in-the-canal*, or IIC, style. The smaller size of the circuit led to smaller IIC hearing aids, resulting in better fitting custom hearing aids for patients.

This paper will discuss the use of second generation embedded die packaging (or CIF) to drive significant further size reduction in custom hearing instruments over what can be achieved using chip-on-flex or ceramic hybrid-based technologies. The 2<sup>nd</sup> generation CIF uses a new DSP and memory chip set and pushes the design boundaries of CIF technology even further. The construction, size reduction,



**Figure 1.** Cross-sectional structure of WABE concept

performance improvement, and supply chain challenges will be discussed herein. This paper will also discuss the results of extensive reliability testing used to qualify this technology for manufacturing.



**Figure 2.** Cross-sectional structure of CIF module

### CONSTRUCTION

The second generation CIF module was fabricated using Wafer and Board Level Embedded (WABE) technology to embed die in flexible circuits followed by standard double sided SMT processing and subsequent molding, resulting in a system-in-package (SiP). WABE technology consists of a thinned embedding die and multi-layer flexible printed circuit board using a one-step lamination process with proprietary paste connection as shown in Figure 1. Multiple FPC layers encase a thin (85 um) embedding die(s) using metal paste interconnections that are fabricated with a one-step lamination process without Cu plating connections or a build-up process.

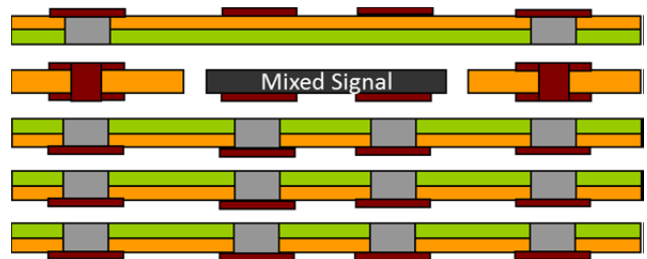
The cross-sectional structure of the CIF module and process-flow are shown in Figures 2 and 3, respectively. The embedding die has Cu terminations that help bridge the gap between the fine integrated circuit level and the wider FPC level design rules, while ensuring a robust connection by forming an intermetallic layer at the interface of the paste and Cu layers. The die thickness is much thinner than that used in standard SMT packaging, thus backside chipping and surface roughness are important parameters that must be well controlled to prevent die cracking during the die placement process, as well as to ensure module level reliability. Dice before grinding (DBG) and dry-polish processes are used for the preparation of the embedding die (while in wafer form) to minimize backside chipping and optimize surface roughness quality.

The 2<sup>nd</sup> generation CIF module consists of five single-sided FPC layers and one double-sided FPC layer which serves as a spacer layer for the embedding die. Standard roll-to-roll FPC fabrication process including photolithography and Cu etching processes are used to fabricate the individual FPC layers followed by 100% automatic optical inspection (AOI).

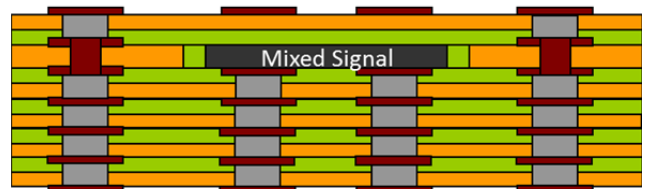
After adhesive lamination, laser drilling and paste filling processes in panel format, each individual FPC layer is set up for the alignment process (Figure 3-1). Only good FPC

layers are populated with embedding die; rejected layers which are identified by AOI during pre-processing are excluded from the embedding die placement operation preventing expensive Known Good Dies (KGD) from being wasted. One FPC layer has a reference fiducial. Subsequent FPC layers utilize this fiducial to ensure accurate optical alignment and eliminate accumulated registration tolerances in the resultant multi-layer FPC, regardless of the number of FPC layers in the finished CIF module (Figure 3-2).

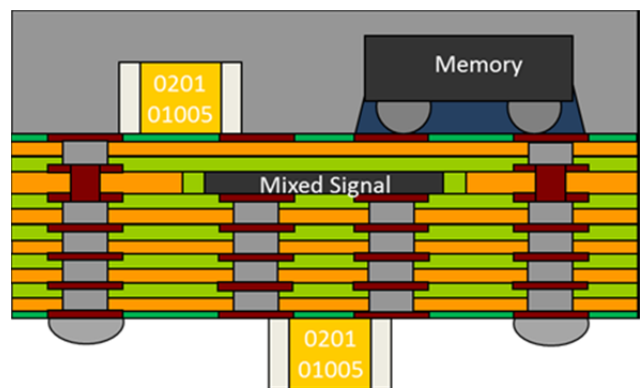
Standard SMT processing is then used to mount BGA die and passive components on the FPC surface in a strip format. Strips are subsequently molded to add protection to the surface mounted components. The molding material also provides a flat surface to support singulation and testing operations (Figure 3-3). Module identification and marking



**Figure 3-1.** Individual FPC preparation and alignment



**Figure 3-2.** Cross-sectional structure after cure process



**Figure 3-3.** Finished module with SMT and molding

are placed on top of the mold surface by a laser operation to ensure traceability.

### SIZE REDUCTION OBTAINED

Prior to 2015, IIC (*invisible-in-the-canal*) hearing devices used an electronics hybrid that was originally designed for use in CIC (*completely-in-the-canal*) hearing aids. The IIC

**Table 1.** Dimensions and volumes of the three generations of electronic packages

Package	Length (mm)	Width (mm)	Thickness (mm)	Volume (mm <sup>3</sup> )
Ceramic hybrid	5.74	3.45	2.43	48.12
1 <sup>st</sup> generation CIF	4.39	3.44	1.33	20.09
2 <sup>nd</sup> generation CIF	4.11	3.28	1.29	17.39

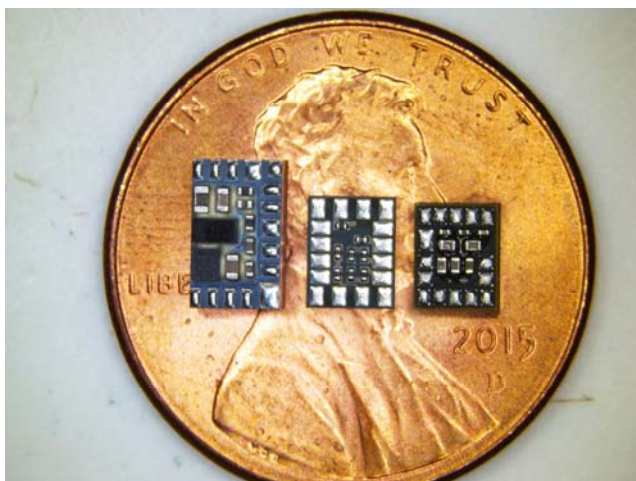
hearing devices are smaller than the CIC, designed to fit beyond the second bend of the ear canal, whereas the CIC hearing devices sit at the face of the ear canal and, while discrete, are not completely invisible. The hybrid required modification by chamfering the top mold material using a custom-made miniature router to facilitate the hybrid fitting inside the smaller IIC shell. These altered hybrids still resulted in less than desirable fit rates of the IIC in patient ears. The reduced size of the first embedded die module for use in IIC hearing aids introduced in 2015 improved the fit rates substantially. The original electronic module was 5.74 mm x 3.45 mm by 2.43 mm thick. The new electronic module was 4.39 mm x 3.44 mm by 1.325 mm thick, resulting in a 60% volumetric size reduction. The second generation device was 4.11 mm x 3.28 mm by 1.29 mm thick. The second generation device saved an additional 13% by volume over the first generation, and 64% volumetric size reduction over the original hybrid package. See Table 1 for dimensions and volumes of the three generations of electronic packages. Figure 4 shows a side-by-side comparison of the three devices in relation to a US one cent coin. Figure 5 offers close-up images of the 1<sup>st</sup> and 2<sup>nd</sup> generation modules for direct comparison.

### PERFORMANCE IMPROVEMENT

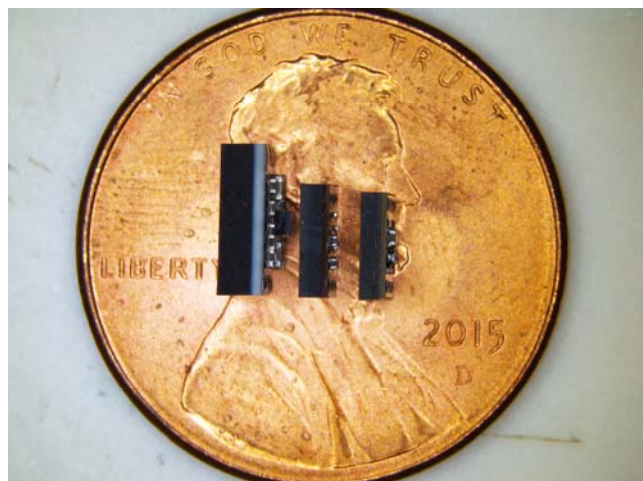
The second generation embedded die module uses the same Fujikura WABE process as the first generation as discussed above. However, the second generation uses a DSP chip with four cores and more onboard memory as well as 2 MB of EPROM-based memory instead of the 1 MB used in the

first generation SiP. The first generation part used a clock frequency of 5.12 MHz and had a performance metric of 65 MIPS in total. The second generation DSP operated at 15.36 MHz yielding 375 MIPS. This is a six-fold improvement in throughput. There was no packaging performance change difference between the two modules. However, when comparing the second generation module to a ceramic hybrid based SiP using the same chip set a huge difference is observed.

The module using WABE technology is 40% smaller (17.03 mm<sup>3</sup> versus 28.4 mm<sup>3</sup>) and requires fewer passive devices because the copper/polyimide in the WABE module is substantially better than silver/glass thick film materials used in the ceramic hybrid module. The smallest silver traces are 100 um wide at a thickness of 12 um yielding a resistivity of 2.5 – 30 mOhms/square. The WABE module copper traces are as small as 40 um at a 12 um thickness yielding about 1.4 mOhms/square resistivity. With the WABE technology smaller traces and spaces can be used while maintaining the electrical performance. The smaller features enabled components to be placed closer together resulting in shorter power and ground traces. These shorter traces in turn lowered parasitic resistance and inductance that cause electrical power noise. Due to these improvements in the WABE design the number of required decoupling capacitors could be reduced contributing to the overall package's large size reduction.

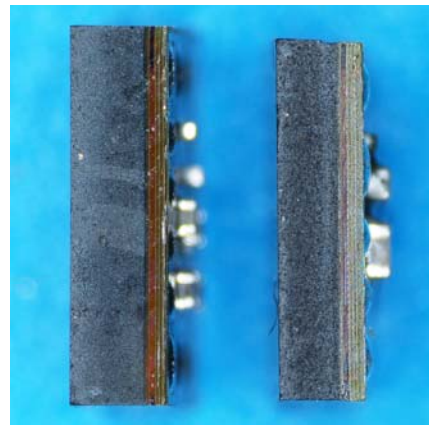
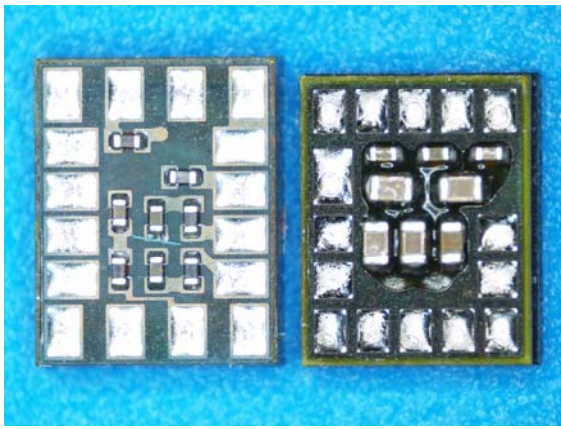


a)



b)

**Figure 4.** a) Top view of circa 2009 hybrid (left), top view of 1<sup>st</sup> generation CIF module (middle); top view of 2<sup>nd</sup> generation CIF module (right) b) Side view of circa 2009 hybrid (left), side view of 1<sup>st</sup> generation CIF module (middle); side view of 2<sup>nd</sup> generation CIF module (right)



a) Top view of 1<sup>st</sup> generation CIF module (left); top view of 2<sup>nd</sup> generation CIF module (right) b) side view of 1<sup>st</sup> generation CIF module (left); side view of 2<sup>nd</sup> generation CIF module (right)

Additionally, because the WABE technology has the processor chip embedded into the flexible circuit layers there is no need to underfill the chip. The underfilling operation adds stress to the system that bends the processor chip and changes its performance. This can be seen in the ceramic hybrid based SiP where extra steps are required to mitigate unwanted stress related clock shifting. Analysis revealed two times more stress related clock shifting in the ceramic hybrid versus the WABE embedded die module.

#### CHANGES IN SUPPLY CHAIN

The IIC CIF module achieved an ultra-small package size and performance improvements as a result of using WABE technology that required a custom package design, proprietary embedding die preparation, and cross-industrial front and backend processing at subcontractors. This strongly impacted the design, the logistics, and the testing as compared to a standard SMT package or a wafer level package.

The package design integrated many often independent processes such as the wafer process flow, the formation of a Cu pattern re-distribution layer (RDL) on the wafer, several FPC Cu layers, location and placement of embedding die, and the SiP structure. Major considerations were the mixed signal performance of the DSP and package size that were impacted by design rules driven towards their lower acceptable limits. Therefore, the complexity of this design versus conventional packages makes a concurrent design approach important to achieve optimum design/performance as well as a rapid design cycle time.

Usually the substrate is the only custom designed component for typical SiP modules and other components including the die and passives are available in tape and reel format as off-the-shelf components. This was not the case with this module because Cu terminations are required on embedding die for WABE technology. This meant that the normal wafer level bumping process, subsequent testing processes, and dicing operations needed to change. The

second generation CIF module had additional backend logistics complexity (subcontractor change) because the DSP wafer changed from the previous generation product's 200 mm format to a 300 mm format.

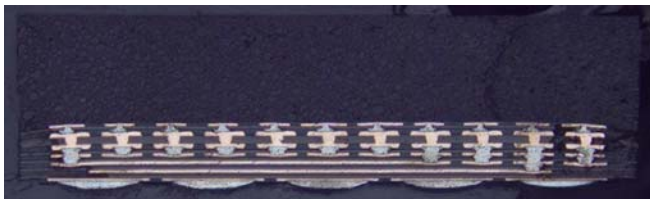
Testing of the wafer also changed to accommodate the new RDL process on 300 mm wafers. The embedding die was tested at the wafer supplier before RDL processing to identify good die. Known good die are populated during the WABE process and open/short testing is performed after embedding to confirm the embedding process quality. Final test is performed at a backend subcontractor. The additional open/short test after the SiP process is completed to differentiate at what steps yield loss occurs. This is important since multiple subcontractors are needed to build this module.

#### EMBEDDED DIE MODULE RELIABILITY

Extensive reliability testing was performed on this technology. The evaluation included microsectioning, 3D x-ray, accelerated aging testing, hearing aid assembly/solder simulation testing, thermal shock testing, acoustic scanning, light sensitivity testing and ESD testing. The results are discussed in the following sections. Additional tests that were performed included packaging and labeling characterization, device electrical testing, visual inspection, and dimensional analysis.

#### Microsection

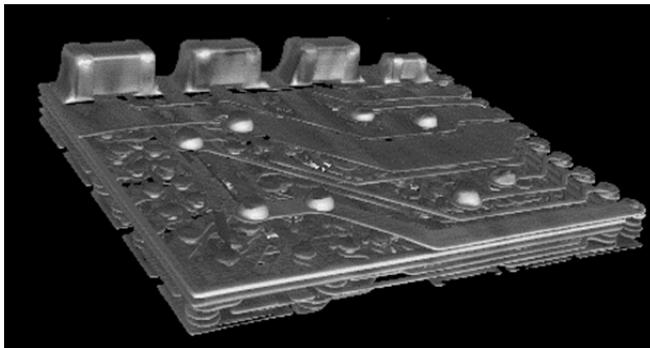
Microsectioning is performed on parts to characterize and baseline the internal features of the SiP module, its components and their connections. A sampling of three circuits were micro-sectioned and there were no abnormalities observed. See Figure 6.



**Figure 6.** Microsection of 2<sup>nd</sup> generation CIF

### 3D X-Ray

3D x-ray is performed to verify the internal construction of circuits: structure, layout, layer registration, solder shape, etc. are reviewed. A sampling of two parts were x-rayed. There were no issues observed in x-ray imaging. See Figure 7 for an example 3D x-ray of one CIF.



**Figure 7.** 3D X-ray of 2<sup>nd</sup> generation CIF

### Accelerated Aging

Accelerated aging testing of electronic components evaluates the field integrity and longevity of the electronics. The test simulates operation of the circuit in a climate of extreme heat and humidity over a period of several years, monitoring for dendrite growth and changes in bias current. Wires were soldered to a positive pad and a ground pad of the test circuits. These wires were soldered to the appropriate connections on a test board.

A sampling of 32 circuits was placed in an environmental chamber and a bias voltage of +1.25 V applied to the parts via a sealed cable port. The chamber parameters were set to 85 °C and 85% relative humidity. A chart recorder was connected to record heat and humidity levels during the test. The current of each circuit was examined every 7-10 seconds, checking regularly for anomalies, such as dendritic growth. All samples were run for an initial 168 hours, then continued on to 500 hours. No failures occurred during the 500 hours. Sixteen of the parts were then continued for 1000 hours. All circuits passed the electrical testing and had no visual evidence of external dendritic growth following 1000 hours of exposure.

### Hearing Aid Assembly/Solder Simulation Testing

The purpose of the hearing aid assembly/solder simulation test is to simulate the stresses (thermal and/or chemical) that a device will be exposed to during the actual SMT and hearing aid assembly processes. The devices were baked in an industrial oven for two hours at 110 °C to remove any

moisture. Flux was then applied to the user pads, and a soldering iron at 650 °F touched to each pad for two seconds, and then removed from the pad for two seconds, repeating this cycle twice. A sampling of 12 parts were used for the hearing aid assembly/ solder simulation test. All CIF modules exhibited normal electrical testing following the soldering process.

### Thermal Shock

Thermal shock testing is used to demonstrate the thermal and mechanical robustness of typical assemblies. There are no definitive “pass/fail” criteria for this test, rather it is used for comparison testing of old versus new components and for benchmarking competitive products. De-ionized water was used for all testing. A sampling of 28 CIF modules were first exposed to an ice-cold water bath for a minimum of one minute, then immediately transferred into a boiling water bath for a minimum of one minute. This cycle was repeated 20 times. A visual and acoustic scanning inspection of the 28 modules post-exposure showed no evidence of delamination or damaged solder joints. There was also no variation in the electrical tests of the modules pre- versus post- exposure.

### Acoustic Scanning

Acoustic scanning is performed on the circuits in order to characterize and baseline the internal features of the SiP modules and to check for voids and delamination. A total of 20 circuits were tested: five new samples, five from accelerated aging tests, five from thermal shock tests and five from soldering simulation tests. There were no abnormalities observed through acoustic scanning.

### Light Sensitivity

The light sensitivity test is designed to determine if the electric and/or acoustic functions of a device are adversely affected by exposure to sunlight. One device was wired so that it was configured for current drain and acoustic testing. A baseline measurement of the current drain and acoustic response was measured and recorded without a light source present. The device was then exposed for one minute to a light source of 12,000+/-500 foot candles as recorded by a light meter. During the exposure the current drain and acoustic response were again measured and recorded. No distortion was observed in the current drains or acoustic responses of the device, indicating the CIF module did not exhibit any light sensitivity.

### ESD Testing

Electrostatic discharge (ESD) can cause device failure and this test is used to characterize the susceptibility of an electronic component to ESD damage. MIL-STD 883F, Method 3015.7 was used for all tests. A sampling of three modules was used and all parts passed the test without issue.

### CONCLUSIONS

The second generation embedded die module using WABE technology reduced module size by 13% over the first generation, even though memory was doubled, and by 40%

as compared to ceramic hybrid based packaging of the same new chip set. There was a huge 64% volumetric size reduction as compared to the original generation 1 SiP. Performance improved by a factor of six. Stress related performance changes associated with packaging were reduced by a factor of two. Extensive reliability testing was performed with all tests passed without issue. Embedded die modules using WABE technology has enabled continued electronic packaging size reduction while at the same time providing improved performance.

#### **ACKNOWLEDGEMENTS**

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