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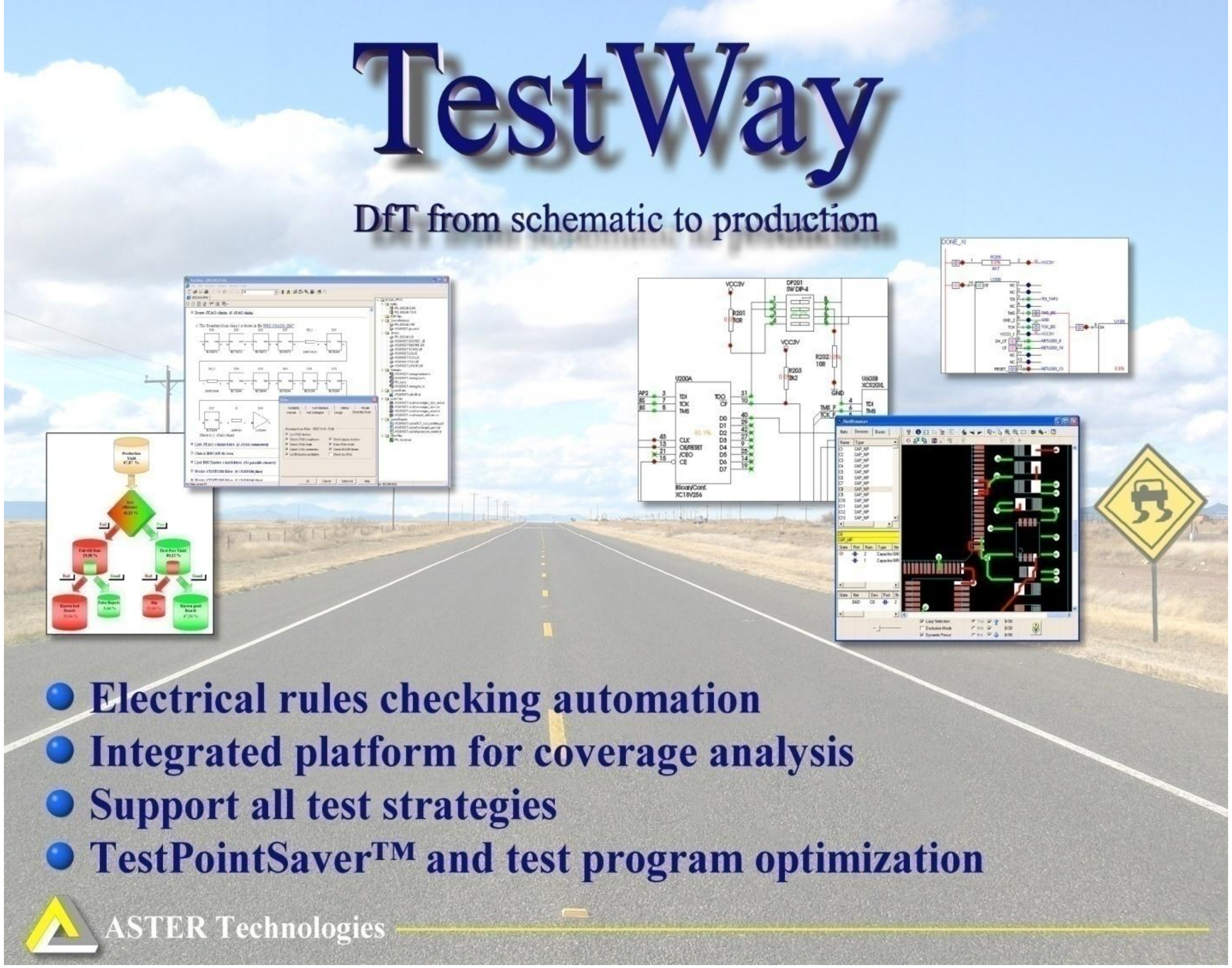
# Electrical DfT & Test Coverage Analysis Techniques for PCB's & System

**TestWay 2015**

- TestWay Objectives
- Support
- Updated eTraining
- Embedded HELP
- OS Support
- Solution convergence
- CAD import
- Test Point ➔ CAD
- Probe Analyzer
- CAD translation
- Test Coverage
- Tester exporters
- Script & report
- CAD Compare
- System viewer
- twDocumentor
- twECO



TestWay

DfT from schematic to production

- Electrical rules checking automation
- Integrated platform for coverage analysis
- Support all test strategies
- TestPointSaver™ and test program optimization

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## TestWay - New features for 2015

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# TestWay Objectives

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- ✓ DfT from schematic to production
- ✓ Electrical rules checking automation
- ✓ Integrated platform for coverage estimation and measurement
- ✓ TestPointSaver™ and test program optimization
- ✓ Test, inspection and assembly machine exporters
- ✓ “Plug-in” integration into third-party tools

AIRBUS
Alcatel·Lucent
Continental
AREVA
EADS
hager
KEYSIGHT TECHNOLOGIES
MBDA MISSILE SYSTEMS
Microsoft
Parrot
Rockwell Collins
Schneider Electric
SAGEM
SIEMENS
THALES
ASTEELFLASH GROUP
éolane
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# 58 experts all over the globe

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CELEBRATING 21 YEARS 1993-2014

# Updated Web Support

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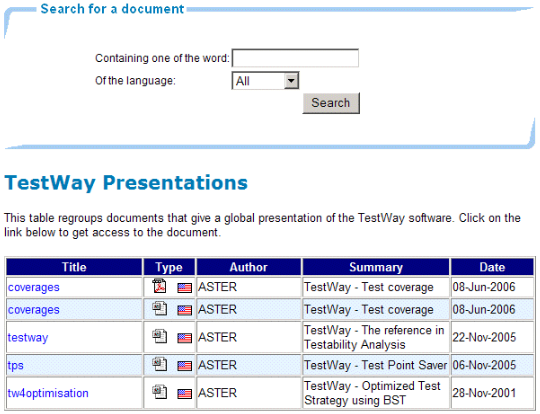


Search for a document

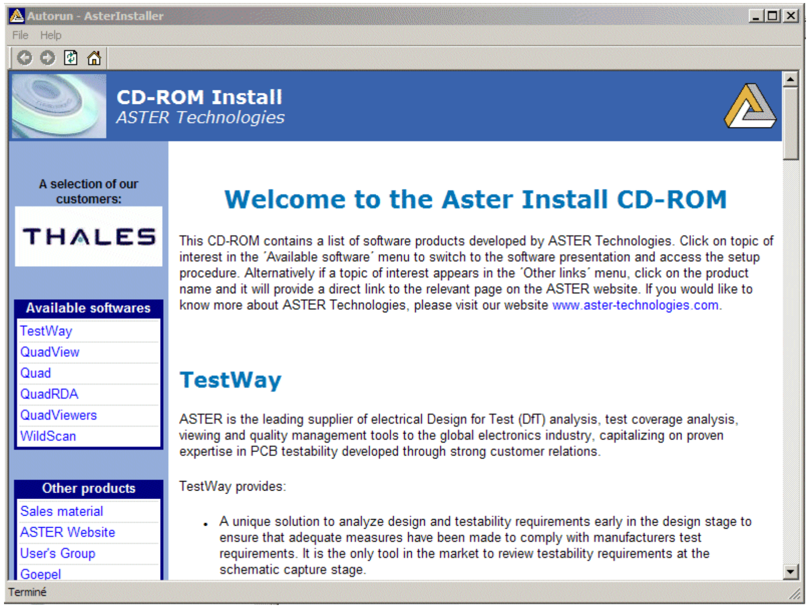
Containing one of the word:

Of the language: All

### TestWay Presentations

This table regroups documents that give a global presentation of the TestWay software. Click on the link below to get access to the document.

| Title | Type | Author | Summary | Date |
|---|---|---|---|---|
| coverages | | ASTER | TestWay - Test coverage | 08-Jun-2006 |
| coverages | | ASTER | TestWay - Test coverage | 08-Jun-2006 |
| testway | | ASTER | TestWay - The reference in Testability Analysis | 22-Nov-2005 |
| tps | | ASTER | TestWay - Test Point Saver | 06-Nov-2005 |
| tw4optimisation | | ASTER | TestWay - Optimized Test Strategy using BST | 28-Nov-2001 |



Welcome to the Aster Install CD-ROM

This CD-ROM contains a list of software products developed by ASTER Technologies. Click on topic of interest in the 'Available software' menu to switch to the software presentation and access the setup procedure. Alternatively if a topic of interest appears in the 'Other links' menu, click on the product name and it will provide a direct link to the relevant page on the ASTER website. If you would like to know more about ASTER Technologies, please visit our website www.aster-technologies.com.

TestWay

ASTER is the leading supplier of electrical Design for Test (DfT) analysis, test coverage analysis, viewing and quality management tools to the global electronics industry, capitalizing on proven expertise in PCB testability developed through strong customer relations.

TestWay provides:

- A unique solution to analyze design and testability requirements early in the design stage to ensure that adequate measures have been made to comply with manufacturers test requirements. It is the only tool in the market to review testability requirements at the schematic capture stage.

- Visit www.aster-technologies.com/support
- Simply login with your license file
- Easy-to-navigate through the ASTER knowledge database. Hundreds of application notes accessible with the embedded search engine

# Updated eTraining

- eTraining is a document that presents the best way to perform a TestWay analysis
  - ✓ All steps are described in detail
  - ✓ Includes exercises on demo board
- Periodically update your competence on TestWay
- Easy to download from Web Support
- Designed to drill-down on your point of interest

# Embedded HELP

- The updated help grants direct access to key information
- HTML helps available on networks new

- Press  for more information

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# OS support

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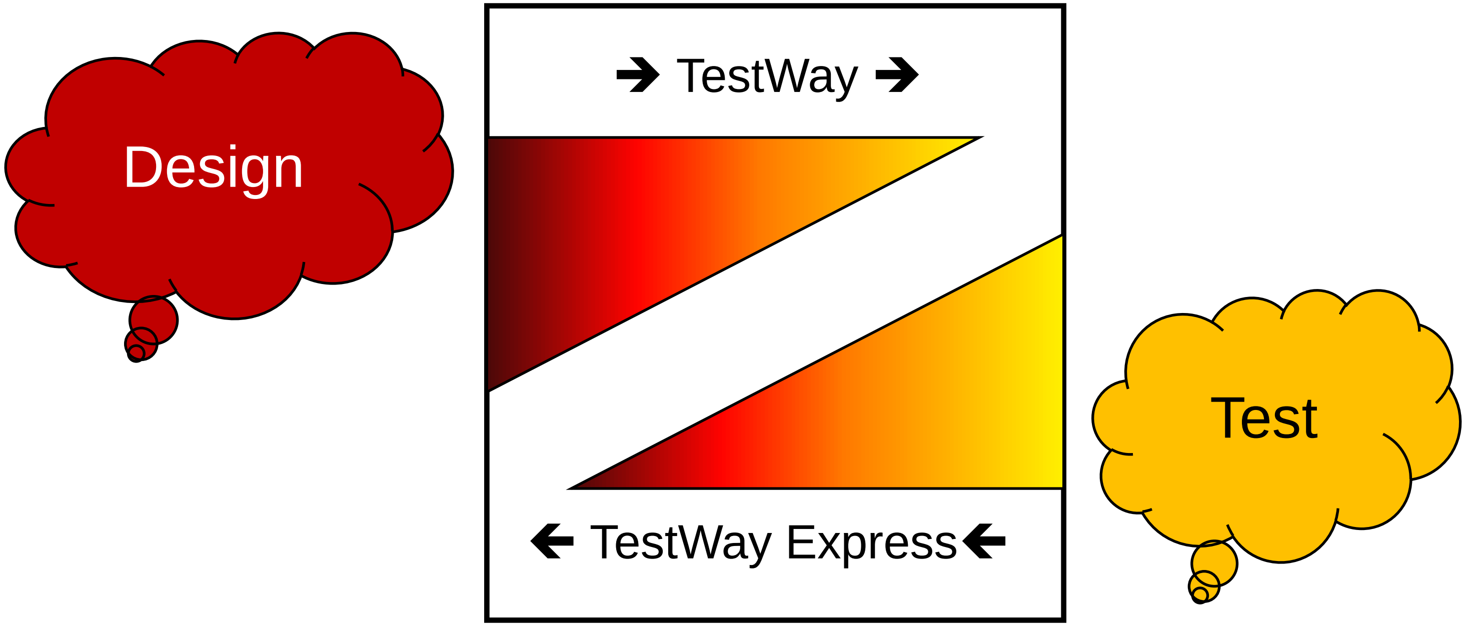
➭ TestWay is validated for the following OS:

- ✓ Windows 2000, Windows 2003
- ✓ Windows XP, VISTA 32-bit and 64-bit
- ✓ Windows 7 32-bit and 64-bit
- ✓ Windows 8 32-bit and 64-bit
- ✓ new Windows 10 32-bit and 64-bit

- ✓ Additional LAN license support is provided for Virtual platforms:
  - Citrix
  - VMware

# Solution convergence

- TestWay Express introduces the new vision of TestWay functionality
  - ✓ Intuitive user interface for new and occasional users
  - ✓ Revisit from test to design validation
  - ✓ TestWay Express is gaining all TestWay features in order to unify the products



# Solution convergence

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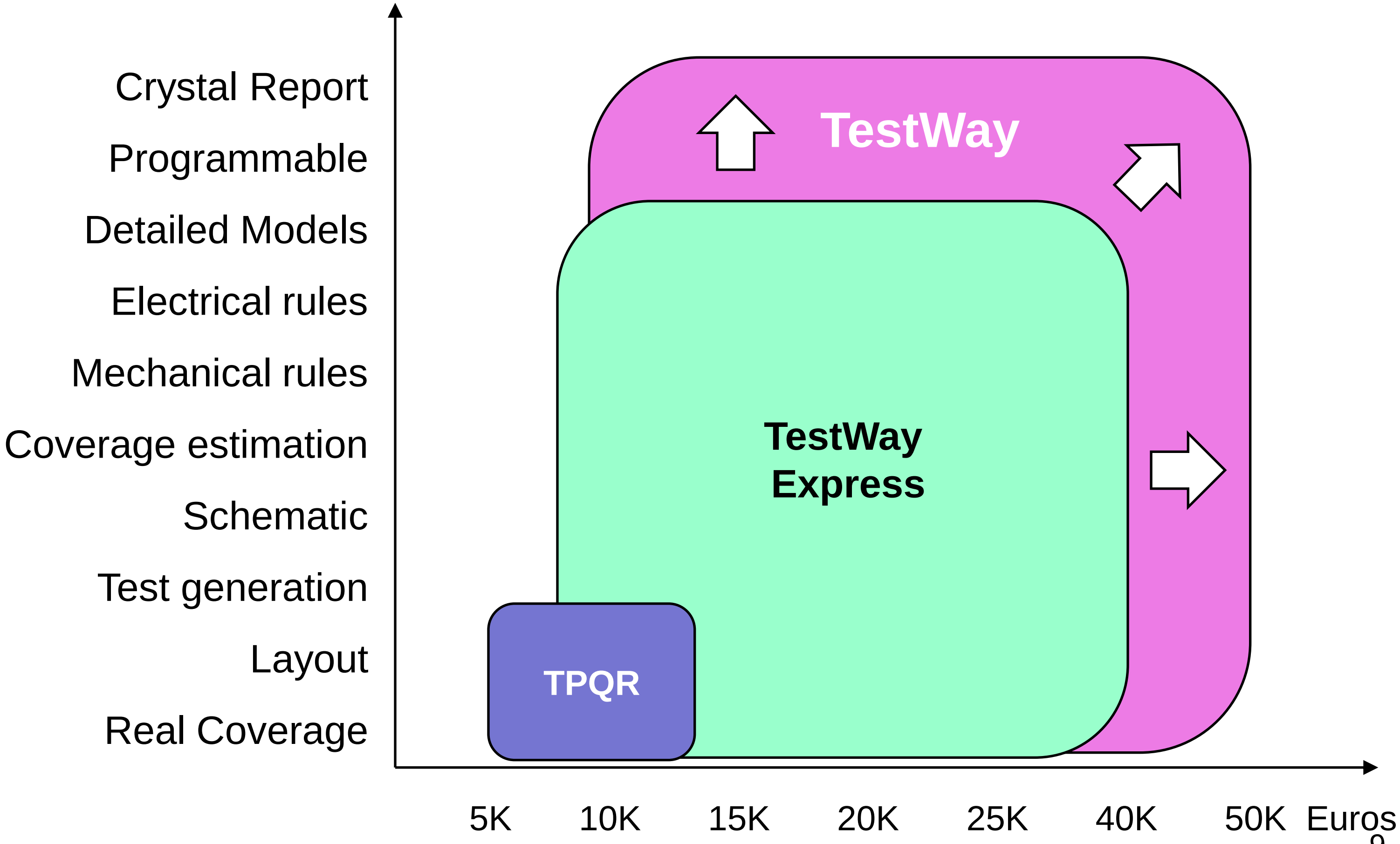
- Price range depending on product configuration (one function ⇔ one price)



# Solution convergence

- New features for 2015
  - ✓ Import Test Points as a separate file (Job setup)
  - ✓ Management of Not Populated devices (identification with Job Setup, rules checking)
  - ✓ Modifier & merger (Job setup)
  - ✓ Advanced "Project Bar"
  - ✓ Model compiler as part of the modelization pack

new

- Point of attention for 2016
  - ✓ New architecture for component modelization (Cross-references, Master libraries, DES Libraries)

- All other functions of TestWay and twExpress are already fully portable from one application to the other

# Solution convergence

- From version 3.8, TestWay licenses that include QuadView Classic, may also run twExpress

- TestWay ➔ twExpress
  - ✓ Take benefits from the TWL file produced by TestWay to enhance the twExpress project with modeling information

- twExpress ➔ TestWay
  - ✓ Select BOMDATA.ASC as Bill Of Materials
  - ✓ Select the rule « Load Test Probe file » to import the ProbeAnalyzer report

# CAD Import

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- TestWay supports all major CAD formats including netlist, schematic and layout
- All TestWay importers are now available within twExpress and QuadView
- CadBridge license option allows the use of allCad on all ASTER’s software new

# Access requirements back-annotation

- The back-annotation process creates a report that will be imported into the target CAD system to transfer test access requirements prior to the layout

| **Script** | Description |
|---|---|
| **camcad.scr** | Back-annotation script for CAMCAD. |
| **fabmastr.scr** | Back-annotation script for FabMaster or TestExpert. |
| **allegro.scr** | Back-annotation script for Cadence-Allegro |
| **cr5000.scr** | Back-annotation script for Zuken-CR5000 |
| **expedition.scr** | Back-annotation for Mentor-Expedition |
| **mentor.scr** | Back-annotation for Mentor-Board Station |
| **orcad.scr** | Back-annotation script for Orcad-Schematic Capture |
| **unicad.scr** | Back-annotation script for Cadence-Unicad |

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# ProbeAnalyzer

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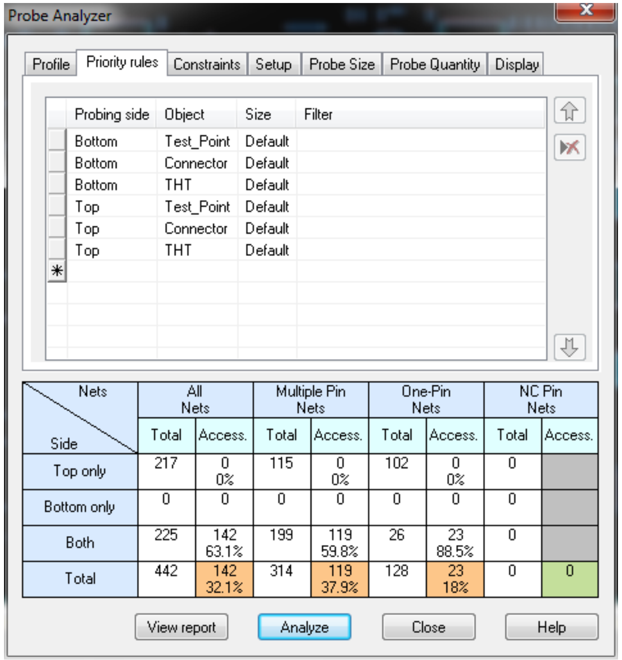
➬ The ProbeAnalyzer determines the probe access to be used for coverage estimation and test generation

- ✓ Mechanical constraints (mils or mm)
- ✓ Customer rules driven
- new ✓ Advanced customer filter
- ✓ Support of Agilent Bead Probes
- ✓ Solder mask management
- ✓ Customer defined probe sizes (100mils, 75mils, …)
- ✓ Accessibility reports
- new ✓ Mechanical drawings in DXF format

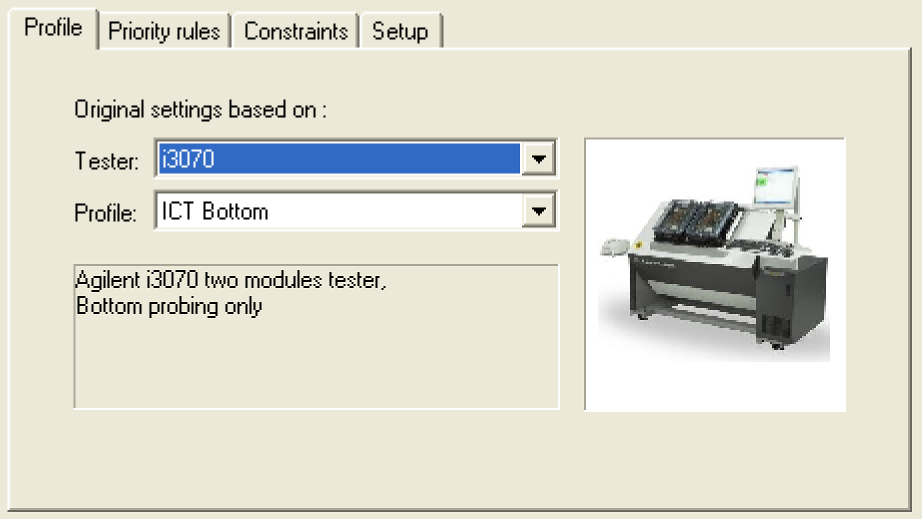


| Probing side | Object | Size | Filter |
|---|---|---|---|
| Bottom | Test_Point | Default | |
| Bottom | Connector | Default | |
| Bottom | THT | Default | |
| Top | Test_Point | Default | |
| Top | Connector | Default | |
| Top | THT | Default | |

| Nets / Side | All Nets | | Multiple Pin Nets | | One-Pin Nets | | NC Pin Nets | |
|---|---|---|---|---|---|---|---|---|
| | Total | Access. | Total | Access. | Total | Access. | Total | Access. |
| Top only | 217 | 0<br>0% | 115 | 0<br>0% | 102 | 0<br>0% | 0 | |
| Bottom only | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Both | 225 | 142<br>63.1% | 199 | 119<br>59.8% | 26 | 23<br>88.5% | 0 | |
| Total | 442 | 142<br>32.1% | 314 | 119<br>37.9% | 128 | 23<br>18% | 0 | 0 |

# ProbeAnalyzer

- Select the ProbeAnalyzer profile that fits perfectly with the test system



Original settings based on :

Tester: i3070

Profile: ICT Bottom

Agilent i3070 two modules tester,
Bottom probing only

- Create custom profiles (VISAROOT:strategy*.pa)

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# ProbeAnalyzer

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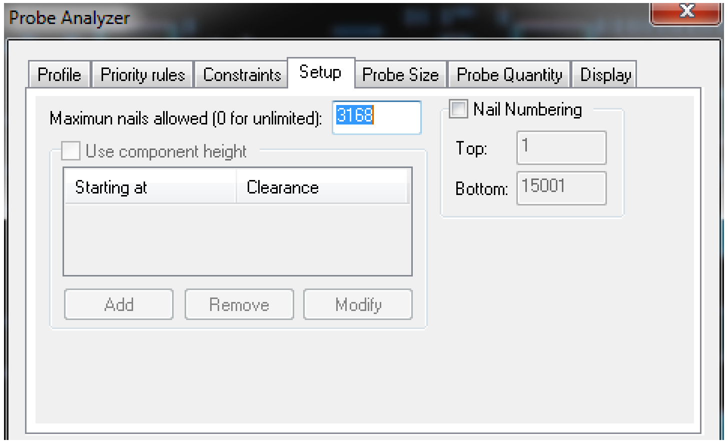
## ↳ Advanced features:

new



Maximun nails allowed (0 for unlimited): 3168

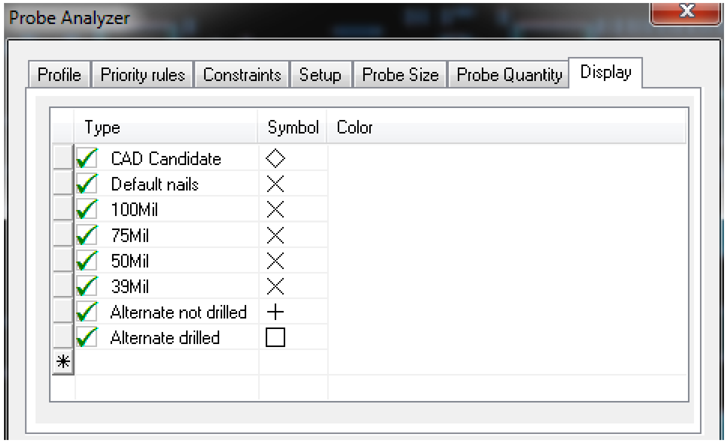
☐ Use component height

| Starting at | Clearance |
|---|---|

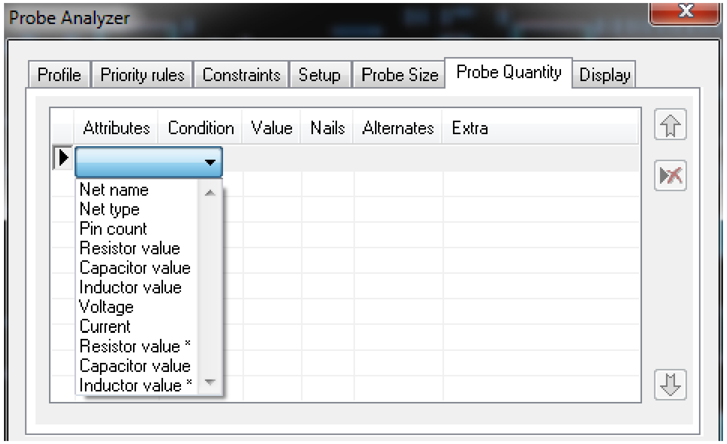
☐ Nail Numbering

Top: 1

Bottom: 15001

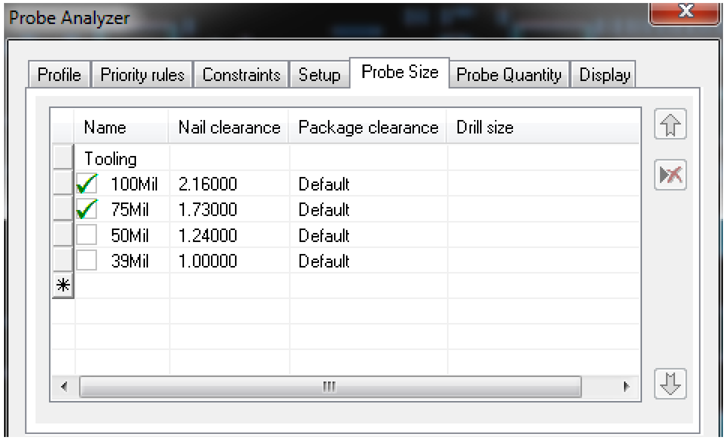


| | Type | Symbol | Color |
|---|---|---|---|
| ☑ | CAD Candidate | ◇ | |
| ☑ | Default nails | ✕ | |
| ☑ | 100Mil | ✕ | |
| ☑ | 75Mil | ✕ | |
| ☑ | 50Mil | ✕ | |
| ☑ | 39Mil | ✕ | |
| ☑ | Alternate not drilled | + | |
| ☑ | Alternate drilled | □ | |
| * | | | |



| Attributes | Condition | Value | Nails | Alternates | Extra |
|---|---|---|---|---|---|

Net name
Net type
Pin count
Resistor value
Capacitor value
Inductor value
Voltage
Current
Resistor value *
Capacitor value
Inductor value *



| | Name | Nail clearance | Package clearance | Drill size |
|---|---|---|---|---|
| | Tooling | | | |
| ☑ | 100Mil | 2.16000 | Default | |
| ☑ | 75Mil | 1.73000 | Default | |
| ☐ | 50Mil | 1.24000 | Default | |
| ☐ | 39Mil | 1.00000 | Default | |
| * | | | | |

# CAD converter

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- TestWay can convert any proprietary CAD format to GenCAD, FATF, **IPC356, EDIF20, Tango, RNIF…**

**CAD Export** ⏩

- The exported layout file includes all PCB information: routes (trace), parts, shapes, nets, etc
- These CAD formats are suitable for electronic data interchange. The primary focus is Printed Circuit Board (PCB) assembly and testing

# Marker File

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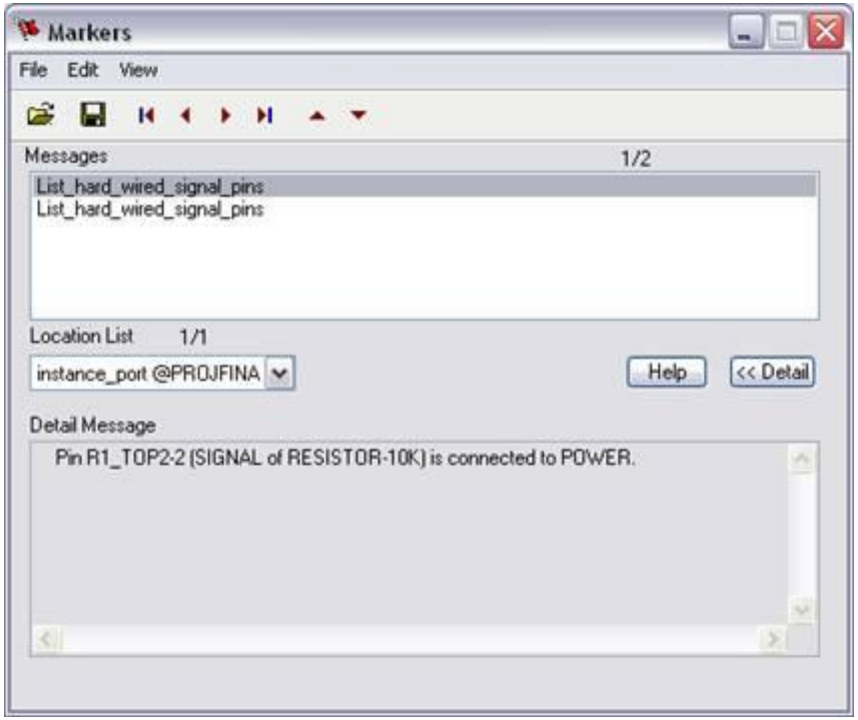
- TestWay can export eDfT reports in a format directly useable on native schematic tools
- TestWay converts rules checks in a Marker file for Cadence. The TestWay results are fully interactive with Concept HDL

Increase designer acceptance to participate in DfT

new



Messages 1/2

List_hard_wired_signal_pins
List_hard_wired_signal_pins

Location List 1/1

instance_port @PROJFINA

Detail Message

Pin R1_TOP2-2 (SIGNAL of RESISTOR-10K) is connected to POWER.

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# Test Coverage

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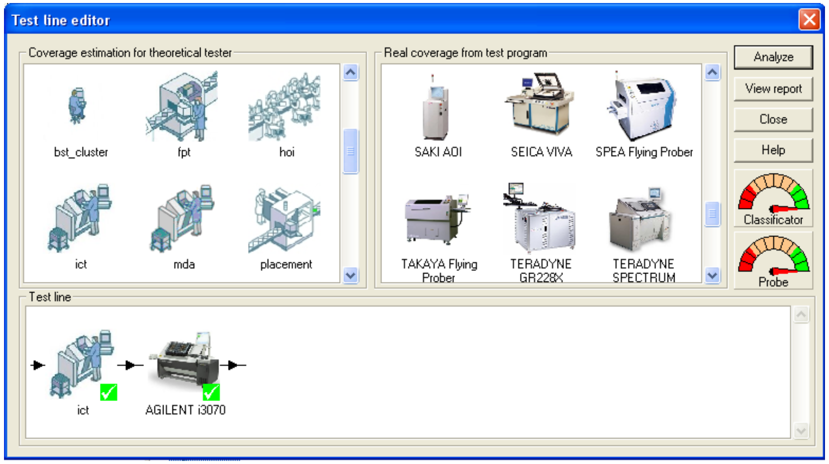
- TestWay & twExpress supports coverage estimation (theoretical test) and coverage measurement (from real/debugged test program):



- Use the latest version incorporating many updates and get more accuracy with:

TestWay HD …High Definition

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# Test Coverage

- To change the weighting of Open and Quality (Electrical test versus optical inspection), it is possible to set a percentage of solder DPMO for each category of defect

- In the example below, there is 20 PPM per solder joint, 10% for quality (2PPM) and 90% for Open (18PPM).

```
Type * -> Soldering_PPM = 20
Type * -> Quality_ratio = 10, OC_ratio = 90
```

# Test Coverage Measurement

## More than 50 coverage importers

Acculogic (BS, Scorpion, SPRINT), Aeroflex (IFR4200,IFR5800), KeySight (SJ10, **SJ50,** 5DX, x6000, i1000, i3070, x1149), ASSET, Checksum, CORELIS, **CyberOptics**, **DrEschke**, EuroPlacer, GOEPEL (CASCON, OPTICON), JTAG Tech, **KohYoung**, **Matrix**, **MIRTEC, MODUS**, **MVP**, MYDATA, **OMRON**, Orbotech (TRION, S22, S36), **Phoenix|Xray, SAKI (BF-Tristar, BF-Frontier, BF-X2),** SEICA, SPEA (3030, 4040), **TAKAYA** (APT800, APT8000, APT9000, **APT1400**), TERADYNE (**GR228x, TS124**, **Spectrum**, Z1800), TRI (TR518, TR5001, TR7500, TR8001), VISCOM, ViTechnology, ViTrox (V510, V810), **WIZE**, XJTAG, YESTech

# New concept of test exporter

- The available tools (Demille, FabMaster, Vayo, Camcad) have used the same architecture (CAD & BOM import, probe placement, test export) for many years
- TestWay propose a new vision of the Design To Test process:
  - ✓ CAD & BOM import
  - ✓ Probe placement
  - ✓ Coverage estimation (test balancing)
  - ✓ Test export based on the coverage estimation

new

- Accurate test coverage report prior to debug !

# Test exporters

- The test strategies simulation results are used to automate the assembly, test and inspection program generation
- Assembly machine, in-circuit test (ICT), flying-probe, X-Ray, Automated Optical Inspection (AOI), Boundary-Scan test and Wiring (cable & backplane) tests are all fully supported
- new Test programs are optimized using test balancing (test distribution) over the manufacturing line. The results show a reduced size test program (cheaper to debug, faster to execute), higher throughput (increased revenues)

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# Test exporters

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ACCULOGIC
AEROFLEX
KEYSIGHT TECHNOLOGIES
ASSET
Assembléon
CORELIS
CHECKSUM
CYBEROPTICS
europlacer
GOPEL electronic
JTAG TECHNOLOGIES™
MIRTEC
MYDATA automation WORLDWIDE
SAKI
Seica
SPEA
TAKAYA CORP.
TERADYNE
TRI Test Research, Inc.
ViTrox

new

## More exporters

Acculogic (BS), Aeroflex (IFR4200,IFR5800), KeySight (SJ10, SJ50, i1000, **i3070**, x1149), ASSET, Checksum, CORELIS, CyberOptics, Europlacer, GOEPEL (CASCON, OPTICON), JTAG Tech, MIRTEC, **MYDATA**, SAKI, (BF-Tristar, BF-Frontier, **BFX2**), **SEICA (GRPilot, S20),** SPEA (3030, 4040), TAKAYA (APT800, APT8000, APT9000, **APT1400**), TERADYNE (GR228x, TS124, Spectrum, Z1800), TRI (TR518, TR5001, TR7500, TR8001), ViTrox (V510, **V810**), **WIZE**, XJTAG

# TS12x exporter

- TestWay generates input files for TS12x
  - ✓ Select part by GR228X_MODEL attribute
  - ✓ Generate NAV files natively
  - ✓ Generate CKT file for compatibility
  - ✓ Generate template of models (.DTS)  for ICs

# Takaya exporter

- TestWay generates input file for Takaya
  - ✓ Short Circuit tests
  - ✓ Passive components (resistor, inductor, capacitor, diode, zener, transistor, FET)
  - ✓ Sub-component test based on SPLIT (array, LED in connector, coil in transformer…)
  - ✓ Manage components mounted in parallel
  - ✓ Automatic computation of equivalent value of parallel components (even thru low resistive components)
  - ✓ Diode tests, Open-Checker
  - ✓ Camera support
  - ✓ Absence test for not-mounted components

# Takaya exporter

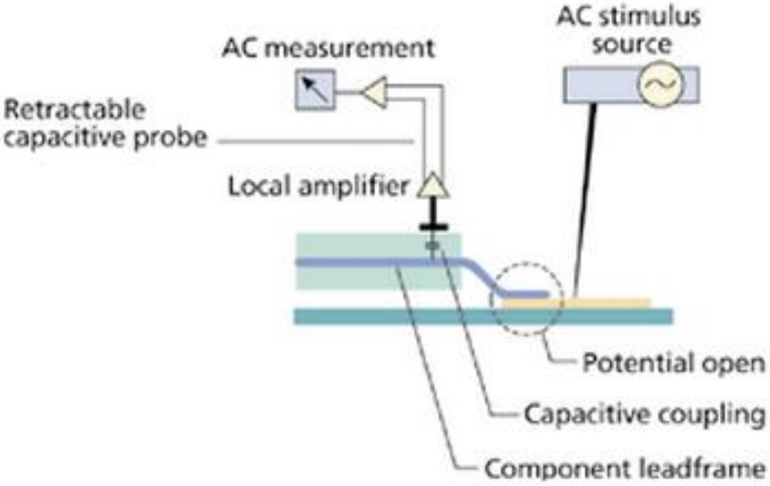
- TestWay optimizes the test program:
  - ✓ Manage single side or dual side testing
  - ✓ Avoid probe contact on pin under test
  - ✓ DriveThru: When a net is not accessible, gain test access via a serial resistor or low resistive component
  - ✓ Takaya strategizer: select the most appropriate test strategy available on the Takaya
  - ✓ Boundary-Scan optimizer: remove Takaya tests already covered by Boundary-Scan. Support: Asset, Acculogic, Goepel, JTAG Technologies, Flynn/OnTAP, Goepel, XJTAG
  - ✓ Custom Takaya models by PartNumber or component type (Re-Use FabMaster models configuration APT*.CNF & library APTMODEL.CNF)

# Takaya exporter

## Open-Checker probe placement

new

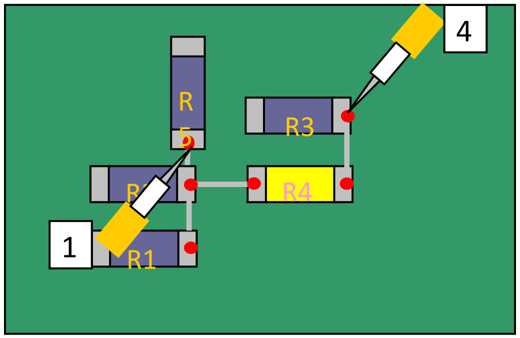
- ✓ The optimum location for the Open-checker sensor is automatically computed: Near the wired bonding which connect the pin to the die, far as possible from the stimulus test point
- ✓ TestWay includes now 3 algorithms to manage small, medium and large components

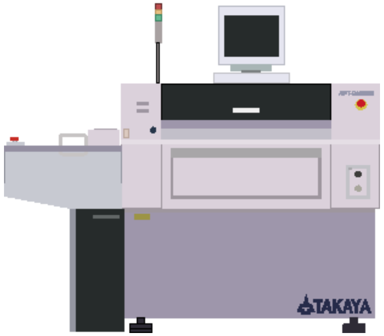


# Takaya exporter

## ↳ Advanced features

- ✓ Increase Test Coverage
  - “Drive thru” & Cluster Testing,
- ✓ Reduce Test Time
  - Intelligent probe placement
  - Overlapping test optimization
- ✓ Minimize debug time
  - Automatic probe selection
  - Parallel measurement calculators
- ✓ Maximize test reliability
  - Intelligent probe placement
- ✓ Improve machine throughput
- ✓ Produce accurate coverage reports





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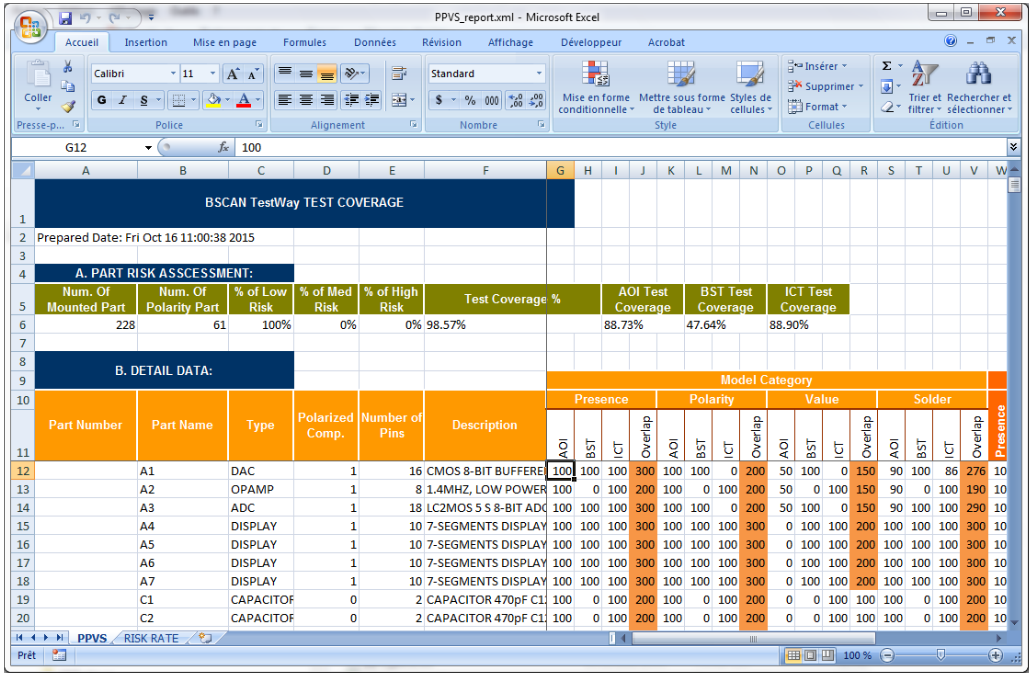
# Script & Report

- New scripts have been developed to report test coverage in a more readable format
  - ✓ PCOLA_report.scr
  - ✓ PPVS_report.scr
- The scripts exports a Excel/XMLSS format

new



BSCAN TestWay TEST COVERAGE

Prepared Date: Fri Oct 16 11:00:38 2015

A. PART RISK ASSCESSMENT:

| Num. Of Mounted Part | Num. Of Polarity Part | % of Low Risk | % of Med Risk | % of High Risk | Test Coverage % | AOI Test Coverage | BST Test Coverage | ICT Test Coverage |
|---|---|---|---|---|---|---|---|---|
| 228 | 61 | 100% | 0% | 0% | 98.57% | 88.73% | 47.64% | 88.90% |

B. DETAIL DATA:

| | | | | | | Model Category | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Presence | | | | Polarity | | | | Value | | | | Solder | | | | |
| Part Number | Part Name | Type | Polarized Comp. | Number of Pins | Description | AOI | BST | ICT | Overlap | AOI | BST | ICT | Overlap | AOI | BST | ICT | Overlap | AOI | BST | ICT | Overlap | Presence |
| | A1 | DAC | 1 | 16 | CMOS 8-BIT BUFFERE | 100 | 100 | 100 | 300 | 100 | 100 | 0 | 200 | 50 | 100 | 0 | 150 | 90 | 100 | 86 | 276 | 10 |
| | A2 | OPAMP | 1 | 8 | 1.4MHZ, LOW POWER | 100 | 0 | 100 | 200 | 100 | 0 | 100 | 200 | 50 | 0 | 100 | 150 | 90 | 0 | 100 | 190 | 10 |
| | A3 | ADC | 1 | 18 | LC2MOS 5 S 8-BIT ADC | 100 | 100 | 100 | 300 | 100 | 100 | 0 | 200 | 50 | 100 | 0 | 150 | 90 | 100 | 100 | 290 | 10 |
| | A4 | DISPLAY | 1 | 10 | 7-SEGMENTS DISPLAY | 100 | 100 | 100 | 300 | 100 | 100 | 100 | 300 | 0 | 100 | 100 | 200 | 100 | 100 | 100 | 300 | 10 |
| | A5 | DISPLAY | 1 | 10 | 7-SEGMENTS DISPLAY | 100 | 100 | 100 | 300 | 100 | 100 | 100 | 300 | 0 | 100 | 100 | 200 | 100 | 100 | 100 | 300 | 10 |
| | A6 | DISPLAY | 1 | 10 | 7-SEGMENTS DISPLAY | 100 | 100 | 100 | 300 | 100 | 100 | 100 | 300 | 0 | 100 | 100 | 200 | 100 | 100 | 100 | 300 | 10 |
| | A7 | DISPLAY | 1 | 10 | 7-SEGMENTS DISPLAY | 100 | 100 | 100 | 300 | 100 | 100 | 100 | 300 | 0 | 100 | 100 | 200 | 100 | 100 | 100 | 300 | 10 |
| | C1 | CAPACITOF | 0 | 2 | CAPACITOR 470pF C1 | 100 | 0 | 100 | 200 | 100 | 0 | 100 | 200 | 0 | 0 | 100 | 100 | 100 | 0 | 100 | 200 | 10 |
| | C2 | CAPACITOF | 0 | 2 | CAPACITOR 470pF C1 | 100 | 0 | 100 | 200 | 100 | 0 | 100 | 200 | 0 | 0 | 100 | 100 | 100 | 0 | 100 | 200 | 10 |

# Crystal Report XI

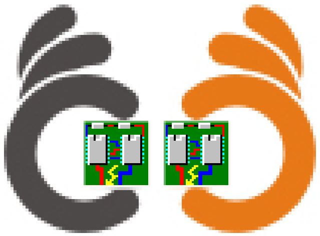
Crystal Reports XI

- TestWay supports Crystal Reports 8.5 up-to version 11.5 R2
- Crystal Reports is a business intelligence application used to design and generate reports from a wide range of data sources
- It allows users to graphically design data connection(s) and report layouts. In the Database Expert, users can select and link tables from a variety of data sources, including Microsoft Excel spreadsheets. Fields from these tables can be placed on the report design surface, and can also be used in custom formulas

# Comparative Data Checker

- ComparativeDataChecker quickly determines the differences between two projects including Computer Aided Design (CAD) and Bill of Materials (BOM)
- You can easily identify differences in new CAD revisions:
  - ✓ Parts Compare
  - ✓ Part Centroid Changes
  - ✓ Part Rotation Changes
  - ✓ Part Footprint Changes
  - ✓ Part PartNumber Changes
  - ✓ Part Value Changes
  - ✓ Netlist Changes
  - ✓ **Bed of nails re-use**

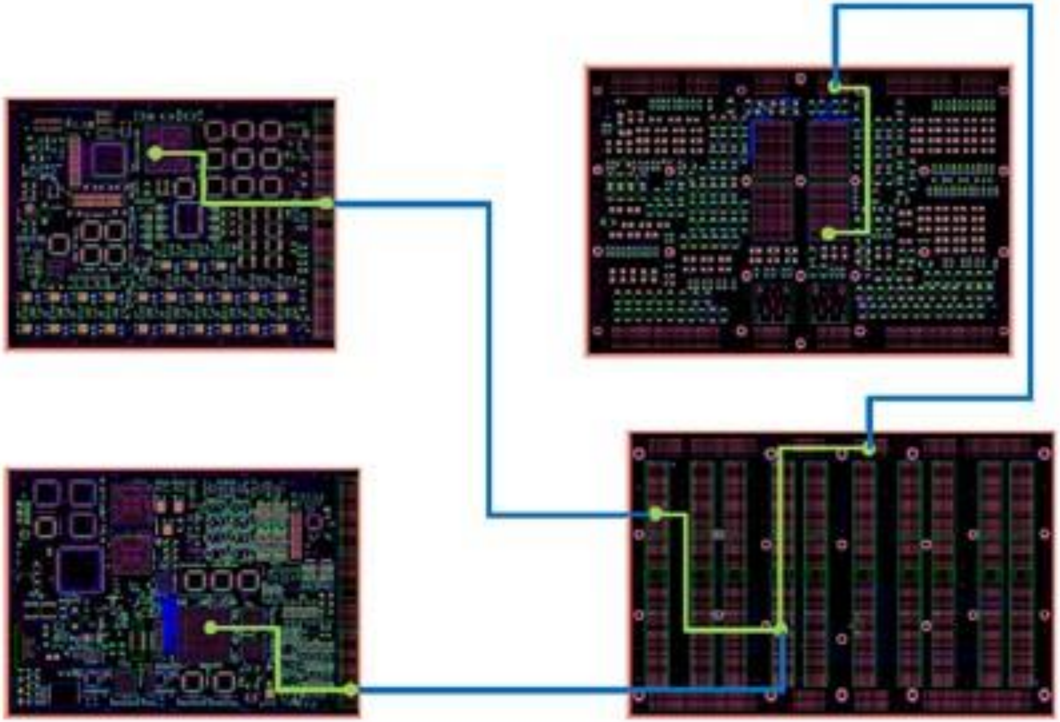
new



# System viewer - twSystem

TestWay 2015

- TestWay Objectives
- Support
- Updated eTraining
- Embedded HELP
- OS Support
- Solution convergence
- CAD import
- Test Point ➔ CAD
- Probe Analyzer
- CAD translation
- Test Coverage
- Tester exporters
- Script & report
- CAD Compare
- System viewer
- twDocumentor
- twECO



➯ **twSystem** is designed to import native CAD data, from all the most popular CAD tools, for each board comprising the system. In addition, a formal description of the backplane or cables is used to describe the interconnection of the boards

# System viewer - twSystem

## TestWay 2015

- TestWay Objectives
- Support
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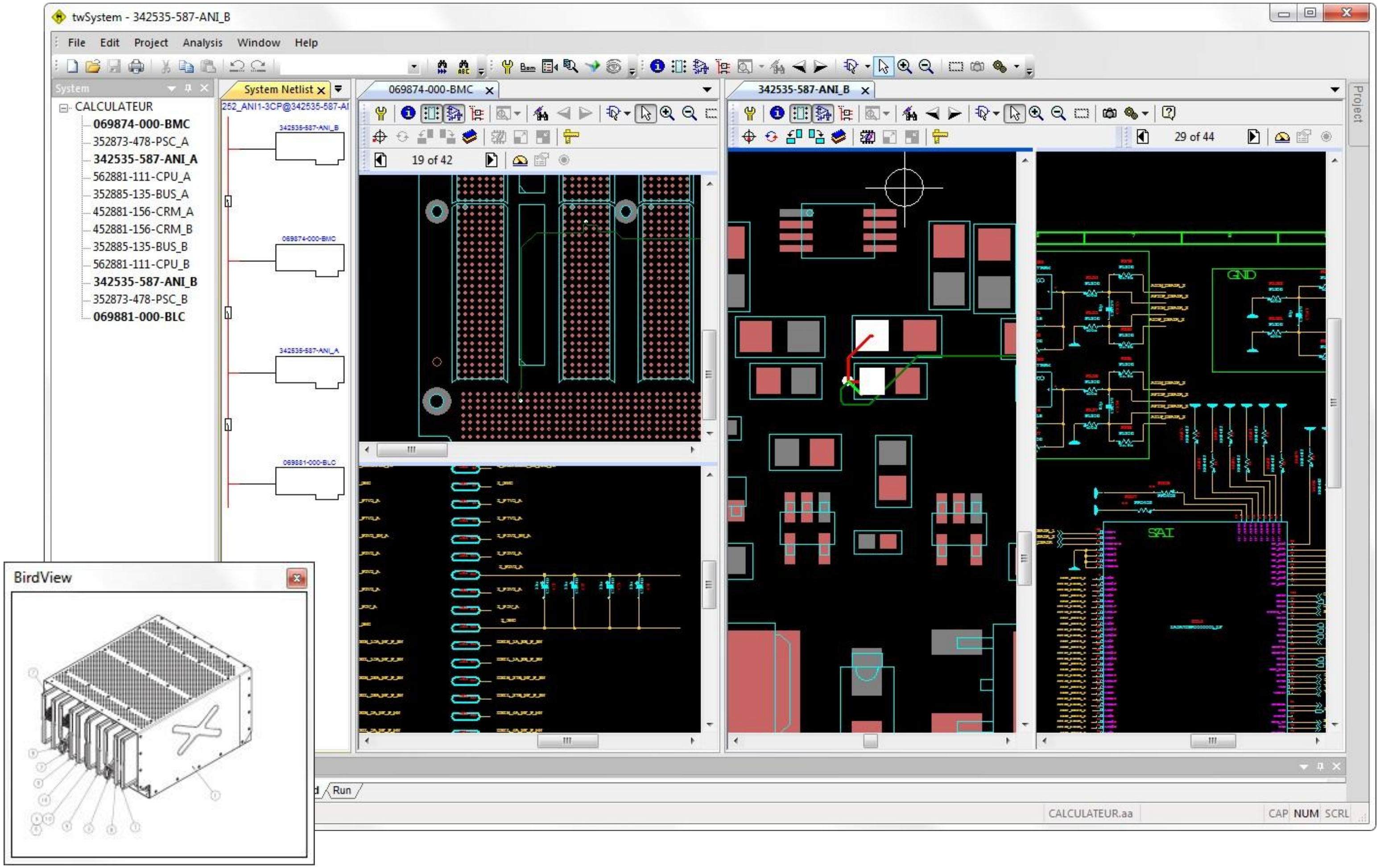
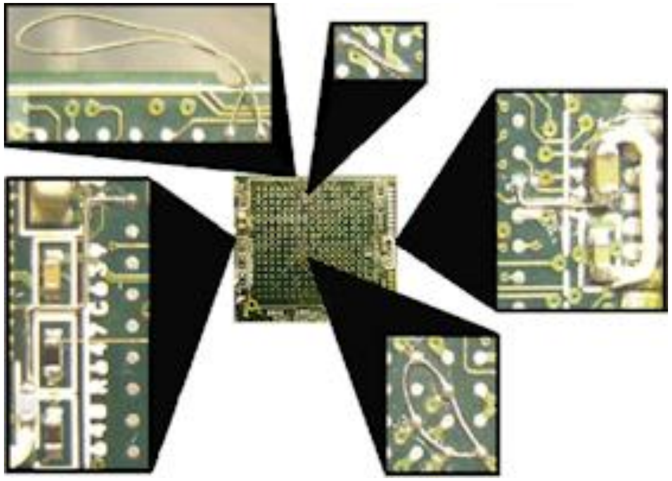
- Tester exporters
- Script & report
- CAD Compare
- **System viewer**
- twDocumentor
- twECO



# twDocumentor

- twDocumentor® is a powerful document management tool that allows quick and easy creation of comprehensive shop floor documentation, as well as the formatting of testability analysis reports
- It is a dedicated toolbar add-in for MS-Word that allows direct access to TestWay Express and QuadView
  - ✓ Load one of the previously created templates using MS-Word, select the TestWay project to document, and then start creating the report
  - ✓ Output formats available: DOC, PDF or HTML

# twECO – Engineering Change Order



- Fully integrated within QuadView is the new ECO toolbar to handle post fabrication PCB modifications such as track cuts, drilled vias, wire straps, component addition or removal and glue dots, etc...

- All these actions are automatically documented and may be exported to twDocumentor® or as a text file

# Contact

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