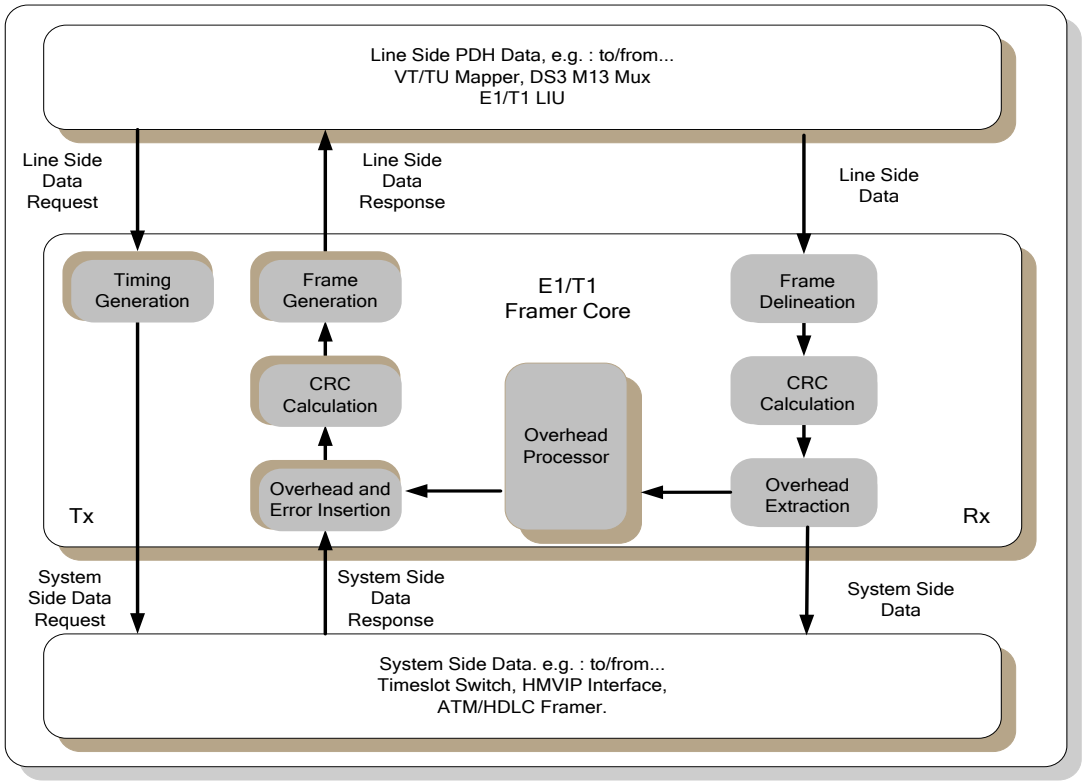
e1t1 Mapper/Framer
Product Brief

Overview

Aliathons's Multi-Channel E1/T1/J1 Framer Core provides a flexible, resource-efficient, high-density programmable logic based solution for PDH interfacing. Running at 155MHz, it is capable of framing and deframing up to 1008/1344 E1/T1 channels (enough for a full OC48/STM16).

Block Diagram



Key Features

- Conforms to ITU G.704/ANSI T1.403.
- Best-in-Class size and performance and supports many hundreds of channels.
- Generates and performs frame synchronization for the following PDH signals: T1 – (ESF/SF), J1, E1 – (CRC/Non-CRC/ G.706 Interworking)
- Calculates and inserts CRC; reports CRC values for T1 (ESF), J1 and E1.
- Frame format of each channel may be configured dynamically and independently.
- Supports independent timing on every channel while providing frame overhead insertion and extraction interfaces.
- Provides frame overhead error injection interface and a byte-wide, frame-aligned timeslot input interface. Implements a byte-wide frame aligned payload output interface.
- Accepts multiple input streams, making it ideal for interfacing to channelized VT/TU Mappers or multi-channel LIUs.
- Output data streams may dynamically range between 1 and 8 bits wide, allowing seamless interfacing to SONET/SDH VT/TU mappings.
- Full Overhead and Defect processing per channel including. OOF, AIS, FAS, CRC, E-Bit, RAI, SEF.
- Performance Monitoring counters (FAS, CRC, E-BIT). Upstream/Downstream Consequent Action.

e1t1 Mapper/Framer
Product Brief

Resources

Example Applications		LUTs (4 input)	FFs	Memory (kbit)
84xT1s 63xE1s	RX	1815	1490	108.8
	TX	430	290	6
	Oh. Proc[2]	570	620	27.5
	Total (1)	**2815**	**2400**	**142.3**
168xT1s 126xE1s	RX	1815	1490	217.6
	TX	430	290	12
	Oh. Proc[2]	570	620	55
	Total (1)	**2815**	**2400**	**284.6**
336xT1s 252xE1s	RX	1815	1490	435.2
	TX	430	290	24
	Oh. Proc[2]	570	620	112.7
	Total (1)	**2815**	**2400**	**571.9**
672xT1s 504xE1s	RX	1815	1490	870.4
	TX	430	290	48
	Oh. Proc[2]	570	620	226.5
	Total (1)	**2815**	**2400**	**1144**
1344xT1s 1008xE1s	RX	3600	3000	1740
	TX	870	590	96
	Oh. Proc[2]	570	620	453.7
	Total (1)	**5040**	**4210**	**2287**
Fmax(3)				
> 160 MHz				

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase.
Memory implementation is device dependent and figures may increase on less memory efficient architectures.
Memory figures may be reduced at the expense of logic on some architectures.
2 - If the OH Processor uses external memory to the FPGA the OH Processor Memory figure reduces by 50%.

Contact Us

info@aliathon.com

+44 (0)1383 737 736

www.aliathon.com

Aliathon Ltd

Evans Business Center

Pitreavie Court

Dunfermline, Fife, KY11 8UU

Scotland, UK

Alliances

ALTERA AMPP SM
ALTERA MEGAFUNCTION PARTNERS PROGRAM

XILINX
ALLIANCE PROGRAM

Mentor Graphics