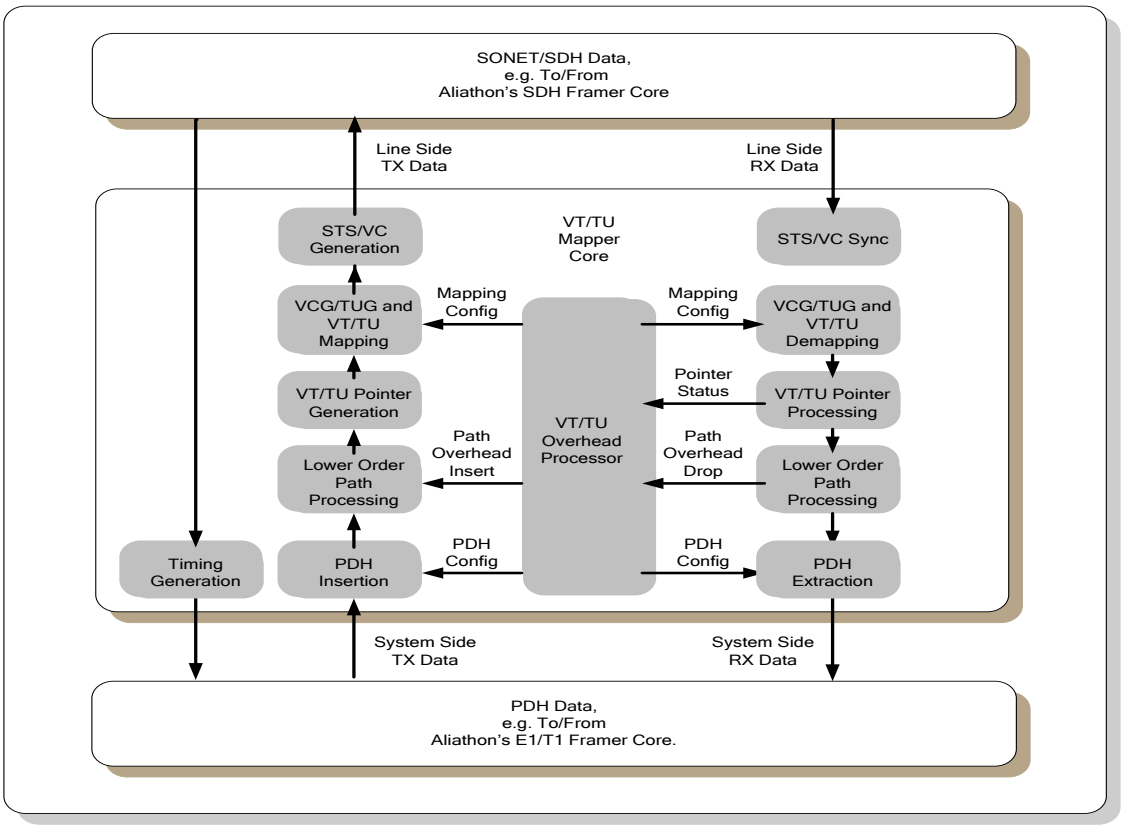
SONET/SDH VT/TU Mapper
Product Brief

Overview

Aliathon's VT/TU Mapper performs the insertion and extraction of PDH signals into or from multiple VT/TU paths. The core handles pointer generation and signal insertion into the transmitted paths as well as the pointer alignment and signal extraction from the received paths. It also performs the lower order path overhead processing for both directions.

Running at over 160MHz, and processing hundreds of Independently configurable TX and RX VT/TU paths concurrently,

Block Diagram



Key Features

- Conforms to ITU G.707/ANSI T1.105.
- Maps/Demaps multiple Lower Order VT/TU paths:
  - VC3 - TUG2 - (TU11 / TU12 / TU2)
  - VC4 - TUG3 - TUG2 - (TU11 / TU12 / TU2)
  - VC4 - TUG3 - TU3
  - STS1 - VCG - (VT1.5 / VT2 / VT6)
- Inserts/Extracts PDH signals for VT/TU and STS/VC containers:
  - DS1 over VT1.5/TU11 or VT2/TU12
  - E1 over VT2/TU12
  - DS2 over VT6/TU2
  - DS3/E3 over STS1/VC3
  - E4 over STS3c/VC4
- Generates/Processes all VT/TU pointers. Calculates and inserts TX VT/TU BIP values. Provides a Path Overhead Insert/drop interface.
- All legal configurations of VT/TU sizes supported, and can be changed dynamically. Supports independent timing of STS/VC inputs/outputs.
- Full Overhead and Defect processing per VT/TU including:
  - LOP, AIS, BIP, eRDI-P/S/C, RFI, REI and LOMF.
  - Trace Messages (J2).
  - Signal Degrade/Excessive Error detection (BIP).
  - Path Label (V5-PL).
  - Performance Monitoring Counters (BIP, REI)
  - Upstream/Downstream Consequent Action.

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Resources

Example Applications		LUTs (4 input)	FFs	Memory (kbit)
84xVT1.5/TU11s 63xVT2/TU12s	RX	1225	1660	9.6
	TX	650	515	7
	Oh.Proc[2,3]	1070	1300	111.7
	Total (1)	**2945**	**3475**	**128.3**
168xVT1.5/TU11s 126xVT2/TU12s	RX	1225	1660	19.2
	TX	650	515	14
	Oh.Proc[2,3]	1070	1300	223.4
	Total (1)	**2945**	**3475**	**256.6**
336xVT1.5/TU11s 252xVT2/TU12s	RX	1225	1660	38.2
	TX	650	515	28
	Oh.Proc[2,3]	1070	1300	419.8
	Total (1)	**2945**	**3475**	**486**
672xVT1.5/TU11s 504xVT2/TU12s	RX	1225	1660	76.5
	TX	650	515	56
	Oh.Proc[2,3]	1070	1300	831
	Total (1)	**2945**	**3475**	**963**
1344xVT1.5/TU11s 1008xVT2/TU12s	RX	2450	3320	153
	TX	1300	1030	112
	Oh.Proc[2,3]	1070	1300	1653
	Total (1)	**4820**	**5650**	**1918**
Fmax(4)				
> 160 MHz				

Deliverables	
IP	EDIF/BIT/SOF file
Simulation	Encrypted Modelsim Back-annotated VHDL
Constraints	QSF or UCF
Documentation	Datasheet

Target families
Altera – Stratix, Arria and Cyclone
Xilinx – Virtex, Kintex, Artix and Spartan
Lattice – ECP2/M and ECP3

1 - Guideline Utilization figures are based on an average sample of the supported architectures and may increase. Memory implementation is device dependent and figures may increase on less memory efficient architectures. Memory figures may be reduced at the expense of logic on some architectures.
2 - If the OH Processor uses memory external to the FPGA the OH Processor Memory figure reduces by 50%.
3 - If Trace Message and SD/EXC processing is not required the OH Processor Memory figure reduces by 50%.
4 - Guideline Performance figures are based on the slowest Speed Grade of the high performance devices and may be less for slower, lower cost, devices.

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XILINX
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Mentor Graphics