## G83/2 Appendix 4 Type Verification Test Report

| Type Approval and manufacturer/supplier declaration of compliance with the requirements of Engineering Recommendation G83/2. | | | |
|---|---|---|---|
| SSEG Type reference number | Photovoltaic Grid-tied inverter | | |
| SSEG Type | ZDNY-TL10000 | | |
| System Supplier name | Solax power Co., Ltd | | |
| Address | Room 220, West Buliding A, National University Science and Technology Park of Zhejiang University 525, Xixi Rd, Hangzhou, Zhejiang Province, China, 310007 | | |
| Tel | +86(0571)-87979860 | Fax | +86(0571)-89988190 |
| E:mail | info@soalxpower.com | Web site | www.solaxpower.com |

| Maximum rated capacity, use separate sheet if more than one connection option. | Connection Option | |
|---|---|---|
| | 10 | kW three phase system |
| | NA | kW single phase system |
| | NA | kW two phases in three phase system |
| | NA | kW two phases split phase system |

SSEG manufacturer/supplier declaration.
I certify on behalf of the company named above as a manufacturer/supplier of Small Scale Embedded Generators, that all products manufactured/supplied by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2.

| Signed | Guo Huawei | On behalf of | Solax power Co., Ltd |
|---|---|---|---|

Note that testing can be done by the manufacturer of an individual component, by an external test house, or by the supplier of the complete system, or any combination of them as appropriate.
Where parts of the testing are carried out by persons or organisations other than the supplier then the supplier shall keep copies of all test records and results supplied to them to verify that the testing has been carried out by people with sufficient technical competency to carry out the tests.

**Power Quality. Harmonics**. The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1

| SSEG rating per phase (rpp) | | | 3.3 | kW | NV=MV*3.68/rpp | |
|---|---|---|---|---|---|---|
| Harmonic | At 50% of rated output | | 100% of rated output | | | |
| | Measured Value (MV) in Amps | Normalised Value (NV) in Amps | Measured Value (MV) in Amps | Normalised Value (NV) in Amps | Limit in BS EN 61000-3-2 in Amps | Higher limit for odd harmonics 21 and above |
| 2 | 0.0235 | 0.0259 | 0.0416 | 0.0459 | 1.080 | |
| 3 | 0.0169 | 0.0187 | 0.0312 | 0.0344 | 2.300 | |
| 4 | 0.0175 | 0.0193 | 0.0311 | 0.0343 | 0.430 | |
| 5 | 0.2267 | 0.2503 | 0.2457 | 0.2713 | 1.140 | |
| 6 | 0.0043 | 0.0047 | 0.0278 | 0.0307 | 0.300 | |
| 7 | 0.1529 | 0.1688 | 0.1637 | 0.1807 | 0.770 | |
| 8 | 0.0059 | 0.0065 | 0.0297 | 0.0328 | 0.230 | |
| 9 | 0.0130 | 0.0144 | 0.0279 | 0.0308 | 0.400 | |
| 10 | 0.0124 | 0.0137 | 0.0286 | 0.0316 | 0.184 | |
| 11 | 0.0975 | 0.1076 | 0.1084 | 0.1197 | 0.330 | |
| 12 | 0.0375 | 0.0414 | 0.0285 | 0.0315 | 0.153 | |
| 13 | 0.0923 | 0.1019 | 0.0789 | 0.0871 | 0.210 | |
| 14 | 0.0217 | 0.0240 | 0.0293 | 0.0323 | 0.131 | |
| 15 | 0.0264 | 0.0291 | 0.0407 | 0.0449 | 0.150 | |
| 16 | 0.0036 | 0.0040 | 0.0279 | 0.0308 | 0.115 | |
| 17 | 0.0354 | 0.0391 | 0.0639 | 0.0705 | 0.132 | |
| 18 | 0.0032 | 0.0035 | 0.0279 | 0.0308 | 0.102 | |
| 19 | 0.0347 | 0.0383 | 0.0491 | 0.0542 | 0.118 | |
| 20 | 0.0062 | 0.0068 | 0.0276 | 0.0305 | 0.092 | |
| 21 | 0.0304 | 0.0336 | 0.0421 | 0.0465 | 0.107 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 22 | 0.0037 | 0.0041 | 0.0255 | 0.0282 | 0.084 | |
| 23 | 0.0202 | 0.0223 | 0.0333 | 0.0368 | 0.098 | |
| 24 | 0.0028 | 0.0031 | 0.0118 | 0.0130 | 0.077 | |
| 25 | 0.0224 | 0.0247 | 0.0240 | 0.0265 | 0.090 | |
| 26 | 0.0034 | 0.0038 | 0.0045 | 0.0050 | 0.071 | |
| 27 | 0.0039 | 0.0043 | 0.0054 | 0.0060 | 0.083 | |
| 28 | 0.0023 | 0.0025 | 0.0044 | 0.0049 | 0.066 | |
| 29 | 0.0142 | 0.0157 | 0.0157 | 0.0173 | 0.078 | |
| 30 | 0.0023 | 0.0025 | 0.0045 | 0.0050 | 0.061 | |
| 31 | 0.0166 | 0.0183 | 0.0145 | 0.0160 | 0.073 | |
| 32 | 0.0022 | 0.0024 | 0.0068 | 0.0075 | 0.058 | |
| 33 | 0.0031 | 0.0034 | 0.0267 | 0.0295 | 0.068 | |
| 34 | 0.0025 | 0.0028 | 0.0365 | 0.0403 | 0.054 | |
| 35 | 0.0127 | 0.0140 | 0.0369 | 0.0407 | 0.064 | |
| 36 | 0.0024 | 0.0026 | 0.0358 | 0.0395 | 0.051 | |
| 37 | 0.0127 | 0.0140 | 0.0344 | 0.0380 | 0.061 | |
| 38 | 0.0023 | 0.0025 | 0.0335 | 0.0370 | 0.048 | |
| 39 | 0.0030 | 0.0033 | 0.0354 | 0.0391 | 0.058 | |
| 40 | 0.0025 | 0.0028 | 0.0330 | 0.0364 | 0.046 | |

Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

| **Power Quality. Voltage fluctuations and Flicker**. The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Starting | | | Stopping | | | Running | |
| | $d_{max}$ | $d_c$ | $d_{(t)}$ | $d_{max}$ | $d_c$ | $d_{(t)}$ | $P_{st}$ | $P_{lt}$ 2 hours |
| Measured Values | 2.00 | 1.86 | 0 | 1.98 | 1.83 | 0 | 0.11 | 0.08 |
| Normalised to standard impedance and 3.68kW for multiple units | NA | NA | NA | NA | NA | NA | NA | NA |
| Limits set under BS EN 61000-3-3 | 4% | 3.3% | 3.3% 500ms | 4% | 3.3% | 3.3% 500ms | 1.0 | 0.65 |

| | | | |
|---|---|---|---|
| Test start date | 2014-10-31 | Test end date | 2014-10-31 |
| Test location | Room 220, West Buliding A, National University Science and Technology Park of Zhejiang University 525, Xixi Rd, Hangzhou, Zhejiang Province, China, 310007 | | |

| **Power quality. DC injection.** The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4 | | | | |
|---|---|---|---|---|
| Test power level | 10% | 55% | 100% | |
| Recorded value | 3.1 mA | 4.4 mA | 6.2 mA | |
| as % of rated AC current | 0.02% | 0.03% | 0.04% | |
| Limit | 0.25% | 0.25% | 0.25% | |

| **Power Quality. Power factor**. The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2 | | | | |
|---|---|---|---|---|
| | 216.2V | 230V | 253V | Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test. |
| Measured value | 0.999 | 0.999 | 0.998 | |
| Limit | >0.95 | >0.95 | >0.95 | |

| **Protection. Frequency tests** The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3 | | | | | | |
|---|---|---|---|---|---|---|
| Function | Setting | | Trip test | | "No trip tests" | |
| | Frequency | Time delay | Frequency | Time delay | Frequency /time | Confirm no trip |
| U/F stage 1 | 47.5Hz | 20s | 47.5Hz | 20.067s | 47.7Hz 25s | No trip |
| U/F stage 2 | 47Hz | 0.5s | 47Hz | 0.554s | 47.2Hz 19.98s | No trip |
| | | | | | 46.8Hz 0.48s | No trip |
| O/F stage 1 | 51.5Hz | 90s | 51.5Hz | 90.065s | 51.3Hz 95s | No trip |
| O/F stage 2 | 52Hz | 0.5s | 52Hz | 0.540s | 51.8Hz 89.98s | No trip |
| | | | | | 52.2Hz 0.48s | No trip |

| **Protection. Voltage tests** The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2 | | | | | | |
|---|---|---|---|---|---|---|
| Function | Setting | | Trip test | | "No trip tests" | |
| | Voltage | Time delay | Voltage | Time delay | Voltage /time | Confirm no trip |
| U/V stage 1 | 200.1V | 2.5s | 199V | 2.544s | 204.1V 3.5s | No trip |
| U/V stage 2 | 184V | 0.5s | 184V | 0.535s | 188V 2.48s | No trip |
| | | | | | 180V 0.48s | No trip |
| O/V stage 1 | 262.2V | 1.0s | 262.2V | 1.056s | 258.2V 2.0s | No trip |
| O/V stage 2 | 273.7V | 0.5s | 273.7V | 0.526s | 269.7V 0.98s | No trip |
| | | | | | 277.7V 0.48s | No trip |
| Note for Voltage tests the Voltage required to trip is the setting ±3.45V. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting ±4V and for the relevant times as shown in the table above to ensure that the protection will not trip in error. | | | | | | |

| **Protection. Loss of Mains test.** The requirement is specified in section 5.3.2, test procedure in Annex A or B 1.3.4 | | | | | | |
|---|---|---|---|---|---|---|
| To be carried out at three output power levels with a tolerance of plus or minus 5% in Test Power levels. | | | | | | |
| For Multi phase SSEGs confirm that the device shuts down correctly after the removal of a single fuse as well as operation of all phases. | | | | | | |
| Test Power | 10% | 55% | 100% | 10% | 55% | 100% |
| Balancing load on islanded network | 95% of SSEG output | 95% of SSEG output | 95% of SSEG output | 105% of SSEG output | 105% of SSEG output | 105% of SSEG output |
| Trip time. Ph1 fuse removed | 0.262s | 0.415s | 0.345s | 0.256s | 0.424s | 0.370s |
| Test Power | 10% | 55% | 100% | 10% | 55% | 100% |
| Balancing load on islanded network | 95% of SSEG output | 95% of SSEG output | 95% of SSEG output | 105% of SSEG output | 105% of SSEG output | 105% of SSEG output |
| Trip time. Ph2 fuse removed | 0.268s | 0.397s | 0.351s | 0.264s | 0.429s | 0.375s |
| Test Power | 10% | 55% | 100% | 10% | 55% | 100% |
| Balancing load on islanded network | 95% of SSEG output | 95% of SSEG output | 95% of SSEG output | 105% of SSEG output | 105% of SSEG output | 105% of SSEG output |
| Trip time. Ph3 fuse removed | 0.273s | 0.423s | 0.356s | 0.253s | 0.434s | 0.378s |
| Note for technologies which have a substantial shut down time this can be added to the 0.5 seconds in establishing that the trip occurred in less than 0.5s. Maximum shut down time could therefore be up to 1.0 seconds for these technologies. | | | | | | |
| Indicate additional shut down time included in above results. | | | | | ms | |

| **Protection. Frequency change, Stability test** The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6 | | | | |
|---|---|---|---|---|
| | Start Frequency | Change | End Frequency | Confirm no trip |
| Positive Vector Shift | 49.5Hz | +9 degrees | | No trip |
| Negative Vector Shift | 50.5Hz | - 9 degrees | | No trip |
| Positive Frequency drift | 49.5Hz | +0.19Hz/sec | 51.5Hz | No trip |
| Negative Frequency drift | 50.5Hz | -0.19Hz/sec | 47.5Hz | No trip |

| **Protection. Re-connection timer**. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5 | | | | | |
|---|---|---|---|---|---|
| Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1. | | | | | |
| Time delay setting | Measured delay | Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1. | | | |
| 30 s | 30 s | At 266.2V | At 196.1V | At 47.4Hz | At 51.6Hz |
| Confirmation that the SSEG does not re-connect. | | No re-connection | No re-connection | No re-connection | No re-connection |

| **Fault level contribution.** The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6 | | | | | |
|---|---|---|---|---|---|
| For a directly coupled SSEG | | | For a Inverter SSEG | | |
| Parameter | Symbol | Value | Time after fault | Volts | Amps |
| Peak Short Circuit current | $i_p$ | | 20ms | 75.4 | 18.3 |
| Initial Value of aperiodic current | $A$ | | 100ms | 73.6 | 22.5 |
| Initial symmetrical short-circuit current* | $I_k$ | | 250ms | 70.8 | 21.7 |
| Decaying (aperiodic) component of short circuit current* | $i_{DC}$ | | 500ms | 69.1 | 20.4 |
| Reactance/Resistance Ratio of source* | $X/R$ | | Time to trip | 0.468s | In seconds |

| **Self-Monitoring solid state switching** The requirement is specified in section 5.3.1, No specified test requirements. | Yes/or NA |
|---|---|
| ZDNY-TL10000 | NA |
| It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0.5 seconds. | |

| Additional comments |
|---|
| |