

With embedded memory occupying 50 percent or more of a typical SoC, custom memories can optimize a design for power, performance, or area to deliver the right chip at the right price for your market.

eFlex embedded memories offer base architectures, proven in silicon, that may be customized for specialty foundry processes, adding or subtracting features to create the right chip.

When Flexibility is Everything

eSilicon's eFlex™ memories provide system-on-chip (SoC) architects with a reliable, affordable method of optimizing their product design. Combining advanced circuit design with industry-leading power-management techniques, eFlex embedded memory can deliver the right blend of power, performance or area (PPA) to make your product a market leader.

About eSilicon Memory IP

Our IP team has been a leading provider of high-quality memory IP since 2000. eFlex memories are available in silicon-proven 14/16nm-180nm technologies, customized to meet challenging PPA requirements for leading foundry and integrated device manufacturer (IDM) processes.

Our modular technology and hand-crafted foundation circuits allow us to quickly and efficiently provide you custom memory IP that meets your exact specifications.

The freedom to specify the power, performance or area of your memories allows you to design your SoC without compromises. We provide this freedom at prices very comparable to standard offerings from other vendors and in very competitive time frames.

Advanced Technology, Proven Silicon

Hundreds of millions of pieces of silicon have been shipped with our embedded memories. Complex ICs for applications such as networking, wireless baseband, high-reliability automotive, media processors, and DSP products have included our IP.

Web Access and Download

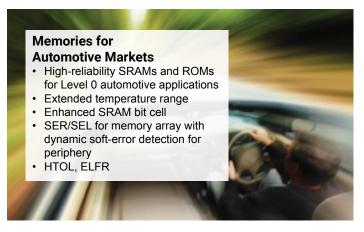
All eSilicon IP is available in Navigator, our online IP evaluation tool, at https://star.esilicon. com. Navigator provides access to eSilicon's full portfolio of IP products. Memory instances may be generated, analyzed and downloaded. Power, performance, and area (PPA) data is pre-loaded for easy data comparison and analysis.

EDA Support

eSilicon memory compilers provide EDA views for leading EDA vendors, helping to ensure seamless integration of our embedded memories into your design flow.

eSilicon Memory IP Offering Types of Memory

- Single-port SRAM
- Dual-port SRAM
- Pseudo 2-port SRAM
- · One-port register file
- Two-port register file
- Cache memories
- ROM
- Asynchronous register file
- Four- to 12-port multi-port register files (MPRF)
- Ternary CAM (TCAM)
- Binary CAM (BCAM)





Architectures

- · High density
- · Ultra-high speed
- Ultra-low power

Processes

- CMOS
- · RF/mixed signal
- Automotive
- · High voltage

Engagement Models

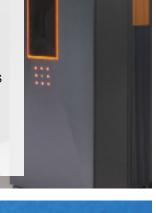
eSilicon offers flexible business models for licensing our embedded memory IP including, but not limited to, a foundrysponsored model and an end-customer-pays model. We also provide a variety of IP services:

Memories for Networking CAMs

- Co-processor for NPU to offload table-lookup tasks
- Fast constant-time lookups over large data array; up to 1.6 BSPS

Multi-Port Register Files

- Enable pipelined processors to access memory from different phases in its pipeline
- Enable super-scalar processors through different cache levels



Memories for Bluetooth & Hearing Aids

- Static RAMs and ROMs with ultra-low voltage support
- Advanced power management circuitry
- Logic-rule bit-cell architectures that are less sensitive to static noise margin
- Unique statistical simulation techniques



eSilicon IP Services

- · Bit-cell development
- Feasibility analysis for aggressive PPA optimization
- Custom memory architectures
- · SRAM process qualifications vehicles
- · Test-chip design and characterization
- · On-site design services
- · Memories for specialty processes

Contact

Please contact us at ipbu@esilicon.com for more information, silicon quality results, white papers or data sheets. To order IP products, please contact sales@esilicon.com or visit Navigator at https://star.esilicon.com.